ENSC 495/851 Final Term (Apr. 15,2014)

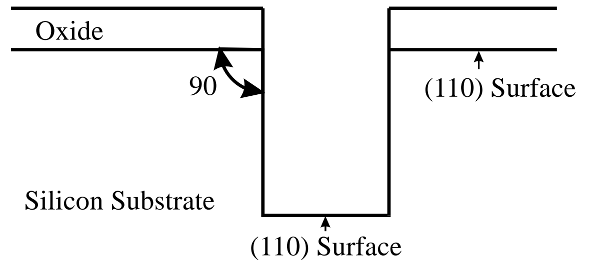
This test is OPEN BOOK: any book, notes and calculator may be used, but not a computer. Time: 3 hr

NOTE: **Do 3 questions in part I 16 marks each for a total of 48 marks**
Do 2 question in part II 26 marks each for total of 52 marks.
Test Total is 100 marks.

Section 1: Do 3 of these 5 questions: 16 marks each

(1) An N type wafer has a stated sheet resistance of 10 ohm-cm.
(1a) How would you confirm this in the lab (state instruments and the formulas used). (2 marks)
(1b) The wafer was patterned and doped with Boron and then Phosphorus to create bipolar transistors. Assume it contains test devices and structures that are at least those you have in the lab work. What test structures and instruments would you then use to verify the P and N+ (last or emitter dopant) sheet resistances? State what would be the important size values in test structures design you would need to know. (6 marks)
(1c) Assume the Boron doping was done similar to the lab 1 method, but with an initial doping of $1000^{o}C$ for 10 minutes (just creates the source) and a drive in of 1100 ^{o}C for 29 minutes. Calculate the junction depth of the resulting diodes. Assume the background N doping is given by the stated sheet resistance. (8 marks).

(2) In vacuum systems what measurement gauge type would be most effective at pressures of (i) $1x10^{-7}$ torr (ii) 1 Pa (convert this to torr) and briefly describe the operation principal of those gauges. (7 marks)
(2b) Give the principle of operation for the two main types of vacuum pumps. Is there a limit to each's upper operating pressure range? What causes the pump to lose effectiveness at its bottom pressure range. (7 marks)
(2c) In a vacuum system that uses a diffusion pump what material must the operator make certain is supplied to the system before the high vac value is opened to the vacuum chamber (not just power to the diff pump). What is a typical upper limit on chamber pressure before the high vac value is opened? (2 marks)



(3a) One proposed way of cooling a wafer is to create vertical channels at the bottom of the IC, with fluid flowing in them (see below). These are fabricated to have the cross section shown below using silicon micromachining of a <110> type wafer. Assume an anisotropic etch is used so that <100>, and <110> are rapidly attacked; while the <111> planes and silicon dioxide attack can be neglected. Assume a quadrangler shaped opening is made in the oxide layer down to the silicon to form the etch mask. What crystal planes must be aligned with the four sides of the oxide opening? Show with a sketch. (list all 4 useful planes, but note that only two planes are used for any structure). (10 marks)
(3b) On the sketch of the quadrangle show the angles that must be defined between the various planes (2 angles mater) (6 marks)

(4a) In IC fabrication name the type of optical photolithographic equipment is used most often for structures larger than 3.0 microns? What type is used for structures 2 microns or less? In which type will the masks last longer and why? (4 marks)
(4b) Name the two types of photoresist. What is the basic process that causes the image to be developed in each case. Do not give details, just a one sentence description of how each resist is changed during exposure and what happens to it during development. (2 marks).
(4c) Sketch how the 1st and 2nd layer alignment structures are aligned to each other when the 2nd mask is a light field one. Do the same for a 2nd mask of the dark field type. (4 marks)
(4d) Chemical mechanical polishing is used in most wafer processing these days for fabrication of 90 nm or smaller critical dimenions. What was the important problem with both the lithography and the fabrication processes that required the move to CMP. (4 marks)

(5) The reaction rate of a given CVD reaction is determined at 600, 650 and 700 ^{o}C. Temperature is found to have little effect on that rate.
(5a) Comment on the relative magnitude of δk_s and D. (2 marks)
(5b) Predict the effect of doubling the reactant concentration N_G. (2 marks)
(5c) Of doubling the gas flow velocity? (4 marks)
(5d) Of reducing the pressure by a factor of 10? (4 marks)
(5e) If the Temperature had a large effect what would that say about the relative magnitude of δk_s and D. (4 marks)

Section 2: Do 2 of these 3 questions: 26 marks each

(6) A layer of poly silicon 500 nm thick is deposited on a gate oxide layer, 40 nm thick, which sits on a <100> silicon substrate. The structure to be patterned is two poly Si lines, 3 microns wide, with 4 microns spaces between each line. After masking a wet etch (nitric acid & HF) removes the poly Si or single crystal silicon at 150 nm per minute. That same etch removes oxide at only 20 nm per min.
(6a) What is the etch time to create the structures (assume only the poly is etched and no overetch) (2 marks)
(6b) If the poly Si thickness varies by +/-13% over the wafer and the etch rate varies by +/-17% how much overetch must occur to guarantee working devices? Show a cross section of the structure after etching with the resist still on it. Calculate the line width and space at the top and bottom of the poly Si for the worse case. What is the average angle of the line edges? What is the appearance of oxide layer and silicon below? (20 marks)
(6c) If no more than 5 nm of gate oxide may be removed what is the maximum amount of overetch allowed (i.e. the limits on the range of material thickness and etch rate). What would the width of the lines be under that condition (worse case – assume the variations in thickness and etch rate are the same percentage)? (4 marks)

(7) In our lab you build a vertical bipolar transistor, in particular the one you measured. Show a cross section of the device (that is through both the base, emitter and collector contacts) after each major process step ie after each deposition/growth/etching step. Assume isotropic wet etching is used when indicating the resist/etched layer appearance. Only show the combined patterned/etch step as one diagram (do not show the resist pattern, and stripped resist steps as separate diagrams). (26 marks)

(8) A 0.1 mA ion implanter beam of 70 KeV P^{31+} ions is scanned across a 200 mm silicon wafer. For these use the implant charts or tables from your notes.
(8a) How long does it take to implant a dose of $3x10^{13}$ atoms/cm^2 (4 marks)
(8b) What is the peak concentration of the dopant? (At what depth will the peak occur concentration occur? Sketch the doing concentration vs depth. What is the surface concentration? (7 marks)
(8d) What type of process needs to be done to activate the dopants? (2 marks)
(8e) The background doping is p type at 10^{14} atoms/cc. Assuming all implanted dopant is activated and ignoring diffusion effects, at what depth will the pn junction be formed? (4 marks)
(8f) An oxide masking layer of 120 nm thick covers all the areas not to be doped with 5 micron widows opened in it. What is the doping concentration at the silicon surface just below the oxide and the total Q in the wafer in those mask protected areas? Plot the concentration with depth in both opening silicon, the edge of the masking oxide window, and the field oxide far from the window. What is the Q total in the areas far from the window. (9 marks)