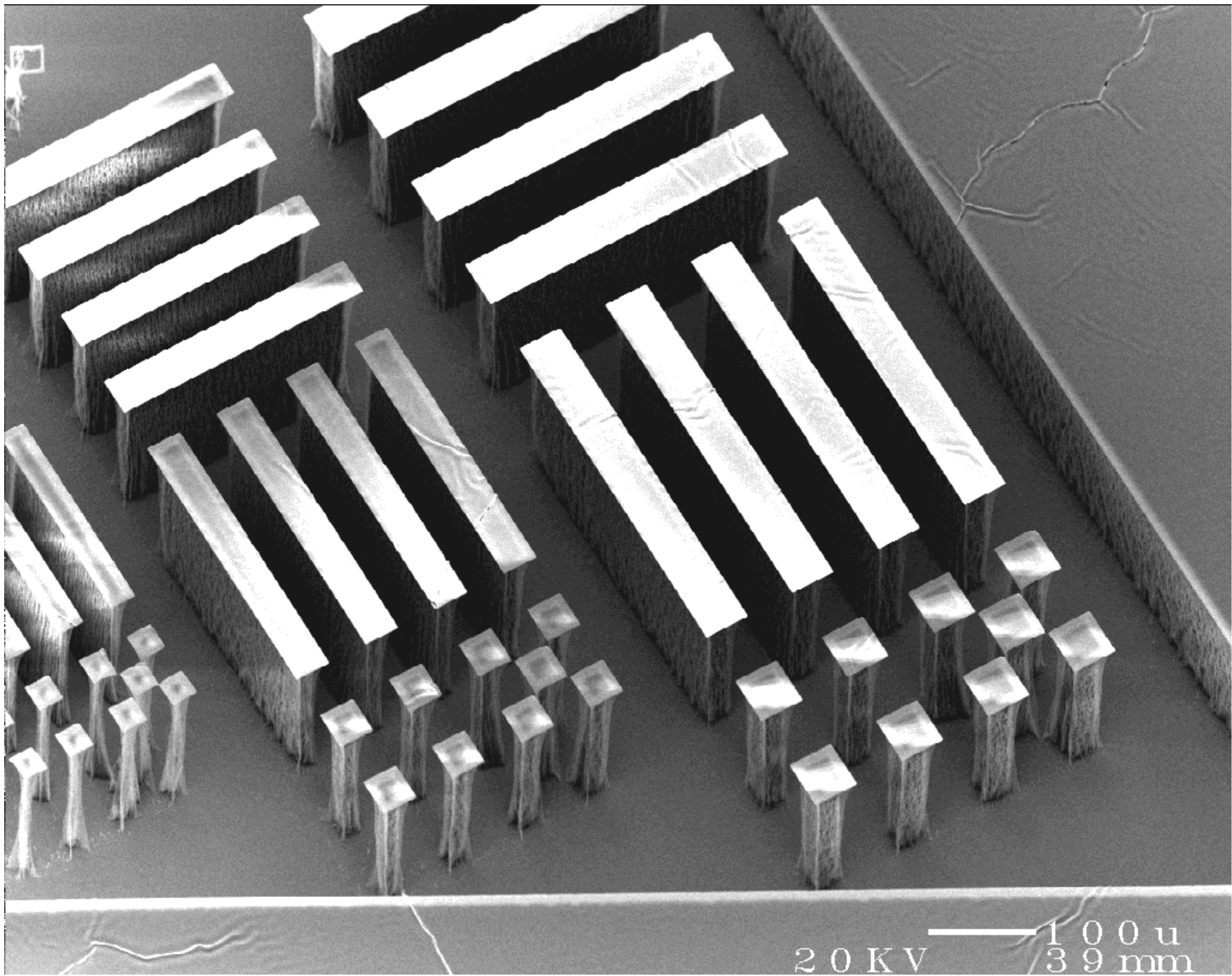
Plasma Etching Rates & Gases

- Gas ratios affects etch rate & etch ratios to resist/substrate

Table 4 Etch Rates and Selectivities for Dry Etching

Material (M)	Gas	Etch Rate (Å/min)	Selectivity		
			M/Resist	M/Si	M/SiO_2
Si	$SF_6 + Cl_2$	1000–4500	5	–	80
SiO_2	$CF_4 + H_2$	400–500	5	40	–
Al, Al–Si, Al–Cu	$BCl_3 + Cl_2$	500	5	5	25
GaAs	$CCl_4 + O_2$	6000	–	–	–



Development of Sidewalls Passivating Films

- Sidewalls get inert species deposited on them with plasma etch
- Creates passivating (non reacting) layers
- Controls how vertical the sidewalls area

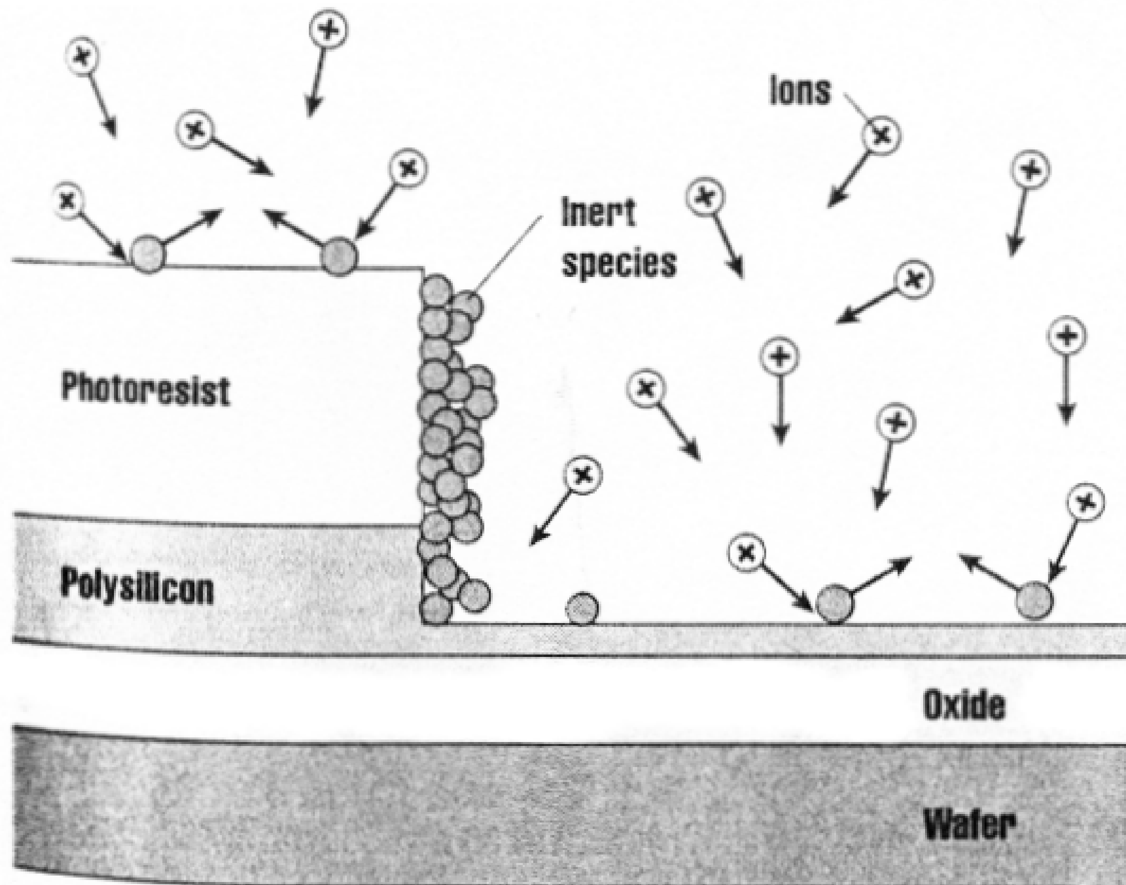


Figure 11-10 Schematic diagram of a high pressure anisotropic etch showing the formation of sidewall passivating films.

Plasma Etch Station

- CVD and Plasma Etch stations identical
- Only difference in chemistry used
- Can have same system do both with plate change
- However if use Chlorine chemistry requires stainless steel
- Much more expensive

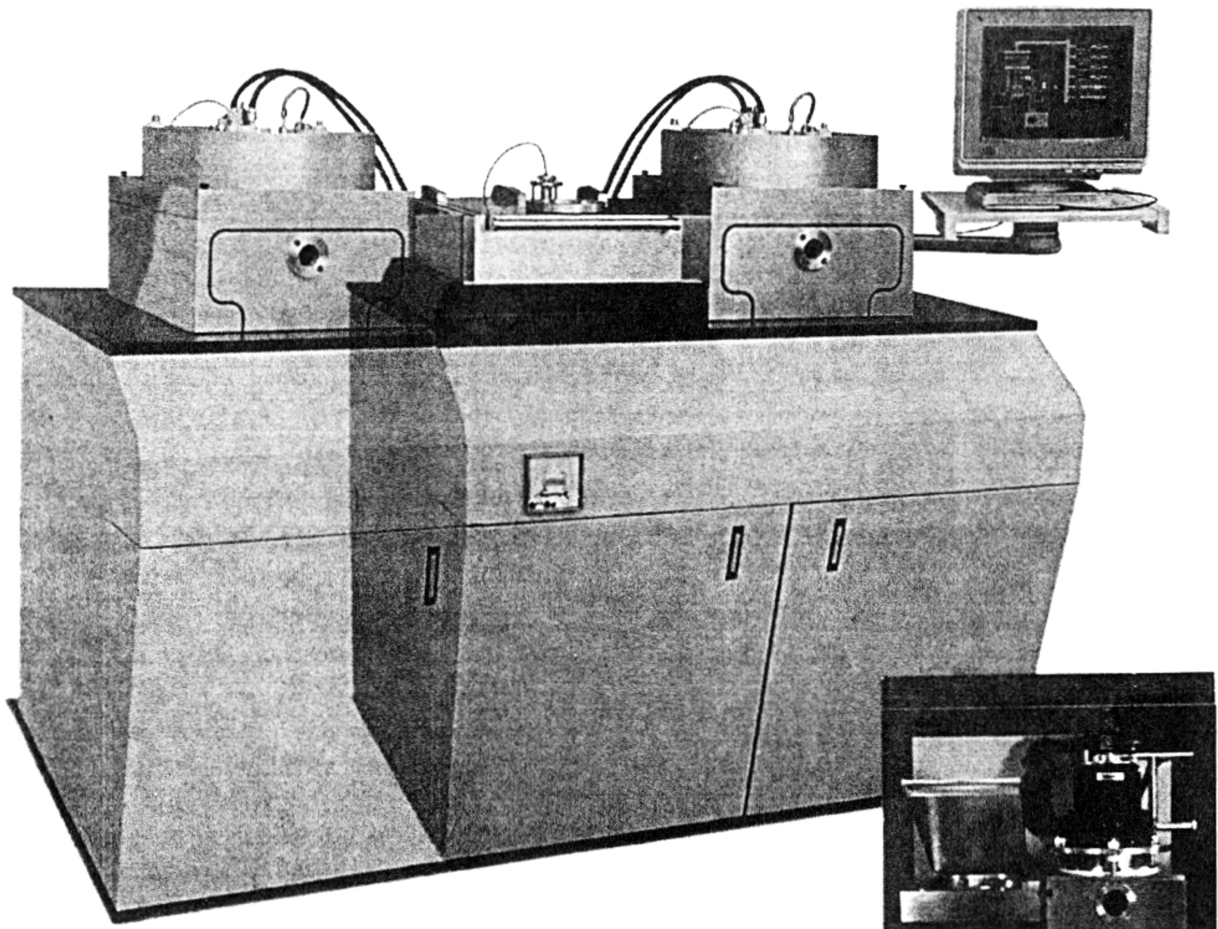


Figure 11-13 Photograph of a computer controlled, dual chamber, parallel plate plasma etch system (*courtesy Plasma Therm*).

Ion Milling

- Removing material in a non reactive mode
- Simple sputtering type process
- ie Sputters material from wafer with Argon (inert)
- Done at low pressures
- Relatively slow process
- Very Anisotropic – voltage directs Argon beam so near verticle
- Problems: tappered edges, photoresist reposition
- Trenching – ie creating deep structures

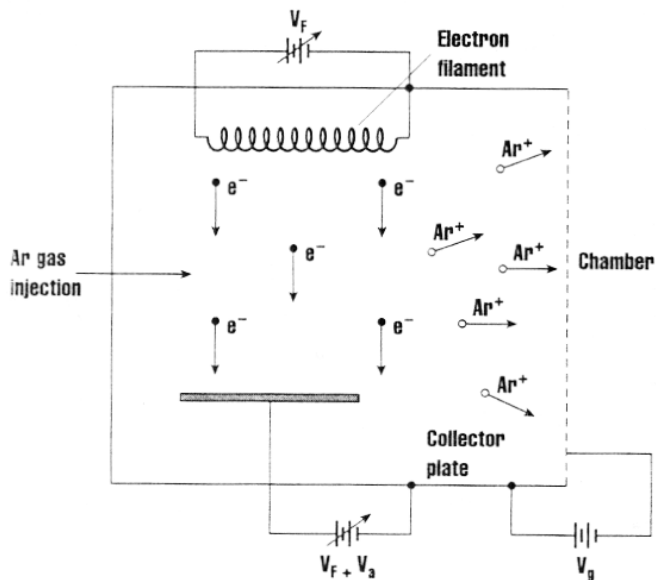


Figure 11-14 Cross section schematic of a Kaufman ion source.

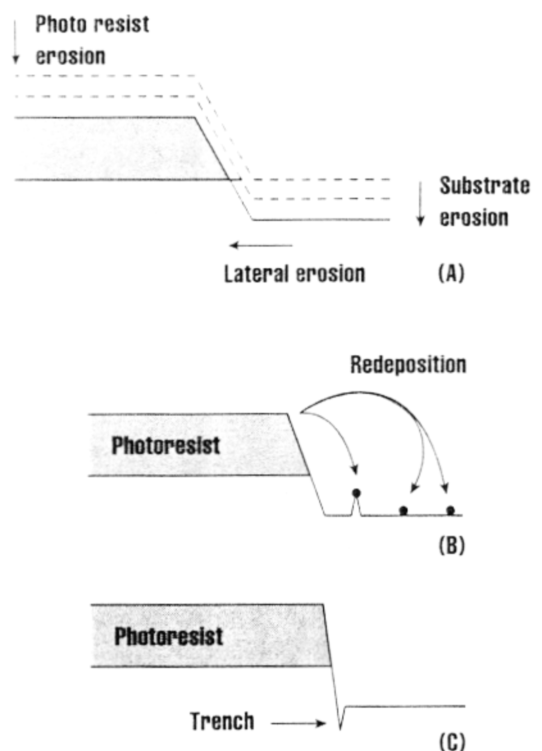


Figure 11-15 Problems that may occur during ion milling: (a) mask taper transfer, (b) redeposition from the mask, and (c) trenching.

Reactive Ion Etching

- Increase electrode/substrate voltage Plasma etch
- Creates ion bombardment like ion milling but with reactive gas
- Called Reactive Ion etchings

Improves Etch Anisotropy in 3 ways

- Sputtering removal of material
- Heating/bond breaking enhances chemical reactions
- Sputtering removal of protective residues
  & redeposition on sidewalls

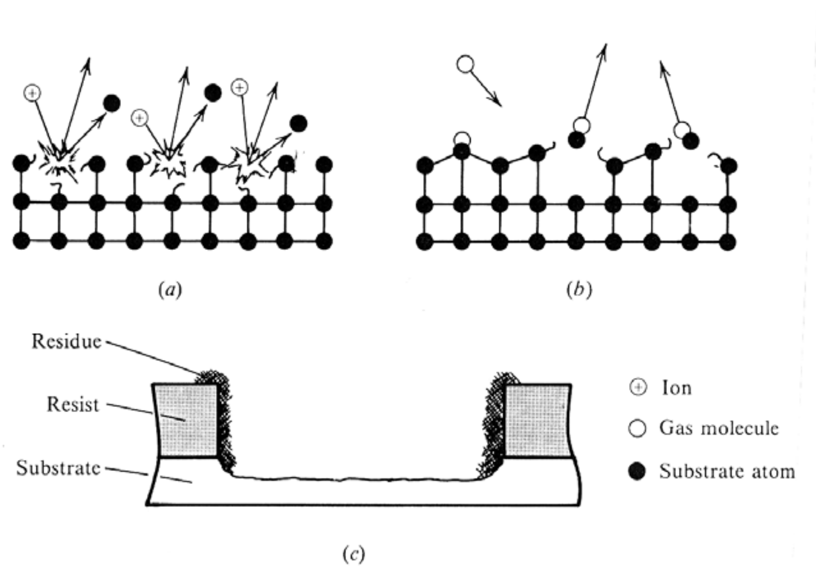
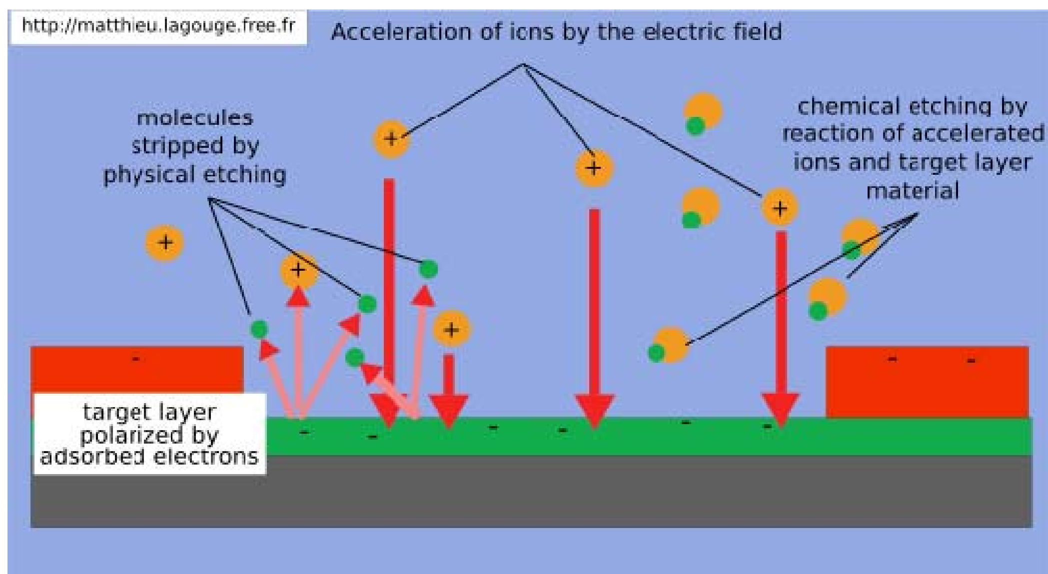


Figure 6-11 Ways in which anisotropic etching is enhanced by ion bombardment in a plasma. (*a*) Sputtering: physical removal of substrate ions. (*b*) Heating and bond loosening accelerate chemical reaction with substrate. (*c*) Sputtering of protective residues in bombarded area enhances reaction rate.



Deep Reactive Ion Etching (Deep RIE)

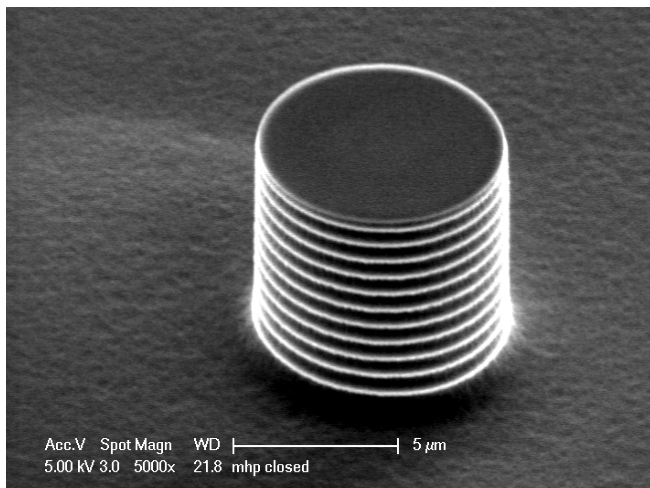
- Creates much deeper, higher aspect ratio etches than RIE
- Enhances the sidewall passivation to obtain
- Bosch process: pulsed or time multiplexed etching

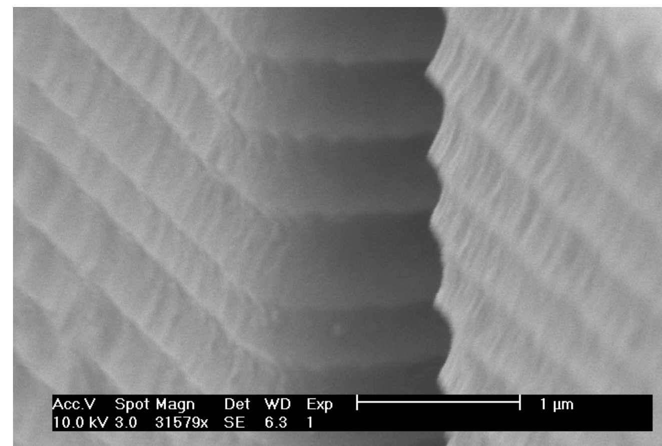
(1) Standard RIE etch with high aspect eg SiF_6 for Silicon

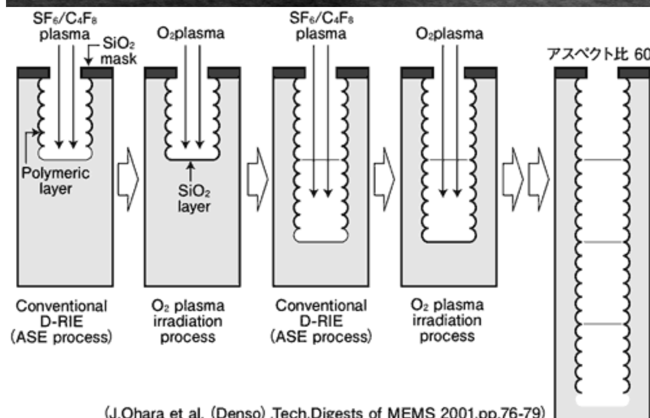
(2) Deposit inert passivation layer on sidewalls

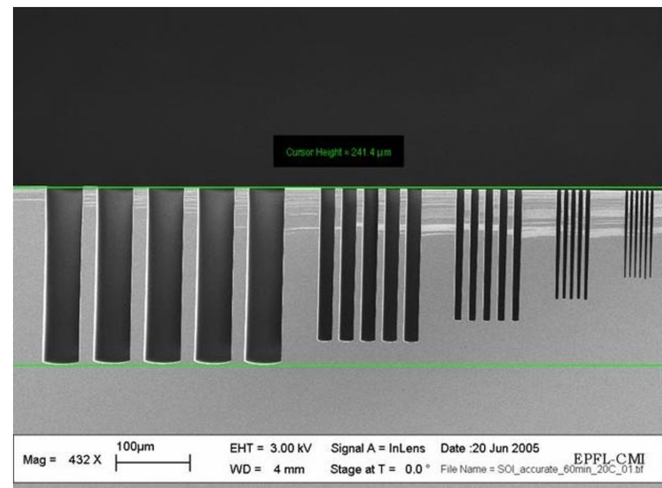
Eg C_4F_6 creates Teflon type coating which prevents sidewall etch

- Repeat these on few second cycle time
- Passivation protects sidewalls and upper surface
- But directional ions etch removes it at the bottom of the hole
- Creates sculpted sidewalls ~100-500 nm cycles
- To etch 500 um (0.5mm) needs 100-1000 cycles



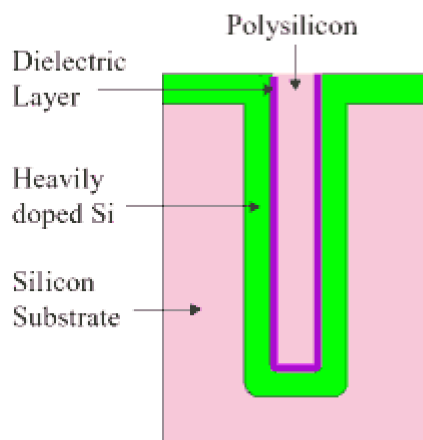


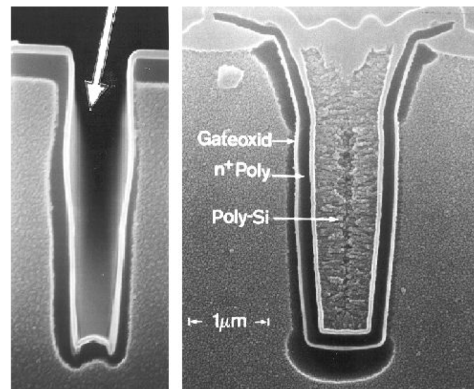


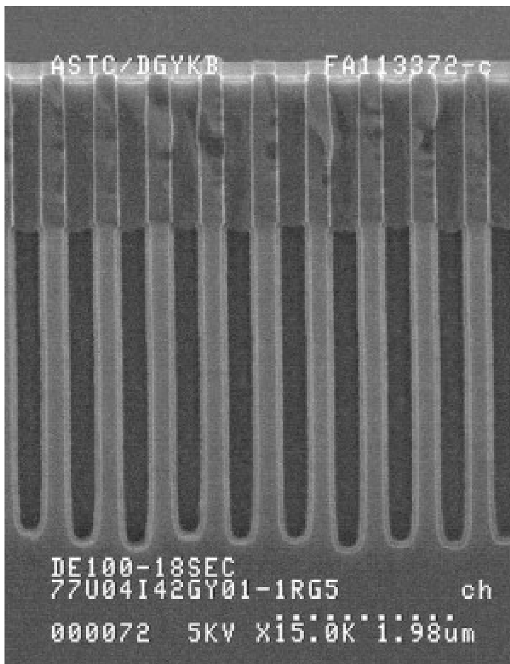


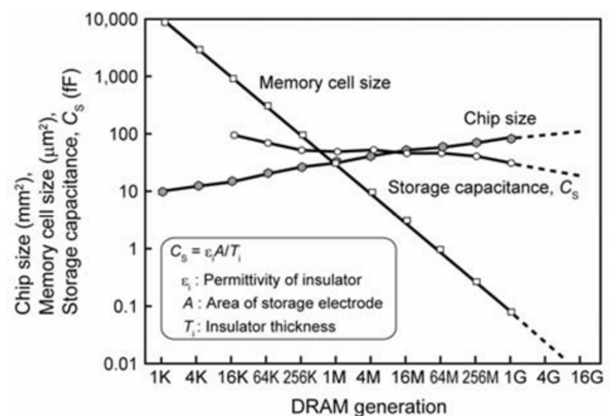
Trench Capacitors

- For DRAM memory as device size shrunk capacitor size fell
- But C depends on area of capacitor
- About 1985 fell to size where Capacitor could not shrink more
- Charge stored reach level where cosmic rays could flip bit
- Solution was to use RIE to create vertical Trench Capacitors
- Deep trenches lined with insulators and conductors
- Now C and charge changes modestly as cell size shrinks
- Get up to 75:1 aspect ratios in this trenches









Example XeF_2 RIE of Si

- Change in flow rate significantly affects etch rate
- Sideways etching is slower, without ion bombardment

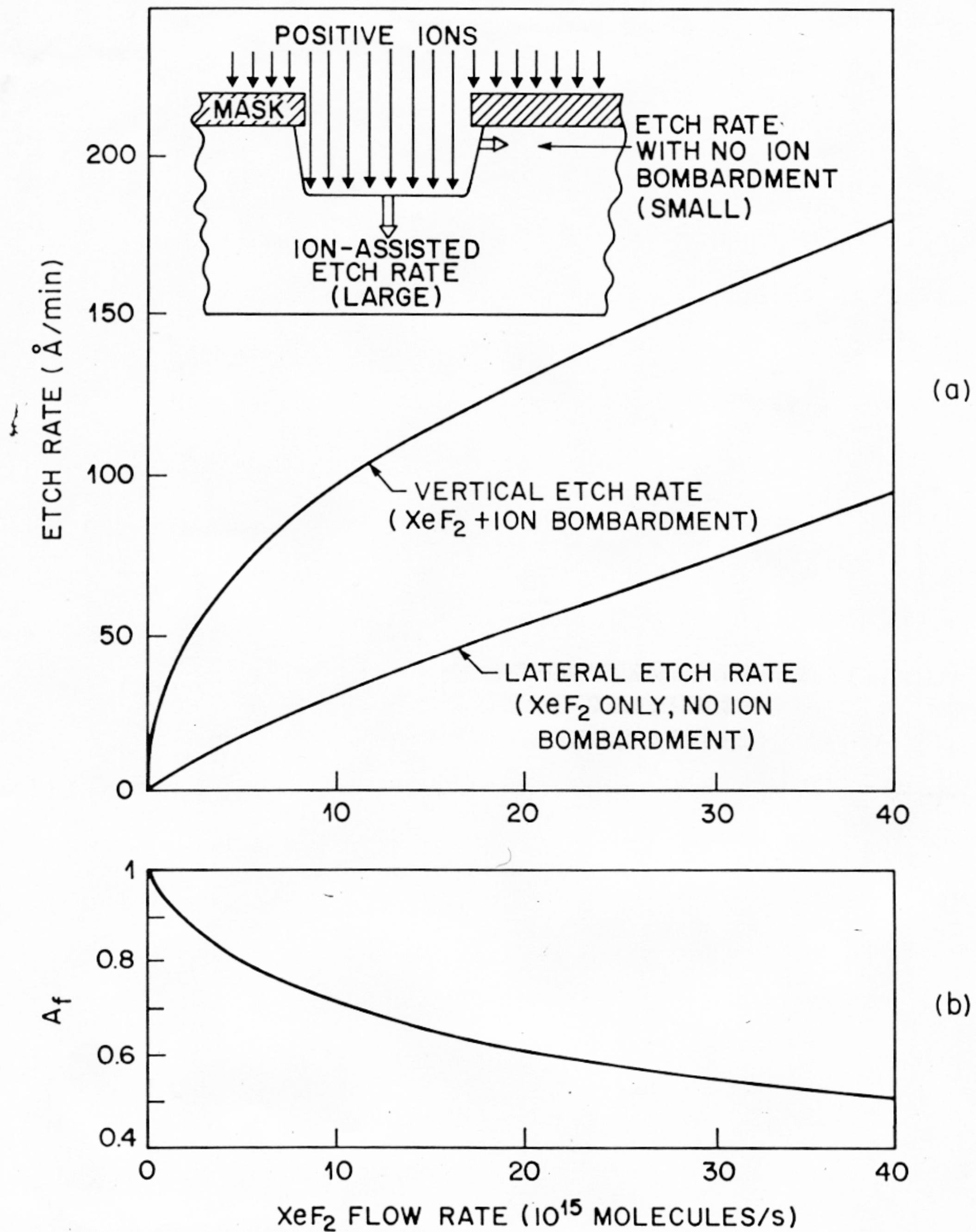


Fig. 29 Silicon etch rate versus XeF_2 flow rate with and without 1-keV Ne^+ bombardment. Insert shows the ion-assisted reaction in the vertical direction.[24]

RIE Reactor Types

- Same basic design as plasma etcher and CVD
- Parallel Plate (1 - 4 at a time)
- Hexode: does many at time

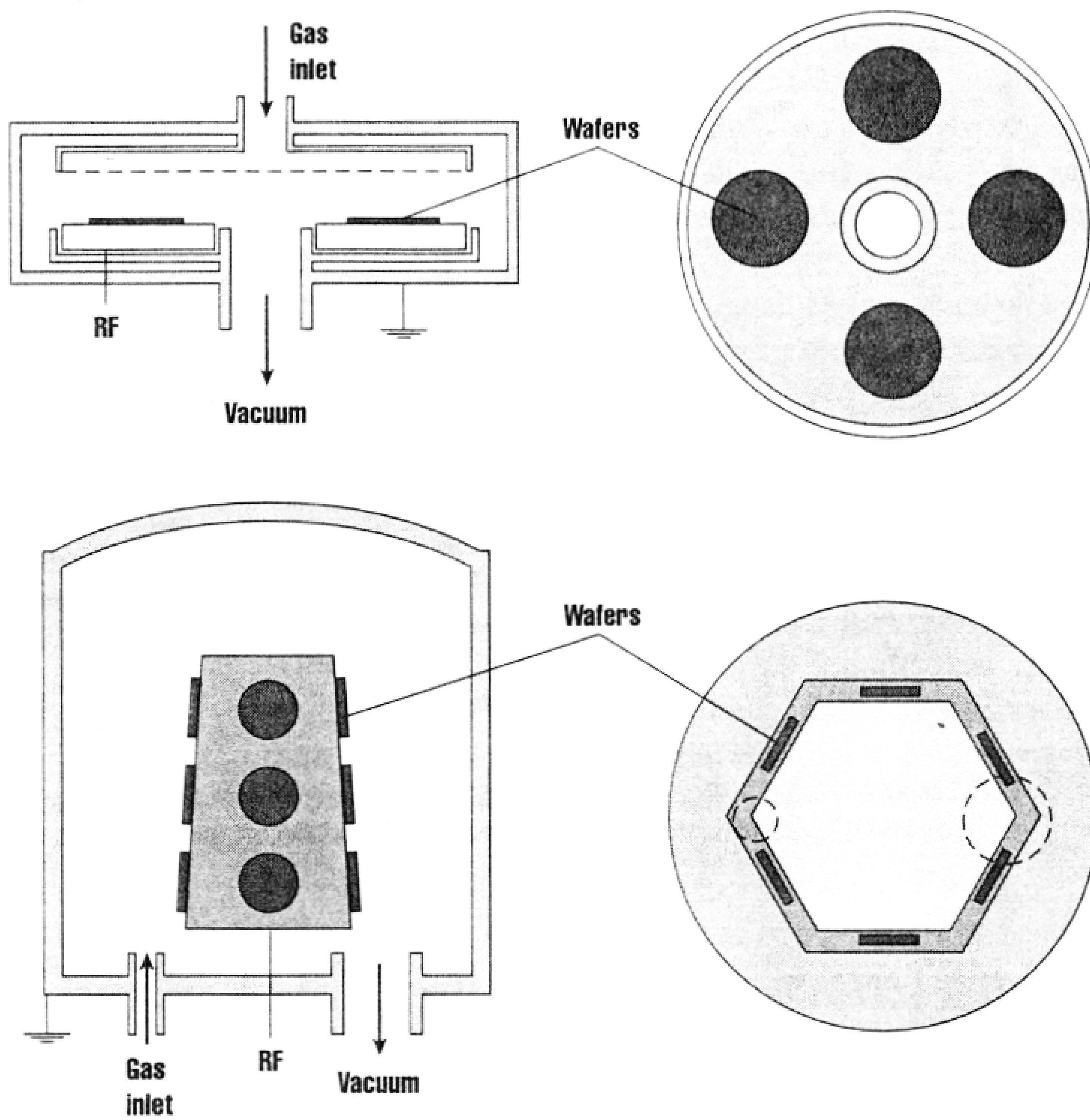


Figure 11-17 Top and side views of parallel plate and hexode batch RIE systems. Typical conditions for either is 50 mtorr and 5 kW/m^2.

Damaged Surface Due to RIE

- Deposit many small layers of unwanted materials
- Comes from reaction with Photoresists and etch material
- eg When etching oxide down to silicon
- Fluorocarbons, Si-O, Si-Carbide, Si damage & H penetration
- Need to remove damage with Anneals at end.

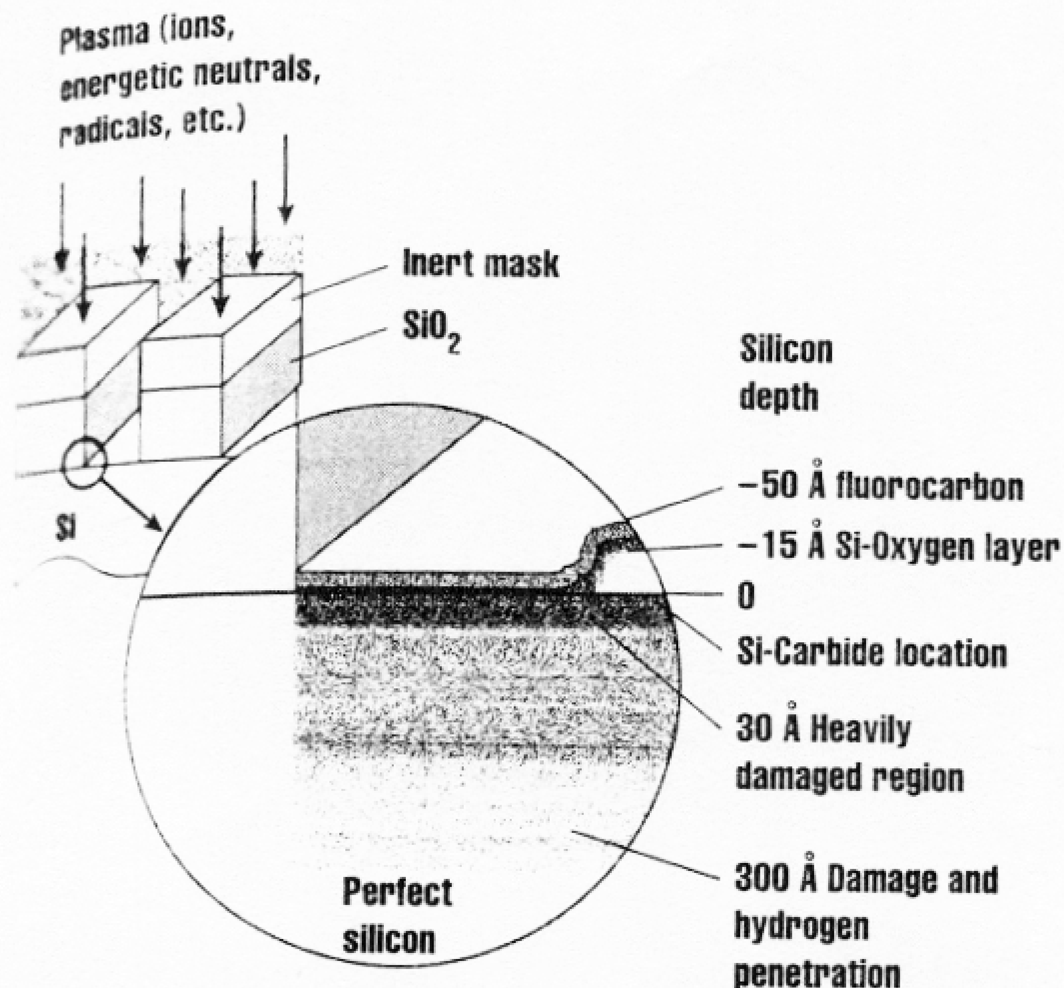


Figure 11-20 A cross section schematic of the results of a typical etch of SiO_2 down to Si using CF_4/H_2 *(after Oehrlein, Rembetski, and Payne, reprinted by permission, AIP).*

Relationship between Plasma Etching and RIE

- Pressure higher for Plasma, above 100 mTorr
- RIE voltage, excitation and directionality higher

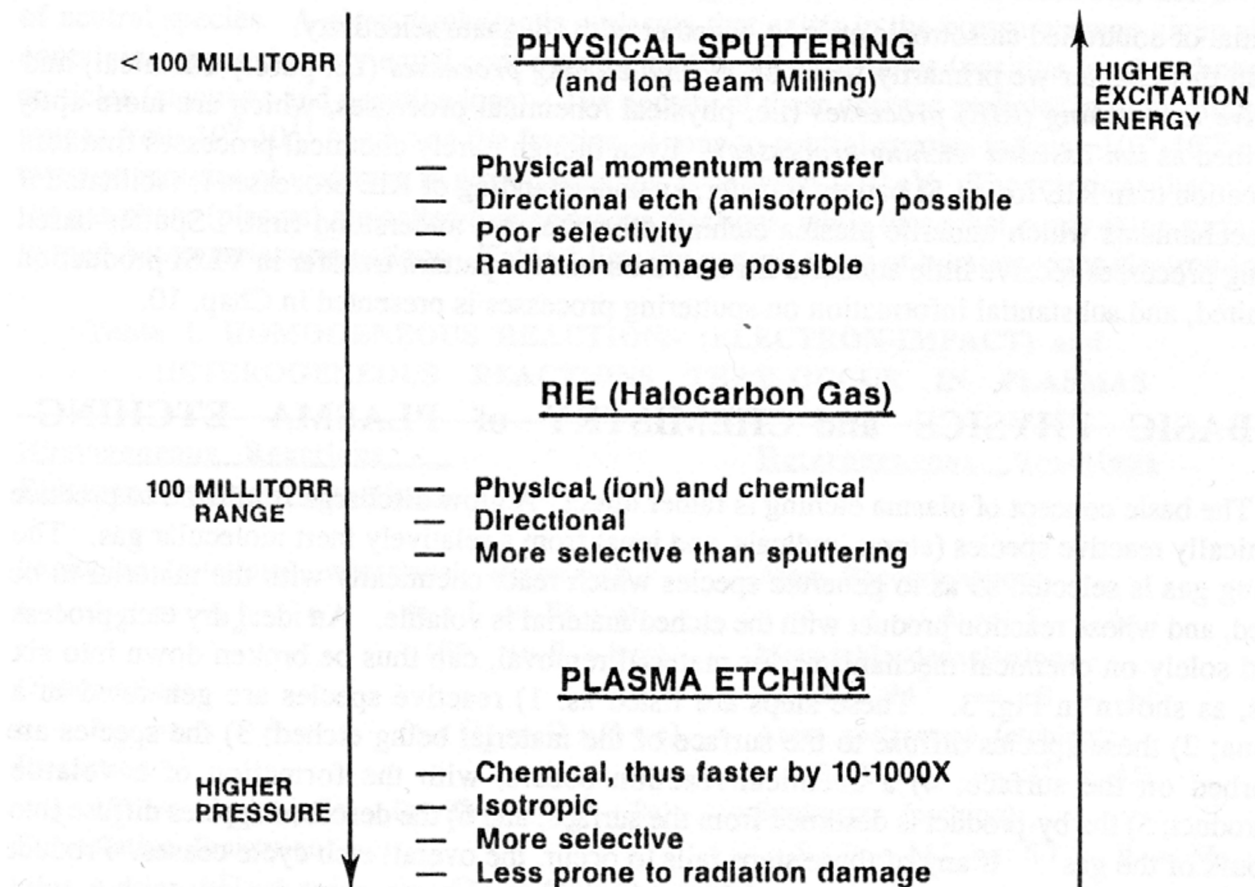


Fig. 2 The dry-etching spectrum.

Variables in Plasma Etching/RIE

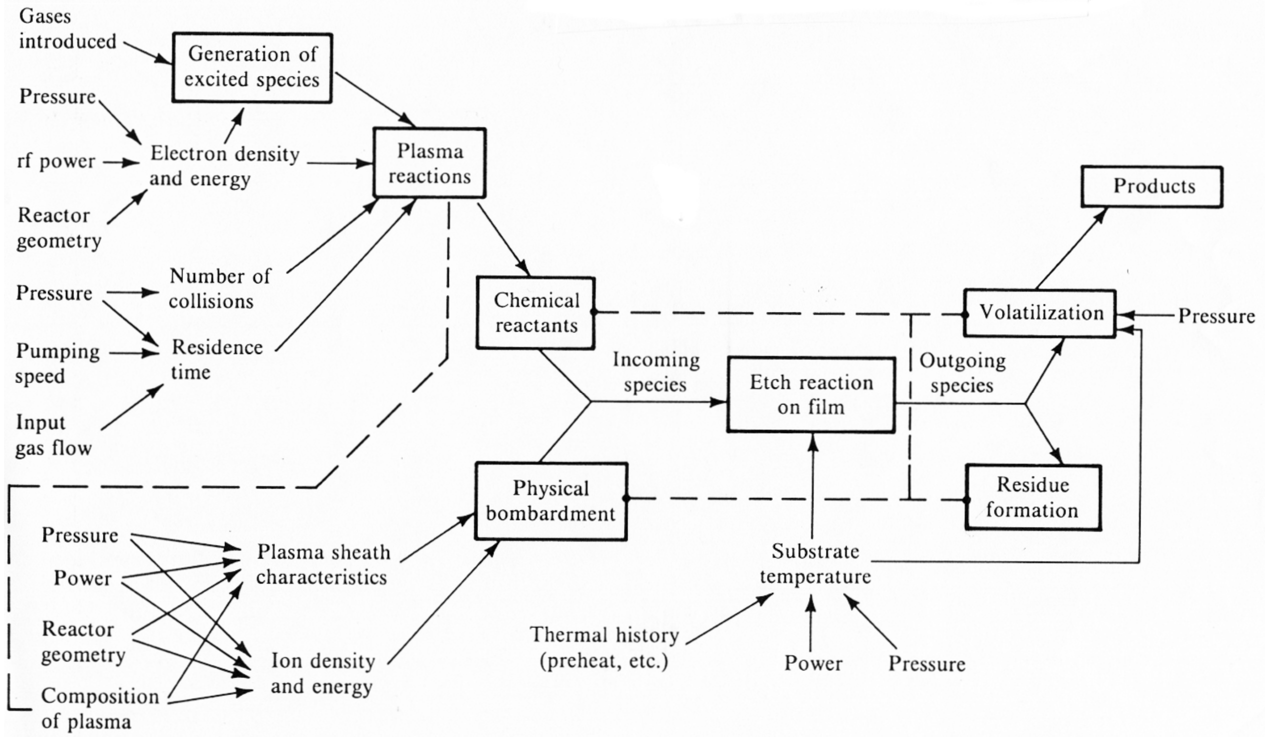
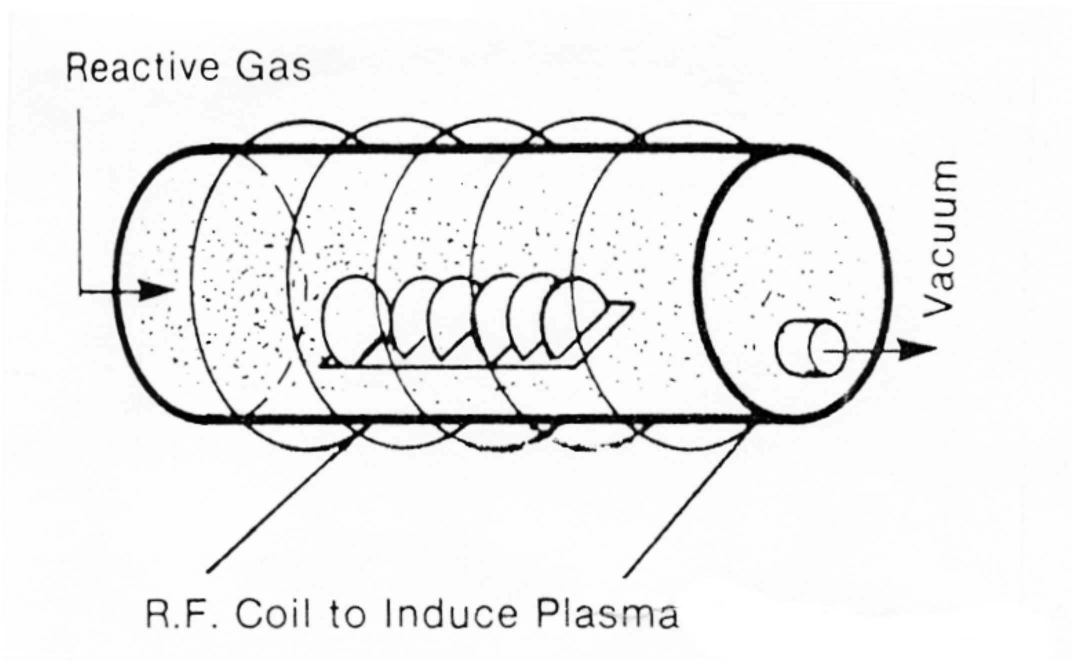


Figure 6-12 Interaction of variables affecting plasma etching.

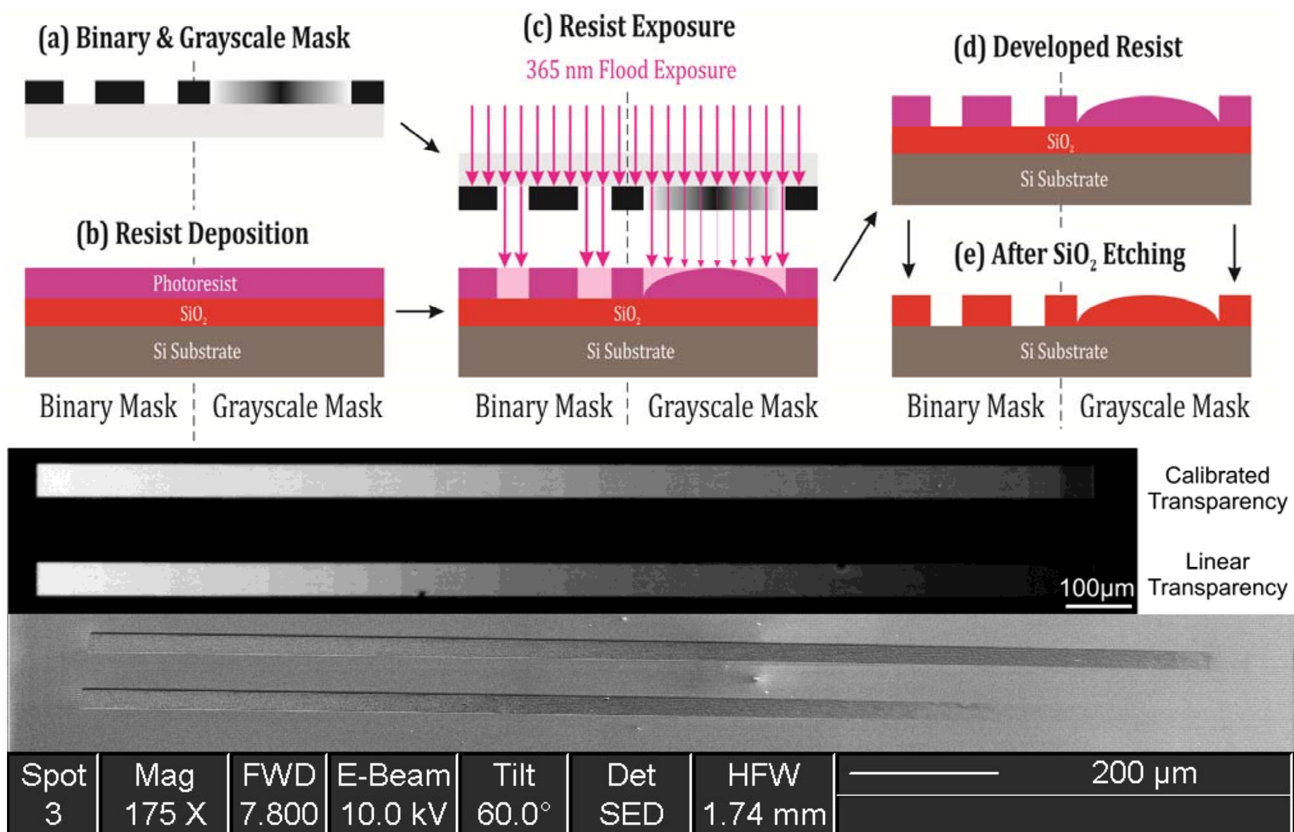
Photoresist Stripping Oxygen Barrel Reactors

- Photoresist often hard to remove with organic strippers
- Use Barrel reactors use RF excited O plasma for resist stripping
- Plasma destroys organics - called Ashing
- Problem: if resist is damaged eg implant resist may not strip
- May leave residue that is very hard to chemically strip



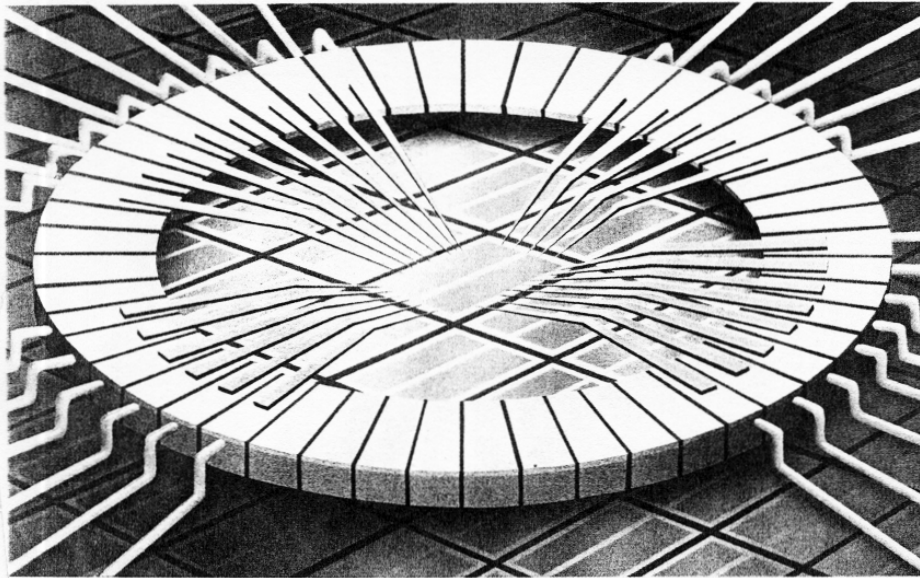
Micro-optics and 3D MEMS

- Resist thickness is a function of exposure after development
- Regular masks are Binary: fully absorbing or transmitting (B&W)
- Grayscale mask is like photograph: many transmitting levels
- If use a grayscale mask then create 3D shaped resist structure
- Then add Oxygen to plasma etch
- Oxygen erodes resist at same rate as etch attacks film
- Result transfer 3D structure from resist into film
- Eg Micro-lens

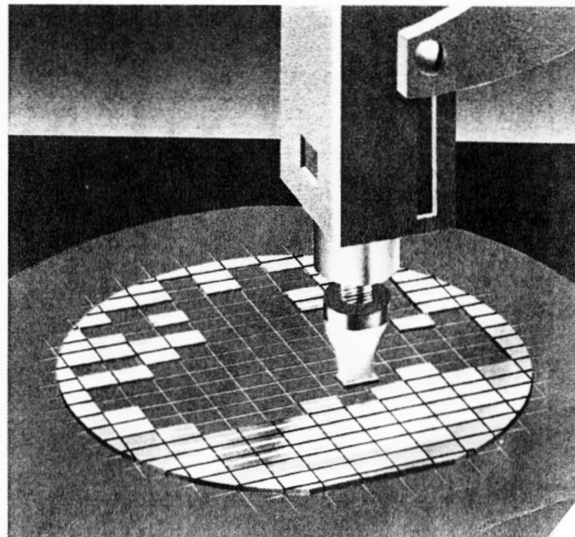


Post Fabrication Operations

- After fabrication die functionally tested
- Use an automatic prober
- Probe card puts needles on every pad
- Functional tester tests device with test vectors
- Difficult to test wafer at full speed
- Bad die marked (dot on waver)
- Wafer sawed up & die separated



Probing for flaws. A finished wafer, held on a chuck by suction, is inspected automatically. Probes reach out like tiny fingers from the test instrument that surrounds each chip in turn. Each probe, driven by a computer that feeds signals and records responses, touches a different contact pad on the chip. The rainbow colors are an optical effect created by light refracted by the thin "passivation" layer of silicon dioxide—glass—that coats each chip.



Extracting the good ones. A die picker uses suction to lift only the good chips from the wafer. The machine is guided in its selections by the computer, which uses the wafer map *(far left)* generated by the testing sequence.

Basic Yield Models

- Wafers have an average defect λ density/area
- Yield is number of chips that work
- Yield 3% on early runs, 80-90% mature runs
- Wafer production cost does not vary with yield
- Typical production costs
  - $1000 per wafer (1 micon 2 metal CMOS)
  - $3500 per wafer (45nm 5 metal CMOS)
- But yield determines profit from run
- Initial new complex design may get only 1 chip /wafer
- Often price device at the initial yield
- As yield increase profit increase as production cost fixed
- eg Current Max speed core i7 ~$1100 yield 2-3 per wafer

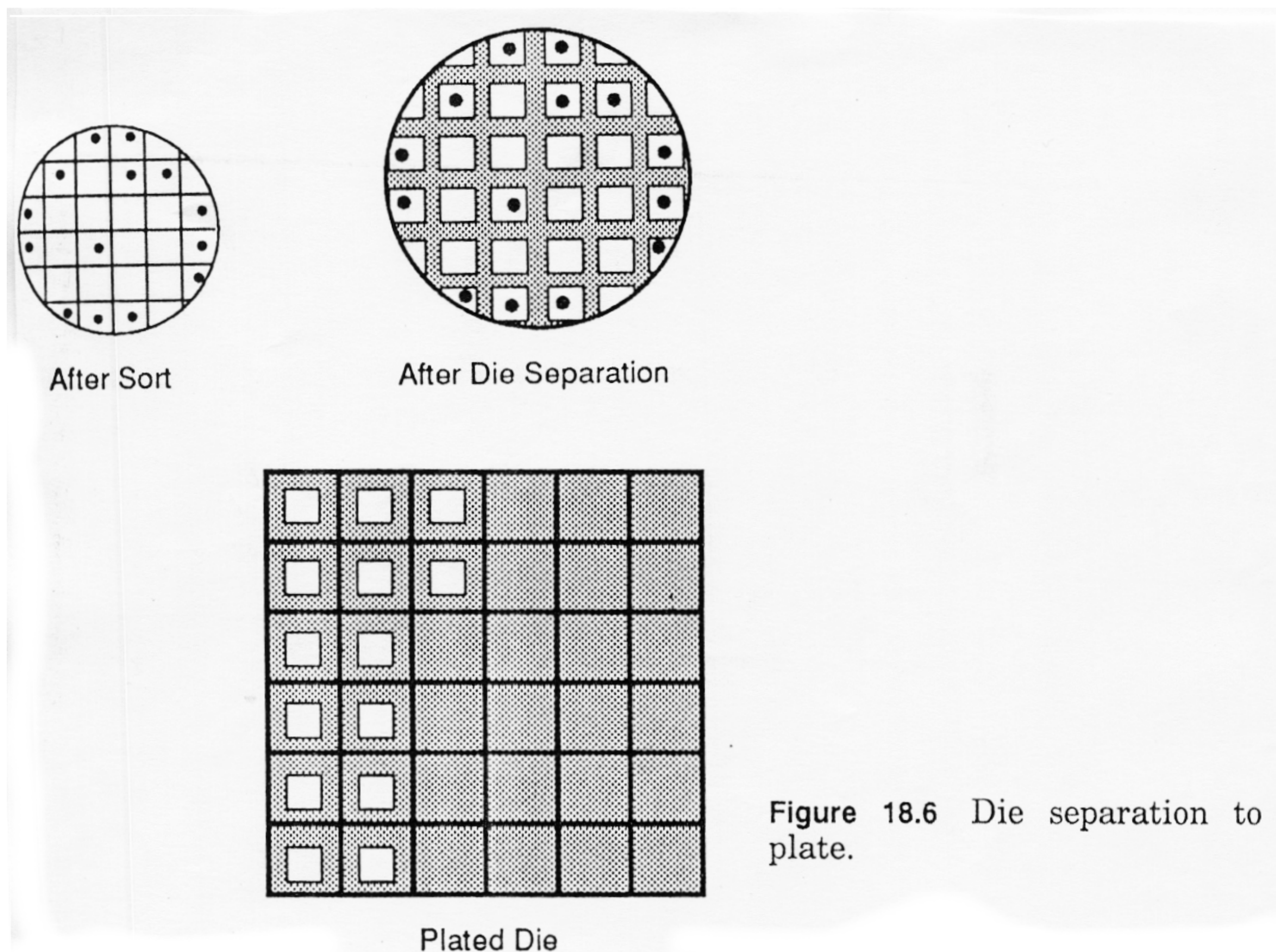


Figure 18.6 Die separation to plate.

Simple Yield modeling

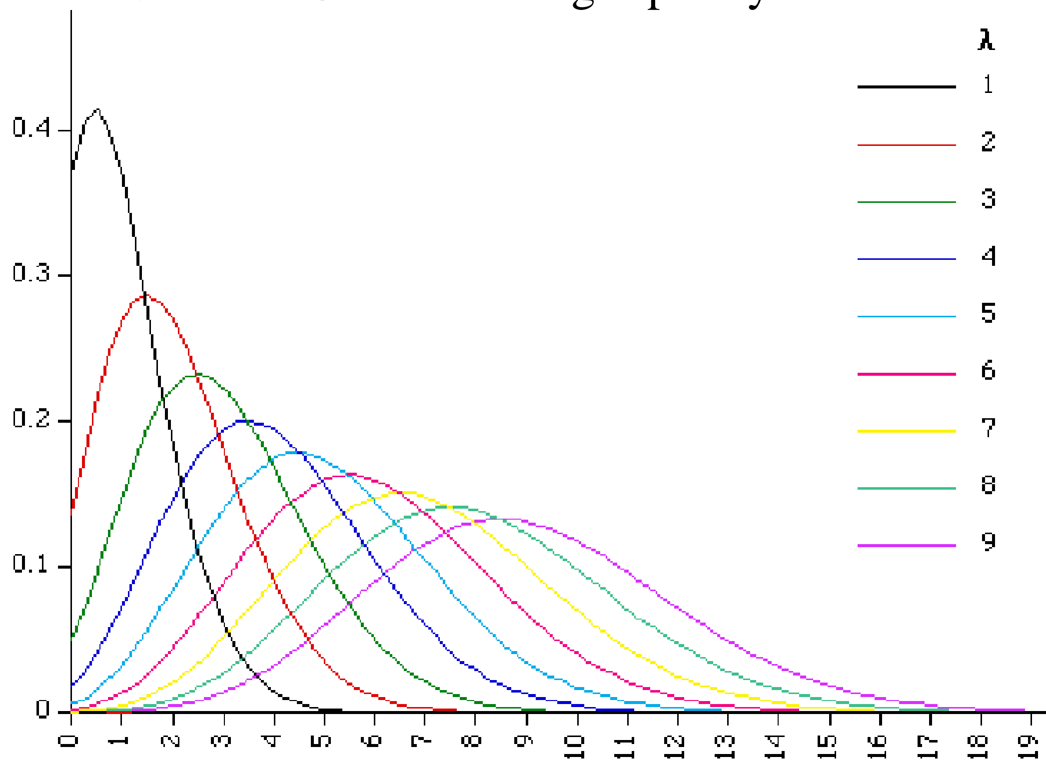
- Generally assume only point defects
- ie single small defect point destroying a single transistor/line
- Map defect distribution at probe time.
- Simple model assumes Poisson Distribution of x defects/die
- Yield of x = 0 defects (ie working device) for chip area S is

$$Y(0,S) = exp(-\lambda S)$$

- λ = defects per area (cm^2)
- Yield is always less than 1
- Note yield drops rapidly as chip area increases
- Eg if area S doubles then yield decreases by square

$$Y(0,2S) = exp(-\lambda 2S) = [exp(-\lambda S)]^2 = Y(0,S)^2$$

- eg: Y(0,S) = 0.5, Y(0,2S)=0.25 ie now 75% of wafer fails
- But some chips have more than one defect
- Yield not that simple often
- Process unevenness: Center and edges poor yield



Clustering of Defects

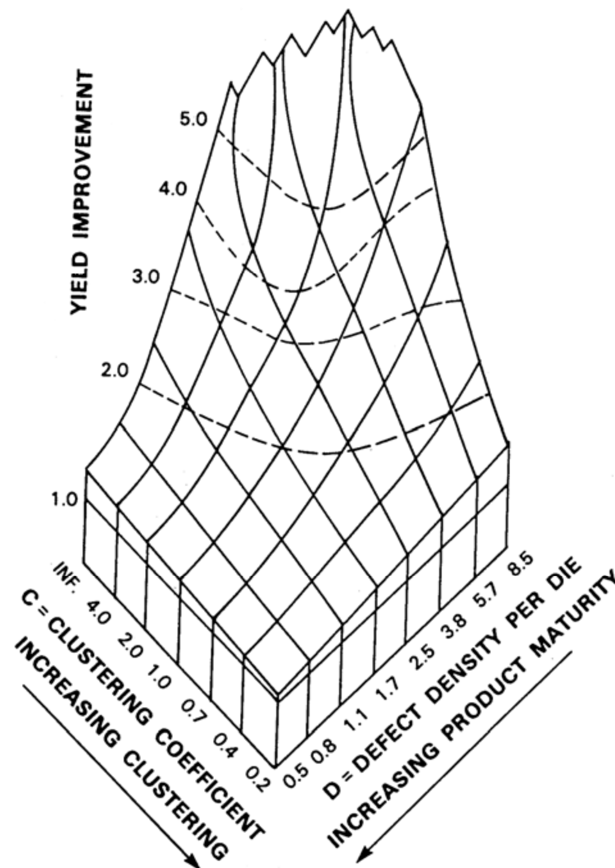
- Get clustering of defects - defects tend to be close together
- Why: simple statistics creates clusters of defects
- Also what causes one defect tends to causes others
- Studies show this follows a different distribution
- Result is Negative Binomial Distribution probability

$$P(x,S) = \frac{\Gamma(x+\alpha_c)}{x!\,\Gamma(\alpha_c)} \frac{\left(\frac{\lambda}{\alpha_c}\right)^{x}}{\left(1+\frac{\lambda}{\alpha_c}\right)^{x+\alpha_c}}$$

Where P = probability of x defects per area S,

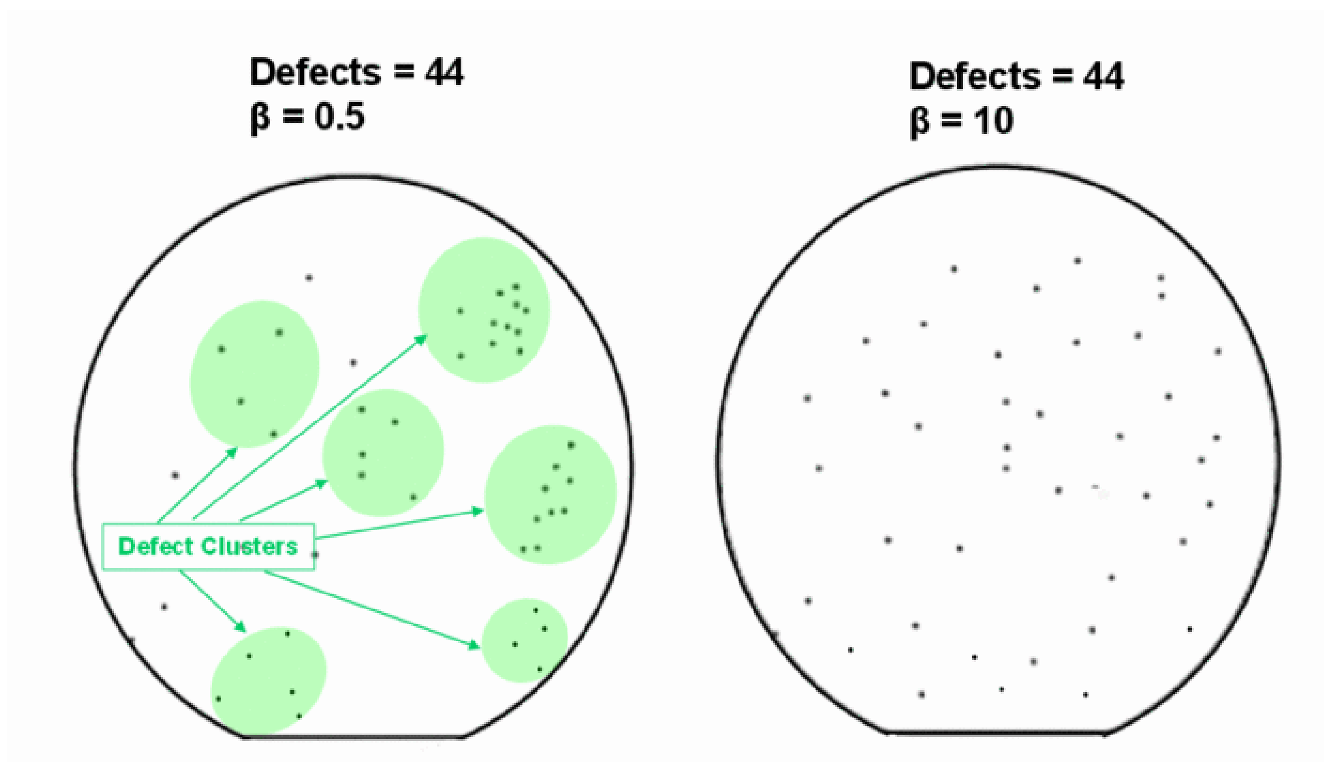
λ = defect density per chip

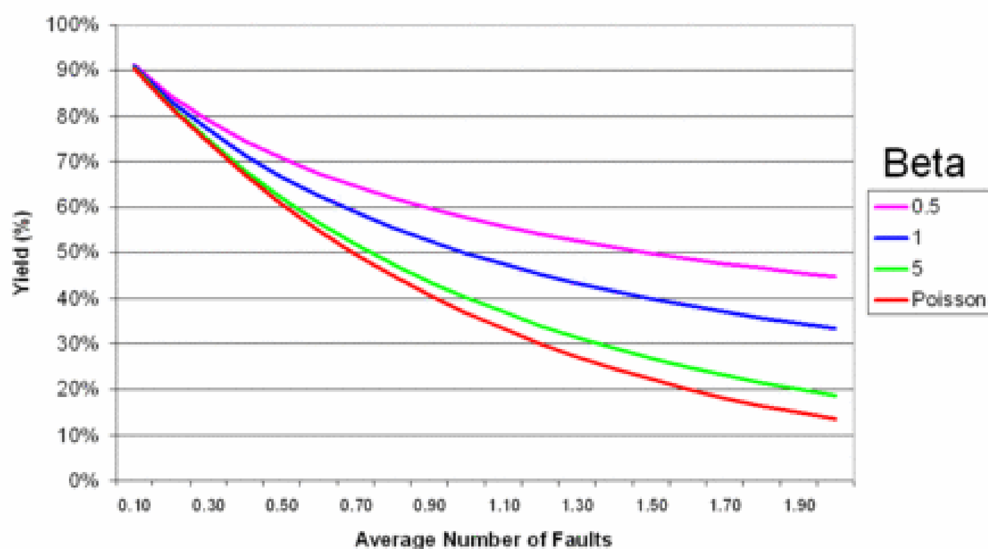
α_c = the cluster coefficient.



Clustering of Defects

- Cluster coefficients start at infinity random Poisson distribution
- $\alpha_c = 1$ is moderate clustering
- $\alpha_c = 0.1$ means most defects near each other
- This gives higher yields for more clustering
- Reason: some chips have many defects
- Leaves more with no defects at given defect density/area





Determining Yield Problems

- Use chip and test devices
- Use chip electrical test for some defect identification
  But difficult to isolate that way
- Visual inspection of defect areas also
- Most wafers have test chips on them
- Check yield of test devices: inserted on wafer
- Typical test devices
- sheet resistance all metals, poly, diffusions
- Via and contact chains:
  checks connections one level to another
- Step coverage devices: conductors over steps
- level to level isolation
- CV diodes to measure threshold
- Transistors characteristics
- Ring Oscillators (chains of odd number of inverters)

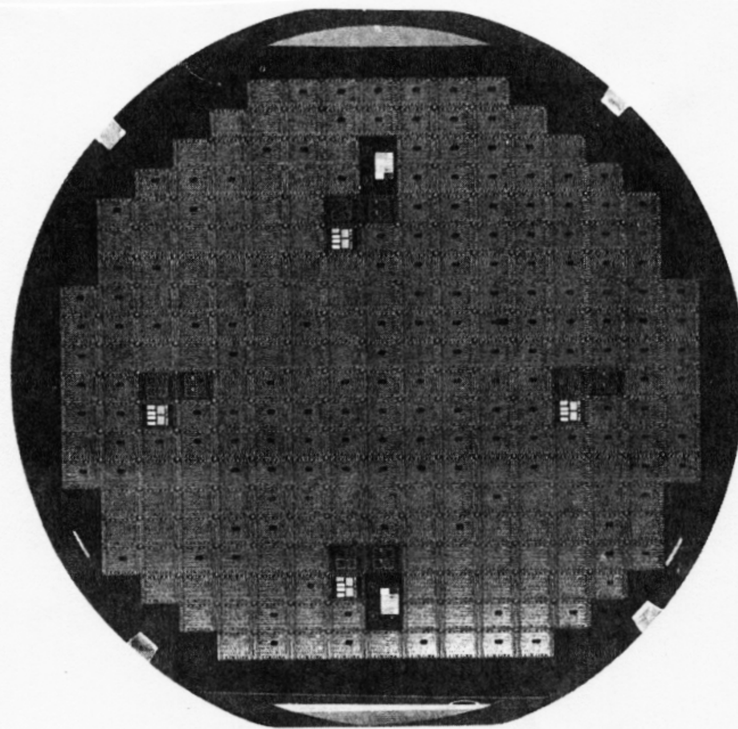
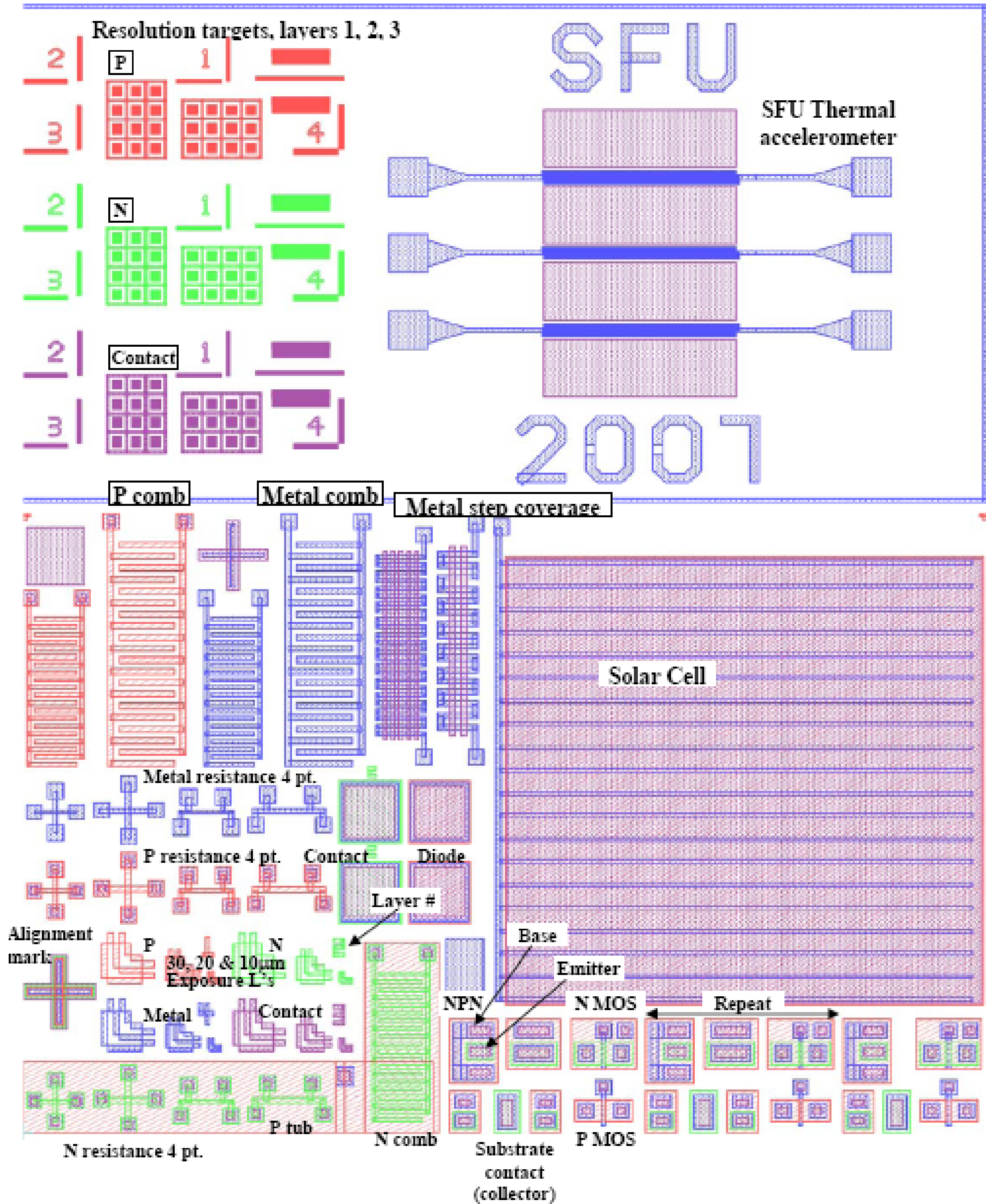


FIGURE 1
Photograph of an IC wafer showing regions of high and low yield. The chips with a black ink dab are bad. The unique-looking chips in the four groups are test chips.

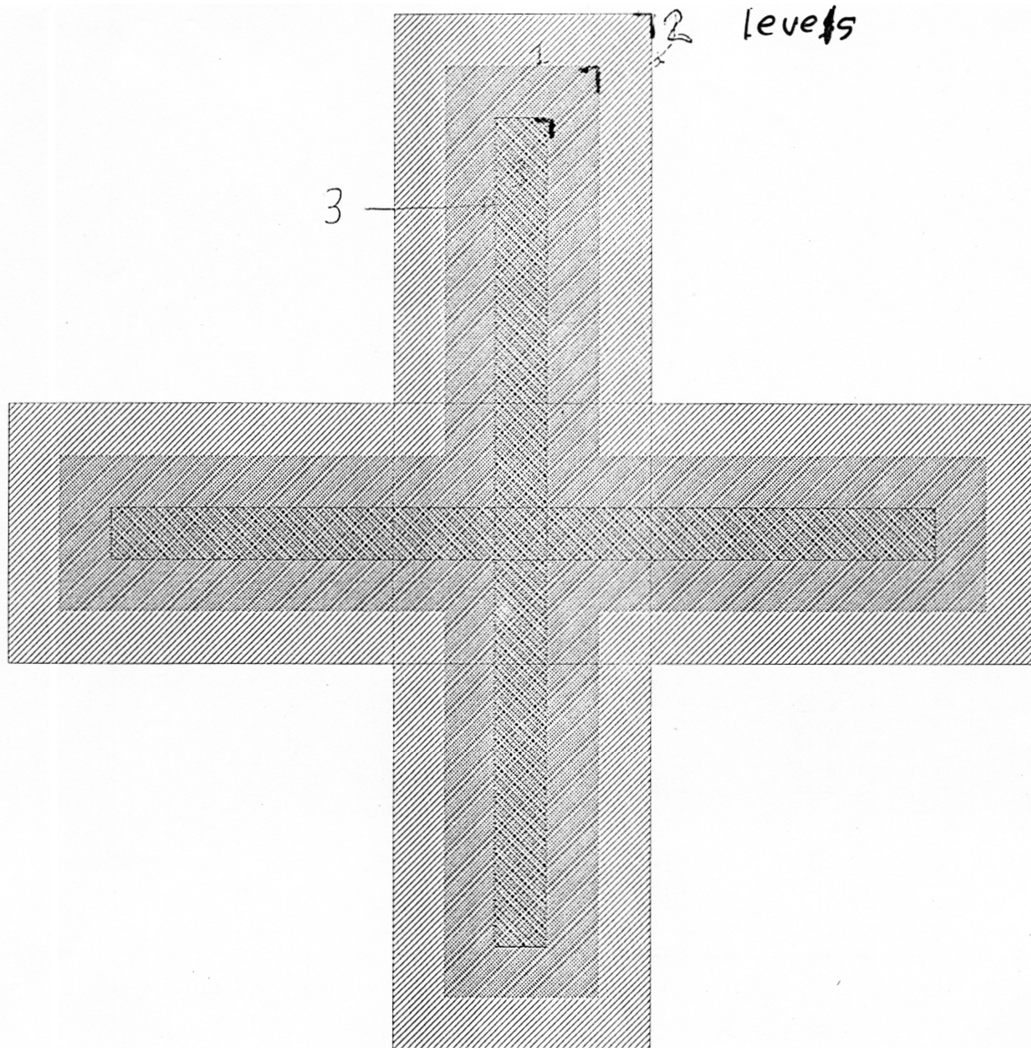
Test Structures on Wafers

- Wafers have areas of test structures
- Designed to characterize the process
- Lab wafer mostly test structures



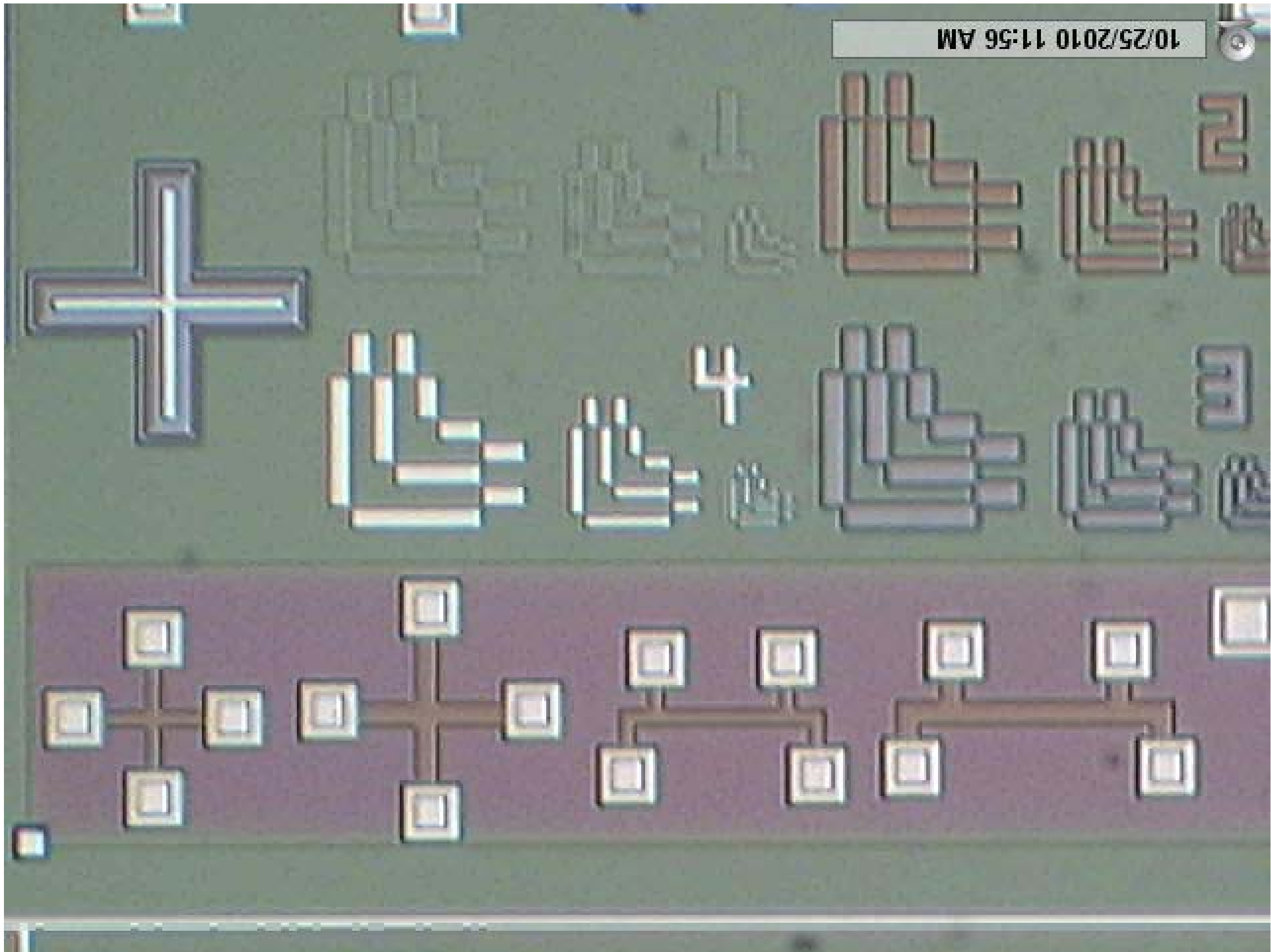
Alignment Cross Structure

- Note the nesting of light and dark field structures
- Often change alignment structures when reach too may levels otherwise grows to large
- Always align relative to critical level (usually first level)



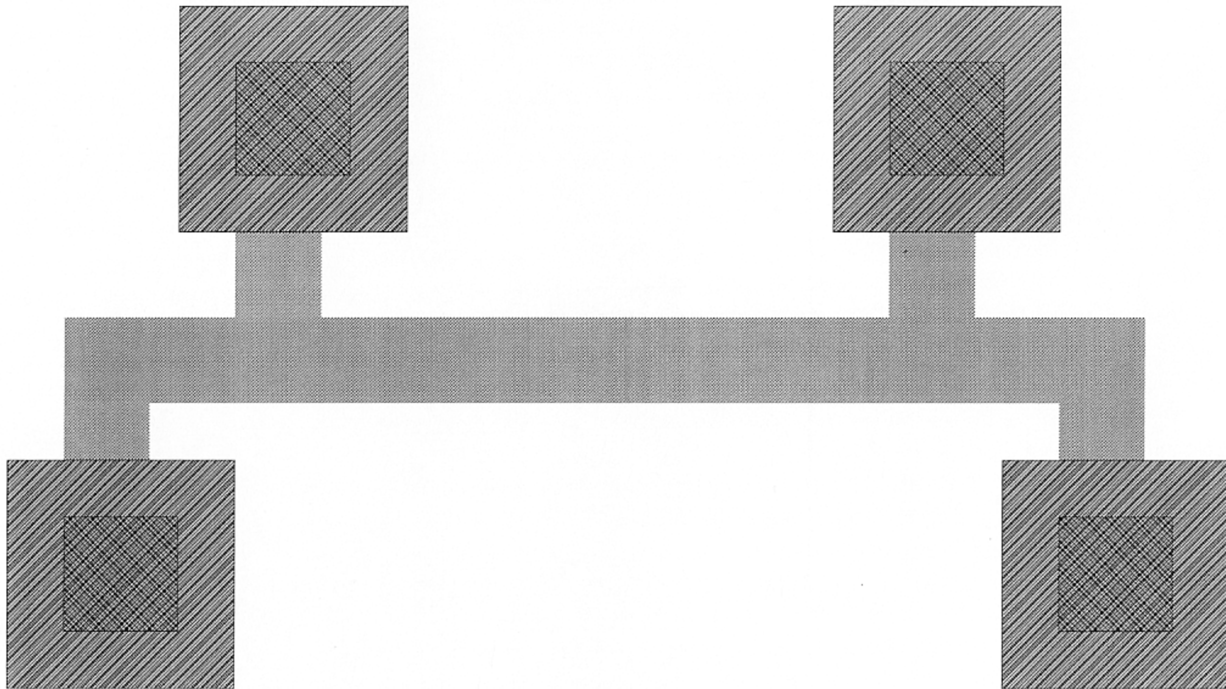
Alignment Cross Structure Pictures

- Alignment structure is near L level structures



Kalvin 4 Point Probs

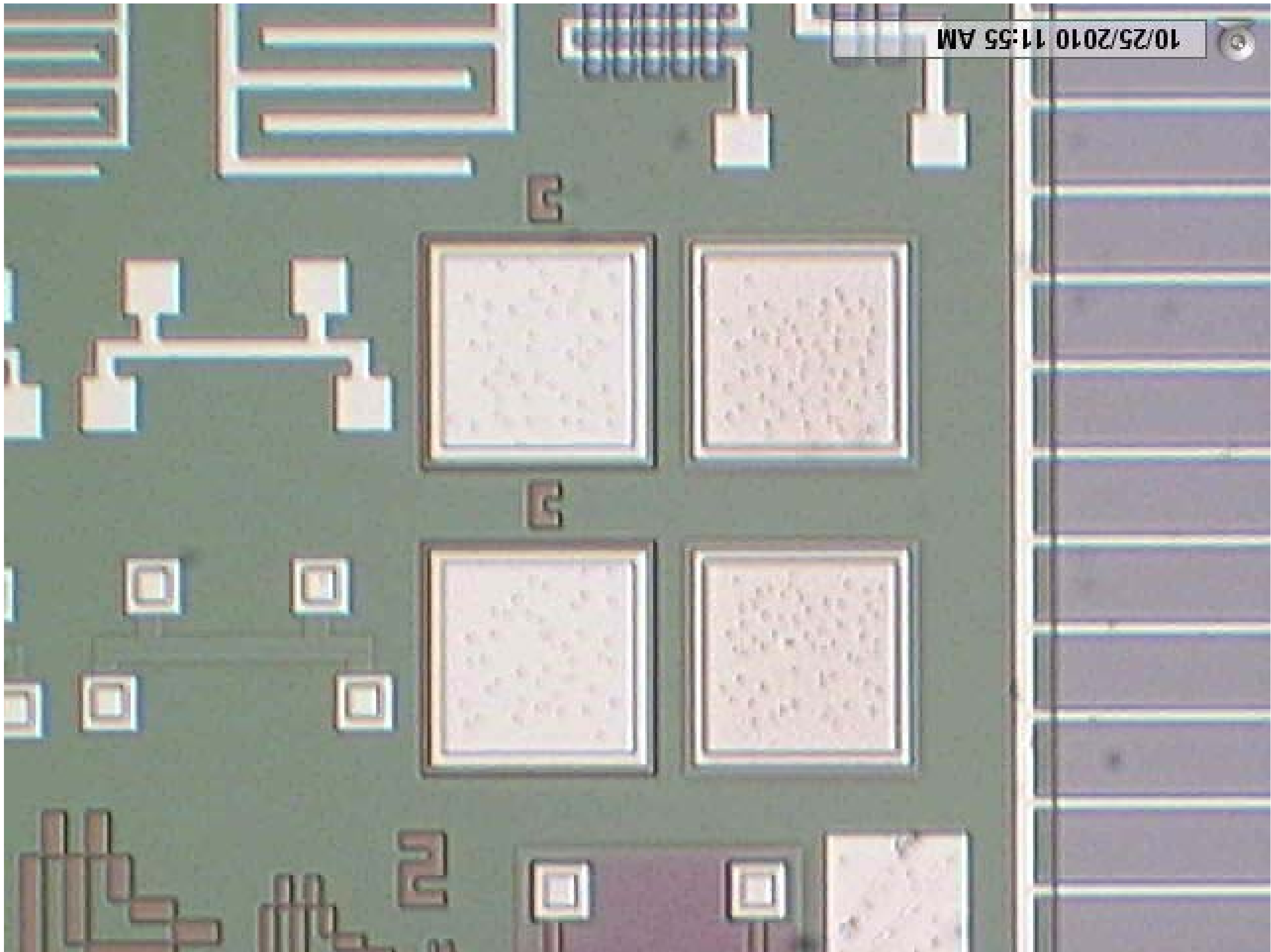
- Used to measure sheet resistance for all layers
- Outer two inject current
- Inner two voltage
- Lab ones have 7 squares in size



Kelvin sheet resistance

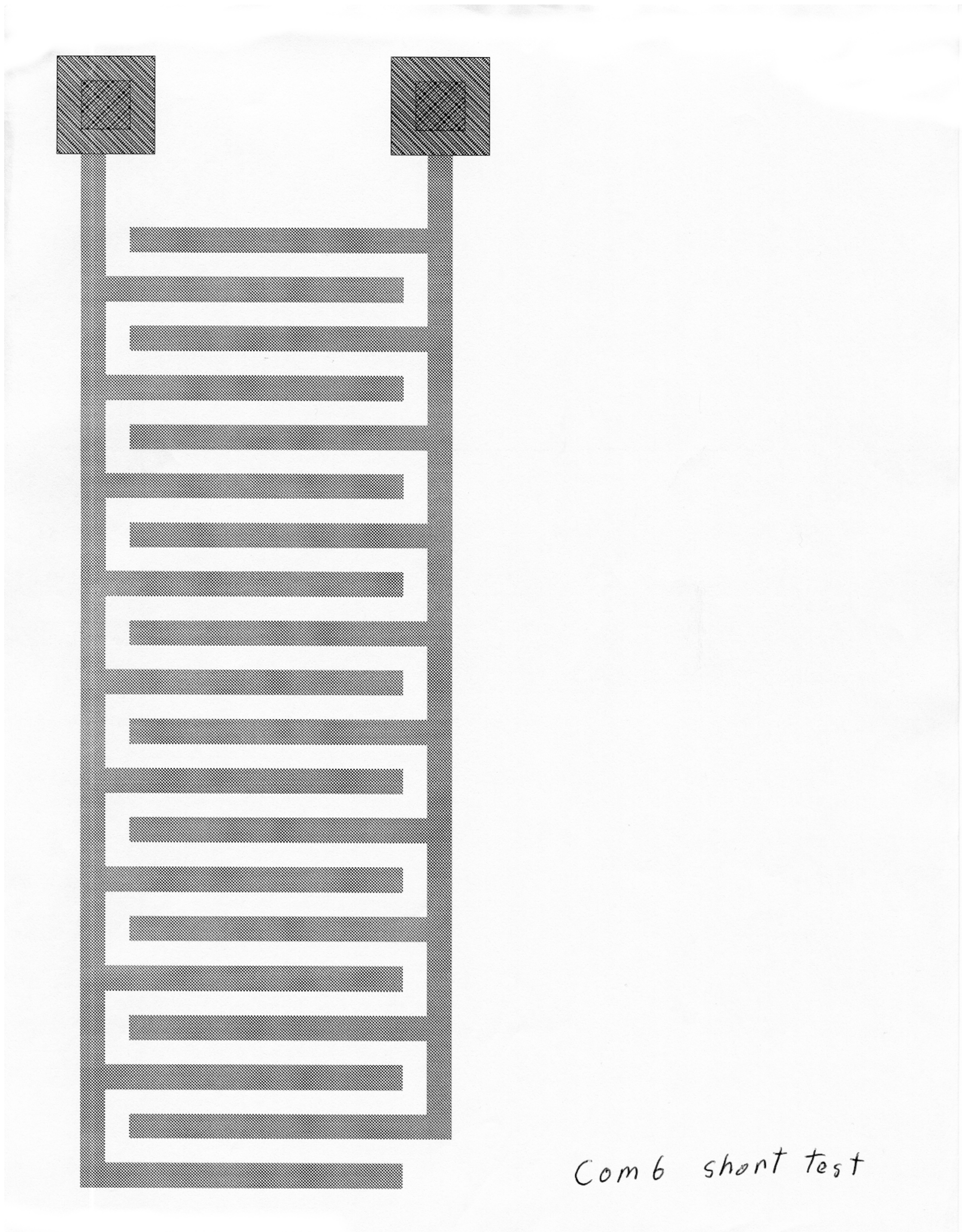
Kalvin 4 Point Probs

- Aluminum, N and P Kalvin located near contacts & solar cell



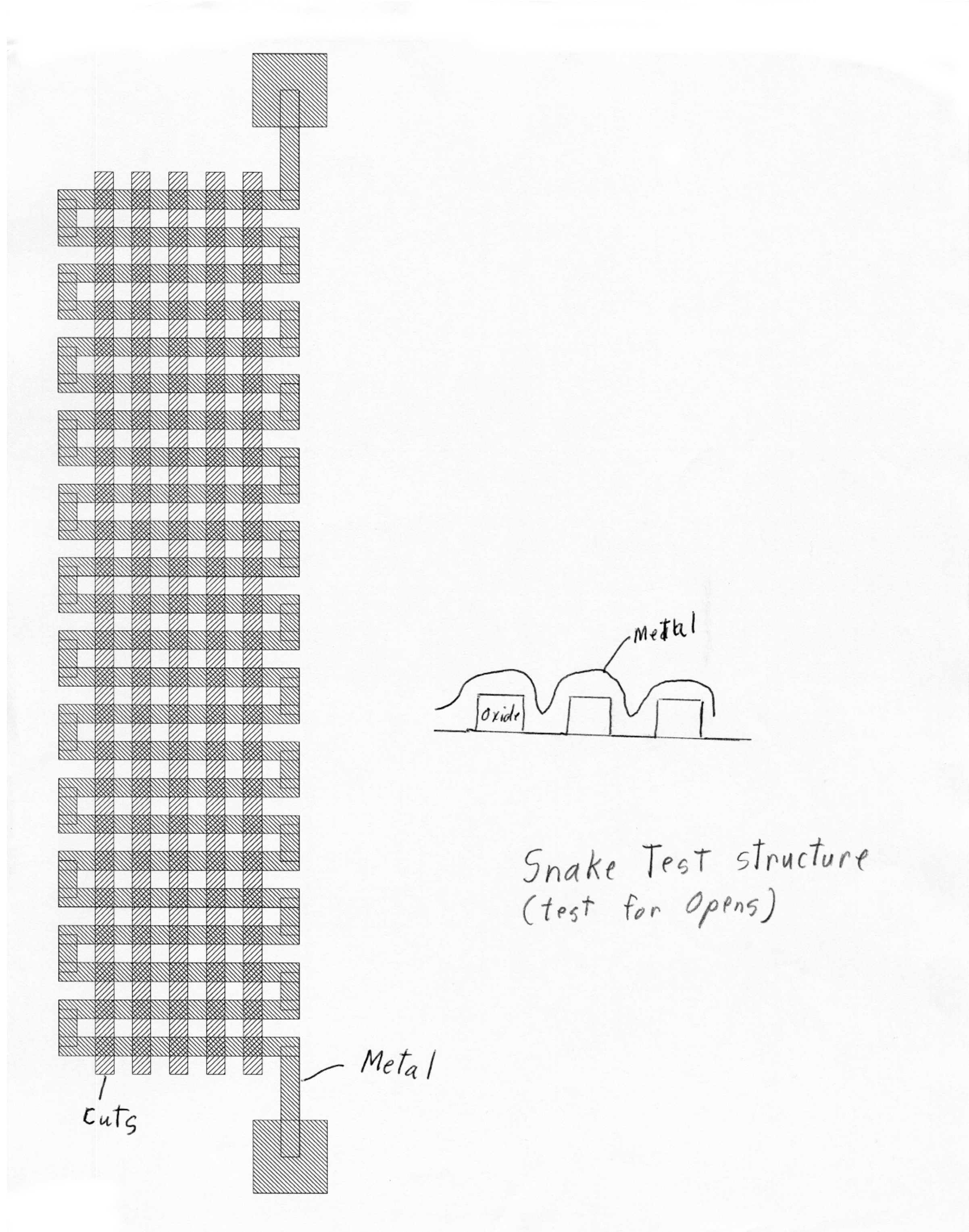
InterDigitated Combs

- Test for shorts between 2 sides of same level at minimum spacing



Line Snakes over Etched Groves

- Check for breaks as steps over etchs/structures (ie when open)
- Also shorts due to conductor along edges (ie low resistance)

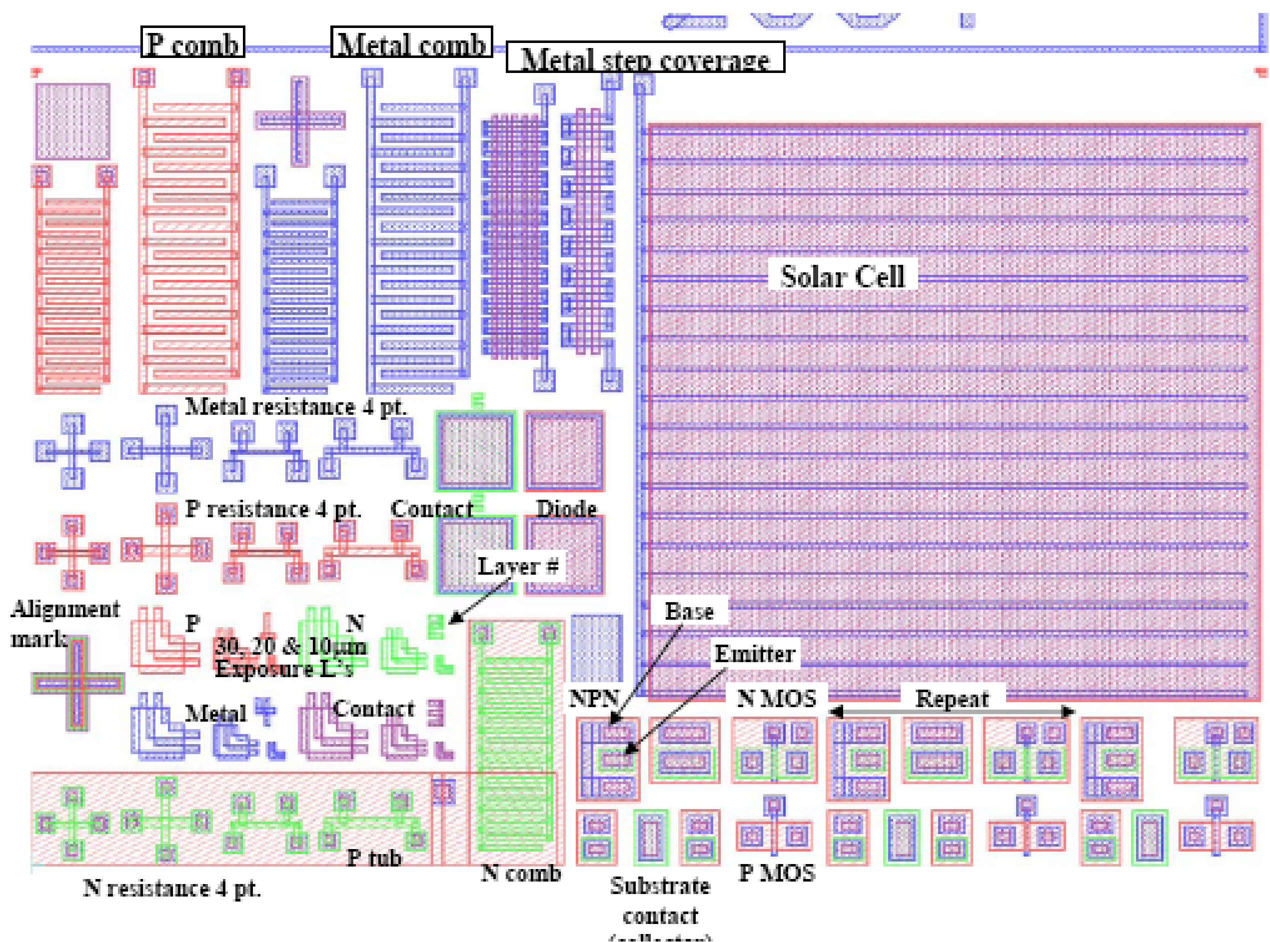


InterDigitated Combs

- Combs and Snakes above 4 point

Other Common Tests

- CV measurements of oxide
- Diode characteristics: turn on voltage, reverse current, breakdown voltage, forward resistance
- MOS Transistor Characteristics: Threshold voltage, impedance IV characteristics (transistor curves)
- Bipolar Transistors (if any): IV of BC, BE, EC & Transistor Curves and
- Via and contact cuts (via/contact resistance & opens)
- Ring oscillators: feed output of odd number of inverters into input
- Creates oscillator at max transistor speed.



Wafer Scribing and Cutting

- Wafer coated to protect die
- Oldest method: diamond tip scribe along d planes
  bend wafer and snap on planes: loss of die
- Diamond saw cuts in channels
  problem: chips from cut can damage die
- Laser beam cutting: newest
  less damage, but more expensive at present

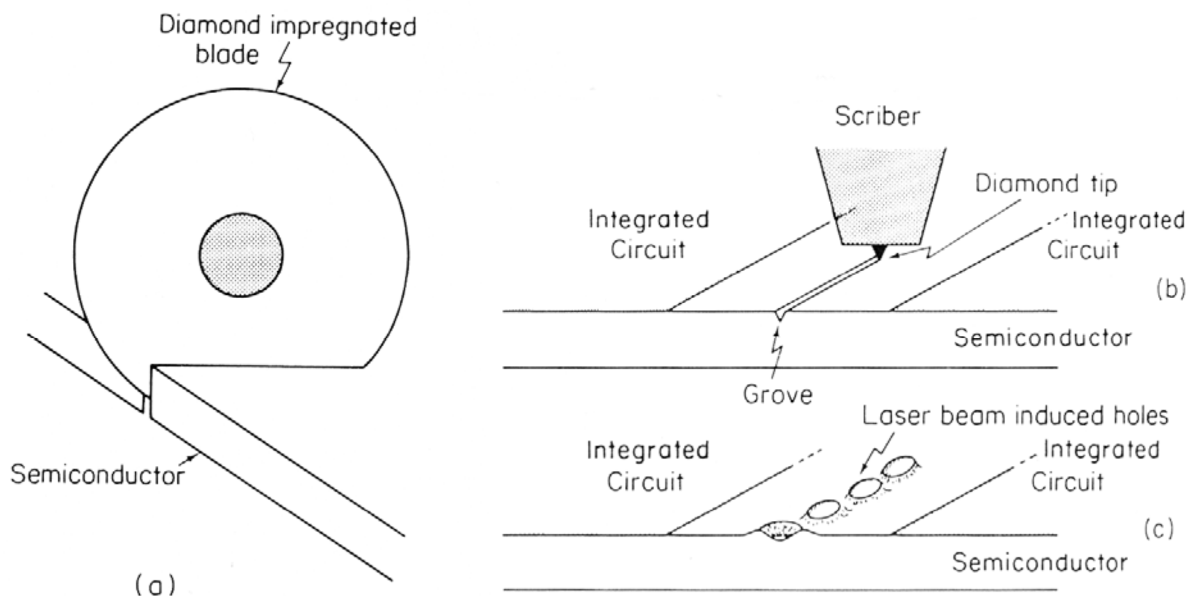
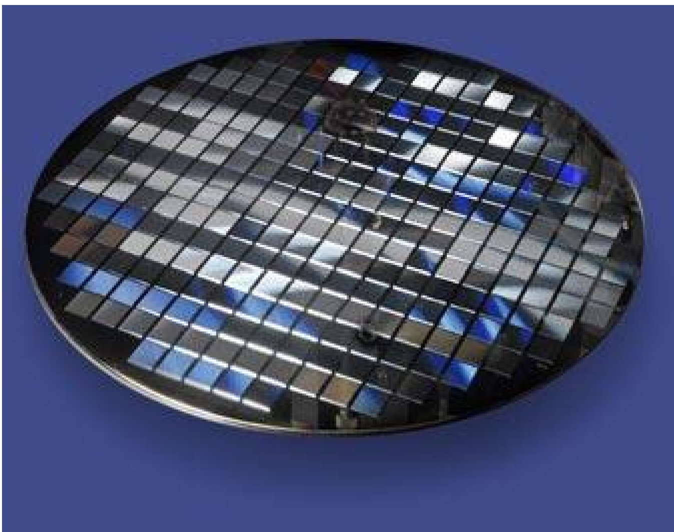
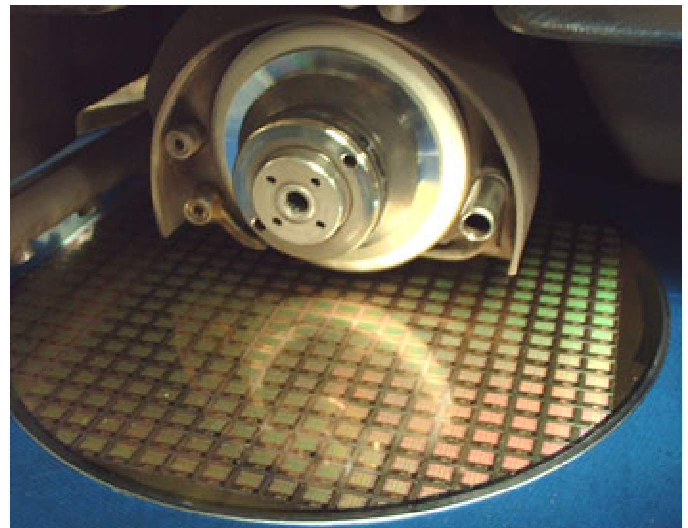


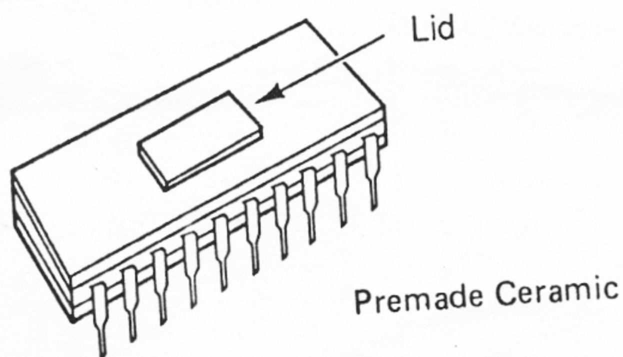
Fig. 6.10 Dicing of ICs: (a) diamond saw; (b) diamond scribe; (c) laser scribing

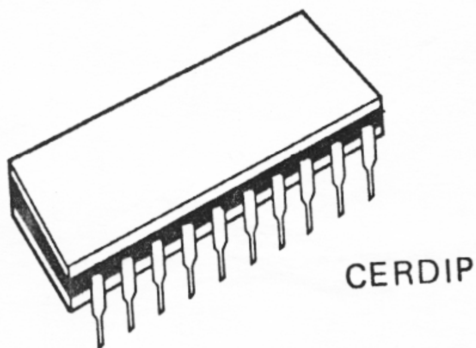




Packaging Chips

- DIP: Dual Inline Pin: up to 64 pins now
- More complex devices mean more complex packages
- Most expensive: Ceramic package with cover
  used in test samples, small runs
- Sealed ceramic: best for high power
- Molded Plastic: low cost, lower power





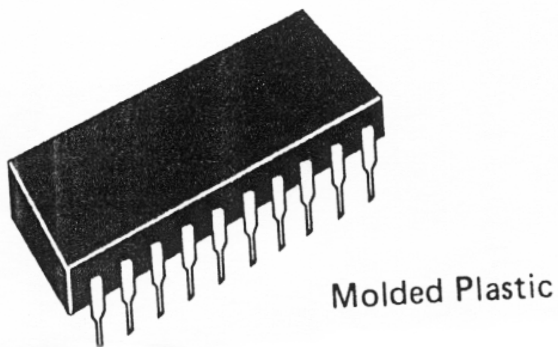
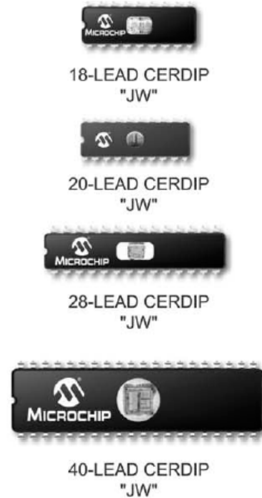


Figure 18.17 DIP packages.

High Pin Count and Density Packages

- Dips moved into Quad packages: pins on 4 sides
- Pin Grid Arrays (PGA): matrix of pins
- Surface mount: put directly on PC board & flip chip

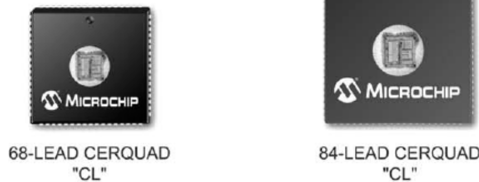
CERAMIC DUAL IN-LINE
CERDIP



PLASTIC DUAL IN-LINE
PDIP

PLASTIC LEADED
CHIP CARRIER
PLCC

CERAMIC CHIP CARRIER
CERQUAD



PLASTIC QUAD
FLATPACK
"QFP"

PACKAGES ARE APPROXIMATE SIZE