Exposures from Mask Aligner into Resist

- Mask aligner images created by shadowing from mask into resist
- Soft contact and Proximity good for 3 micron structures
- Vacuum Hard Contact: no shadow effects at edge
- Can produce << 1 μm
- But gets mask dirty & damages resists so poor yield
- Size of mask structure & λ determines separation distance
- Smaller line, or shorter wavelength closer object
- Exposure time T and total intensity I gives the exposure energy

$$E = TI$$

- T in sec, I in W/cm^2 , E in J/cm^2

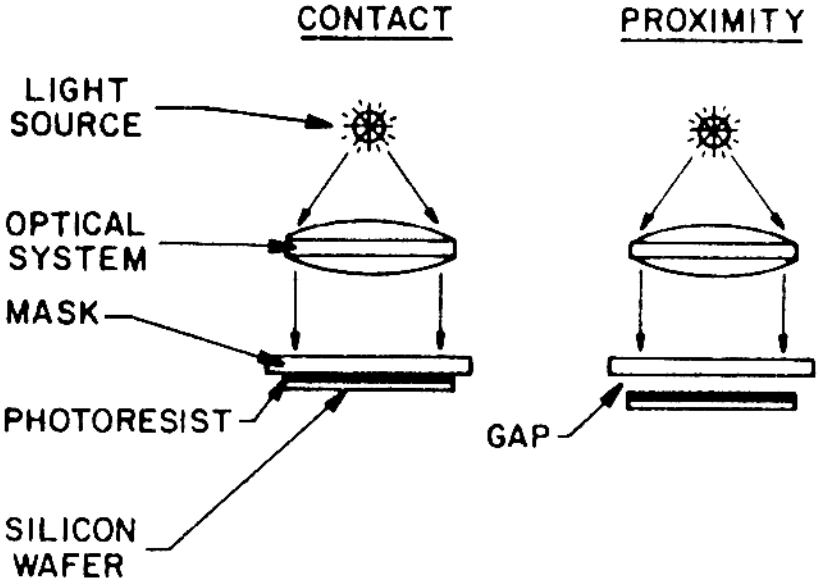


Table 7.4 Maximum allowable proximity gap for near and deep UV sources as a function of the feature size normalized to the gap required for 2.5 μm resolution with a deep UV source

Feature Size (μm)	Maximum Gap for Near UV Source	Maximum Gap for Deep UV Source
2.5	0.63	1.0
2.0	0.37	0.61
1.0	0.08	0.24
0.5	0.05	0.07

Data taken from Lin.

Aligner Exposure Near the Mask Structure Edges

- Proximity: diffraction & shadowing cause non abrupt exposure
- Diffraction causes shadow width to increase with separation
- Light changes gradually from zero to full intensity
- Causes a variation in line width after development
- Edge shadow spread creates partially exposed resist
- Resist development then creates slopped edges
- Hence resolution limitation ~2 micron on non contact aligner
- With contact alignment diffraction is almost nill

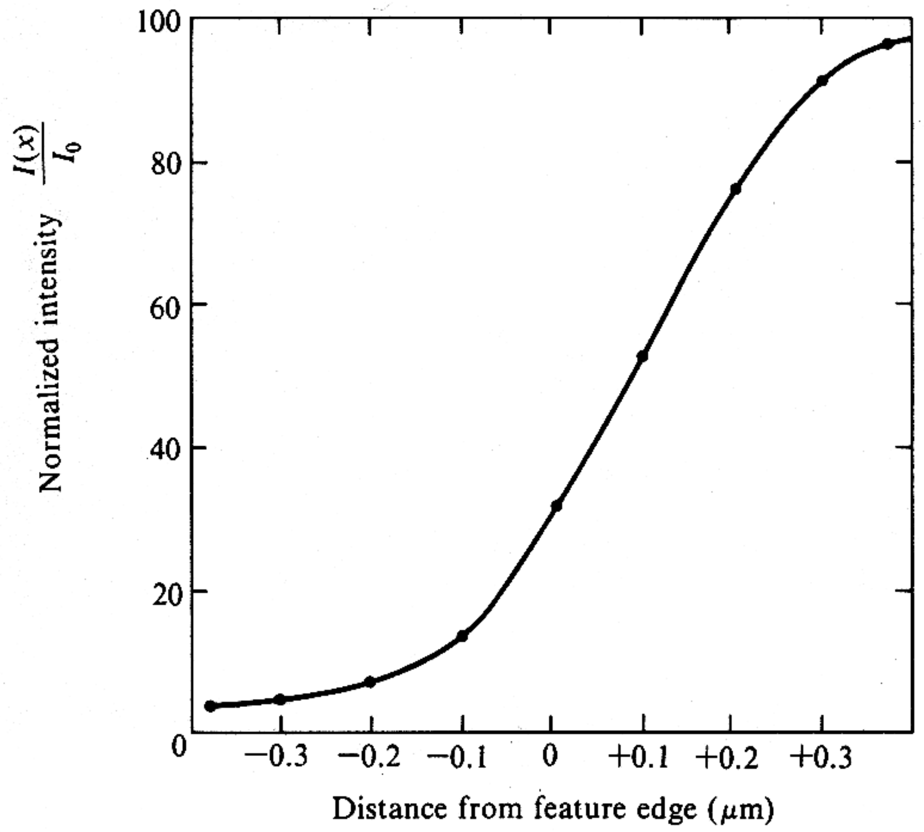


Figure 5-14 Light intensity near the image edge. The geometrical edge of this mask feature is at $x = 0$. N.A. = 0.42, λ = 436 nm, S = 0.7, linewidth = spacewidth = 0.75 μm. (*After Ref. 3. Reprinted with permission of* Solid State Technology, *published by Technical Publishing, a company of Dun & Bradstreet.*)

Contrast Curves and Resist

- What fraction of resist is removed for given exposure
- Define two exposure points (for positive resist)
- D_0 Energy (mJ/cm^2) threshold where resist just affected
- D_{100} Energy where resist full removed after exposure
- Get almost a straight line projection on semilog plot
- Contrast Gamma γ is the resulting slope

$$\gamma = \frac{1}{\log_{10}\left(\frac{D_{100}}{D_0}\right)}$$

- Typical contrast $\gamma = 2 - 3$ regular resists – now up to 10
- Higher Gamma sharper the slope edge
- Note: negative resist reverses terms: D_0 just affected: D_{100} solid
- Light absorbed by resist thickness T_R decreases by

$$A = \exp(-\alpha T_R)$$

- α is the optical absorption coefficient in cm^{-1}
- Thus the contrast becomes

$$\gamma = \frac{1}{\beta + \alpha T_R}$$

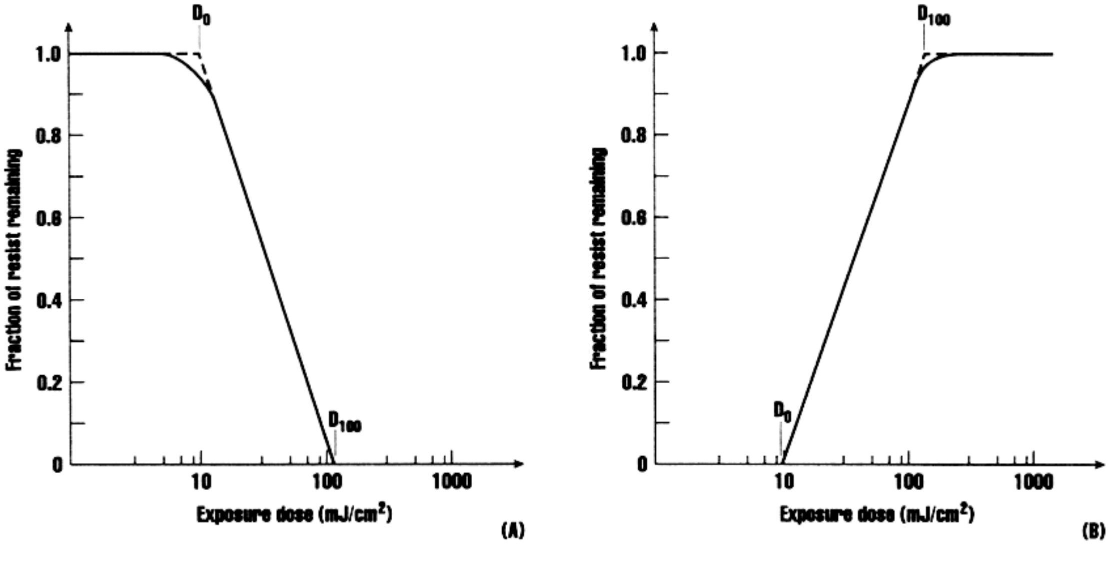


Figure 8-7 Contrast curves for idealized resists: (a) positive tone and (b) negative tone.

Critical Modulation Transfer Function

- Brightest to darkest part of exposure is
  Modulation Transfer Function (MTF):

$$MTF = \frac{I_{\max} - I_{\min}}{I_{\max} + I_{\min}}$$

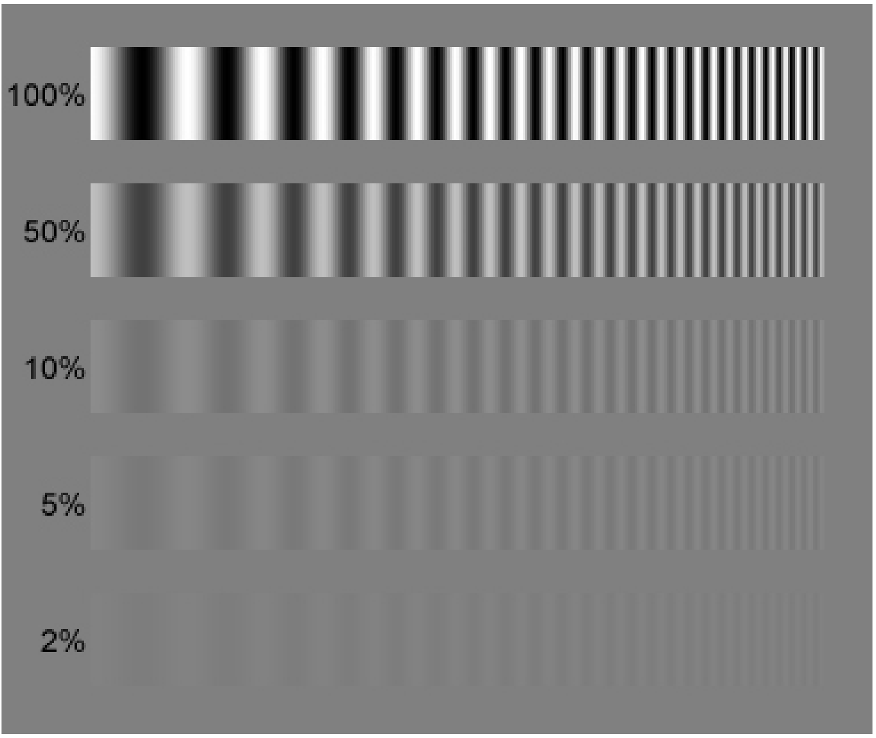
- For resist use Critical Modulation Transfer Function (CMTF)
- Minimum optical modulation needed to create pattern

$$CMTF = \frac{D_{100} - D_0}{D_{100} + D_0}$$

- Converting to using contrast ratio

$$CMTF = \frac{10^{1/\gamma} - 1}{10^{1/\gamma} + 1}$$

- Typical need CMTF at least 0.4
- MTF must exceed CMTF for successful exposure



MTF

Development Process

- Developing is a chemical process that removes the exposed resist
- Action on resist similar to solvent dissolving (etching) resist
- Development rate depends on the exposure level
- Negative resists use organic solvent to dissolve soft resist
- Unexposed removed, exposed polymerized resists solvent
- Positive resists use water based developers
- Developer removes exposed (softened) resist
- Unexposed resist lack the broken bonds – does not dissolve
- Developer Mixed (usually 1:1 with DI water)
- Simple method: dunk in tanks time: 30 - 60 sec.
- Agate while in the tank – changes development rate
- Brings in fresh developer and removes resist
- Can see resist dissolved in the developer
- Rinse in DI after Development
- Spin Dry

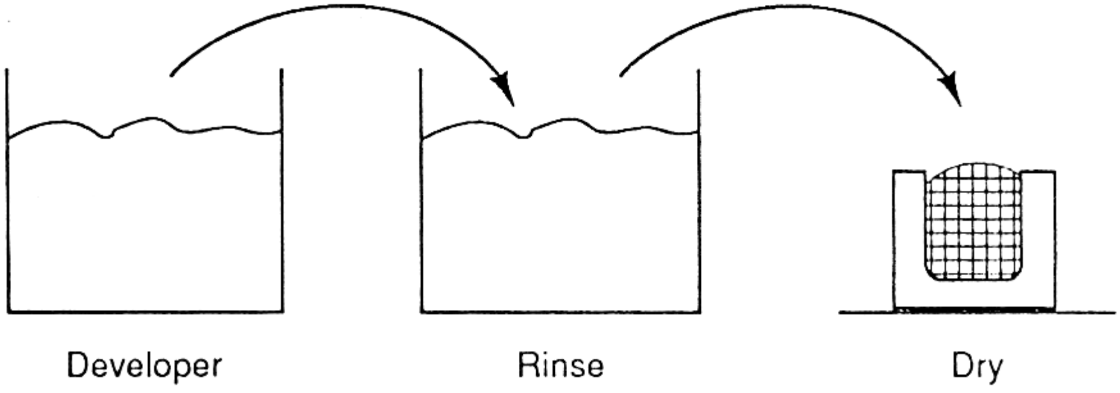


Figure 9.6 Immersion developer steps.

Wafer Track Development Systems

- Automatic development uses the spin coaters
- Several methods depending on developer/resist combination:
- Puddle developer
- Spin with spray to make even
- To finish high speed rinse and spin dry
- Often do hard bake as well on the wafer track system

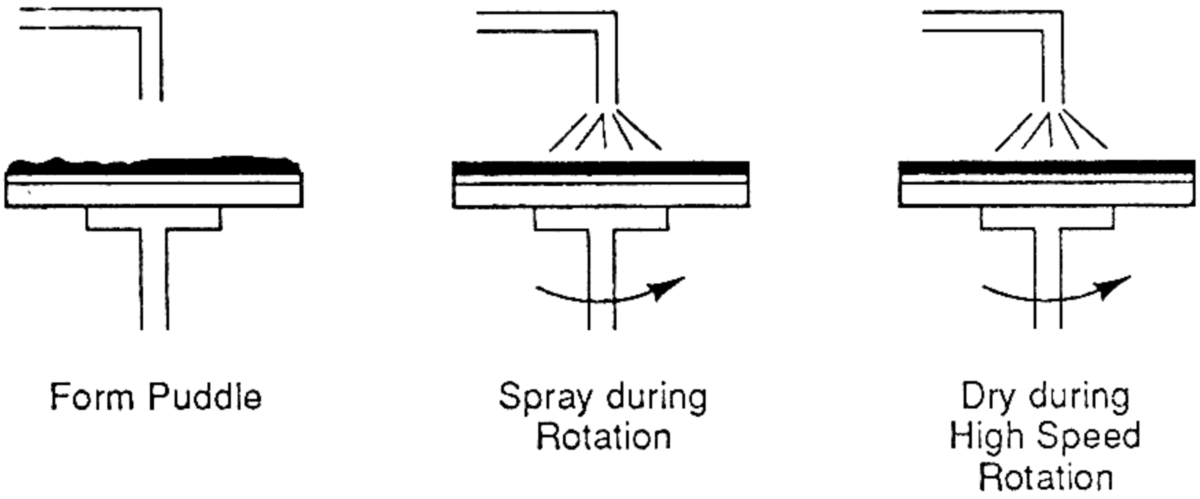


Figure 9.8 Puddle-spray development.

Photoresist Exposure/Development

- Development removal rate of resist is a function of exposure
- Unexposed resist removed (etched) at a low rate
  eg 0.2 nm/sec
- Exposed resist rate removal dependent on UV light level
- Higher intensity, faster removal
  eg. 75 mJ/cm^2 develops resist at 10 nm/sec
  eg. 150 mJ/cm^2 develops resist at 20 nm/sec
- Develop rate increases with temperature
- Rate increases with developer concentration
- As wafers developed dissolved resist slows development rate
- Hence fresh developer faster than used developer

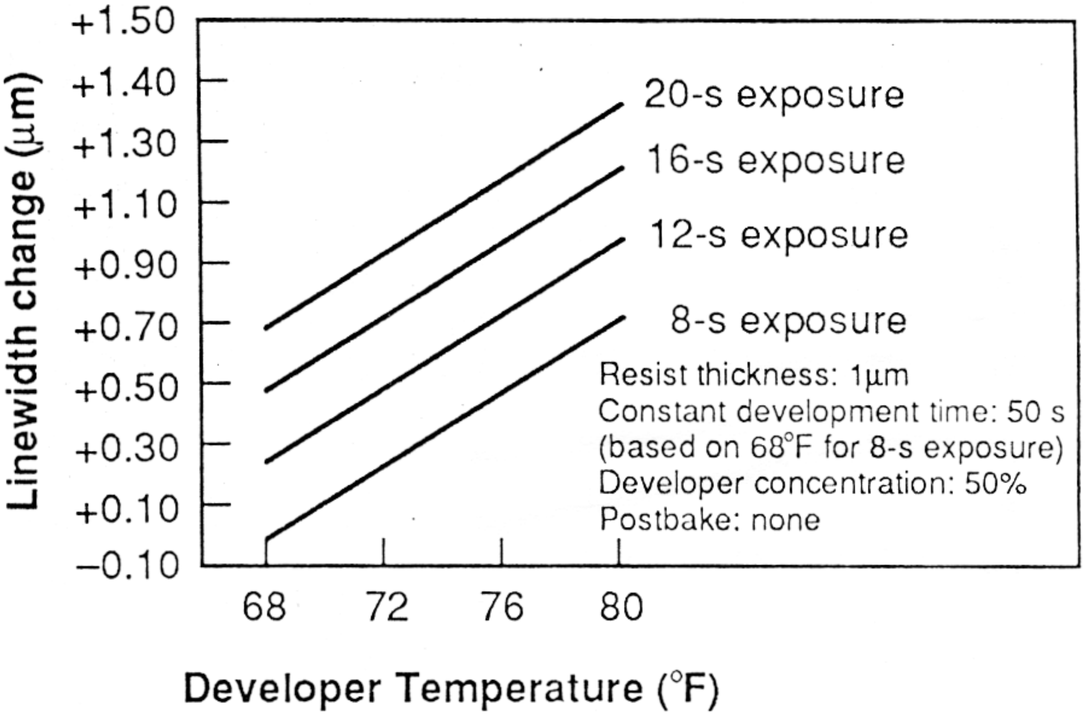


Figure 9.4 Developer temperature and exposure relationship versus line-width change.

Resist Hole/Line Width vs Development Time

- Let x_0 be the proper development time
  to clear resist from the structures

$$x_0 = \frac{t_0}{d_r}$$

where t_0 = film thickness
d_r = rate of resist development removal

- If < x_0 get remnant resist
- If > x_0 get bloated holes, narrow lines
- Always get some resist loss at top
- Sideways etching and ramp of exposure edge
- Light must penetrate through full layer of resist

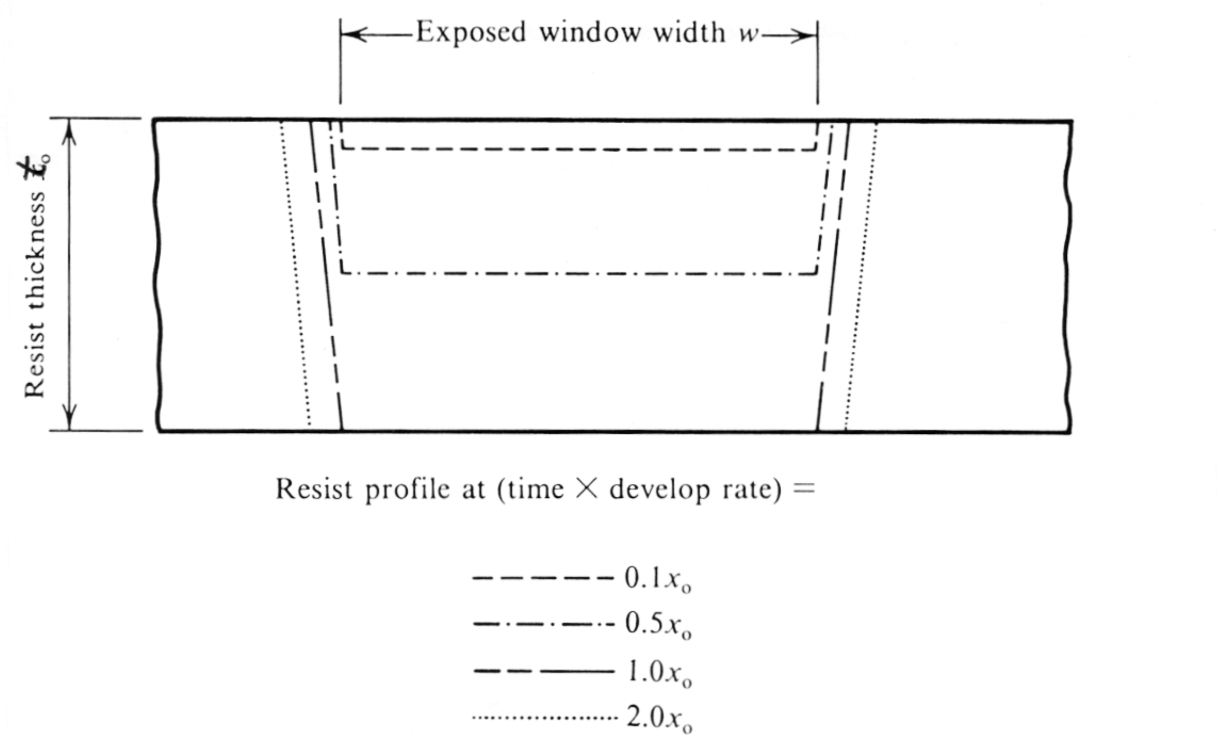


Figure 4-10 The evolution of positive resist development with time. Note that with time the pattern widens as well as deepens.

Proper Clearing of Resist

- Perfect Development
- Smallest holes (vias) clear of resist at bottom
- Smallest lines acceptable width
- No "stringers" between closest lines
- Usually overdevelop 5-10% so all structures clear
- Incomplete development: thick resist in openings
- Underdeveloped: sloped edges at bottom
  may leave resist scum (especially small opens)
- Overdeveloped: sloped sidewalls of resist
  Lines too small (may disappear or lift off)

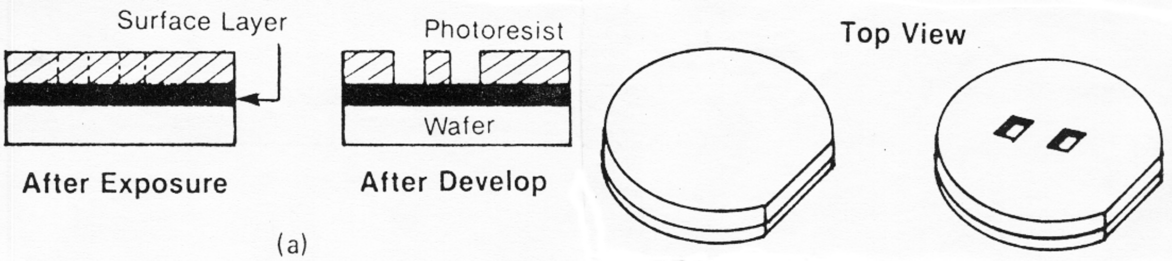
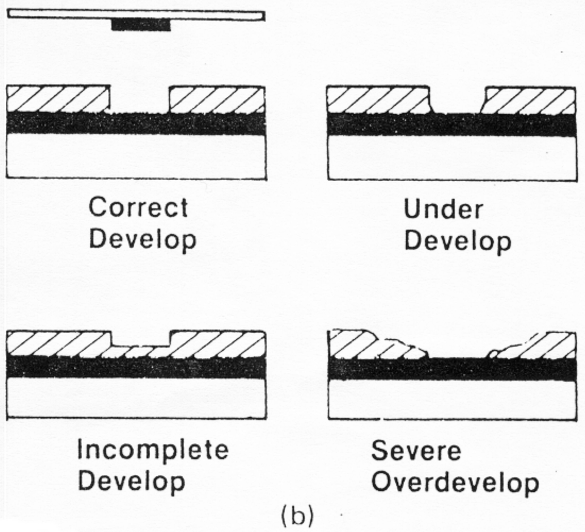


Figure 9.1 Photoresist development. (*a*) Process



(*b*) problems.

Mask Image Transfer to Resist Pattern

Mask Image Transfer to Resist Pattern

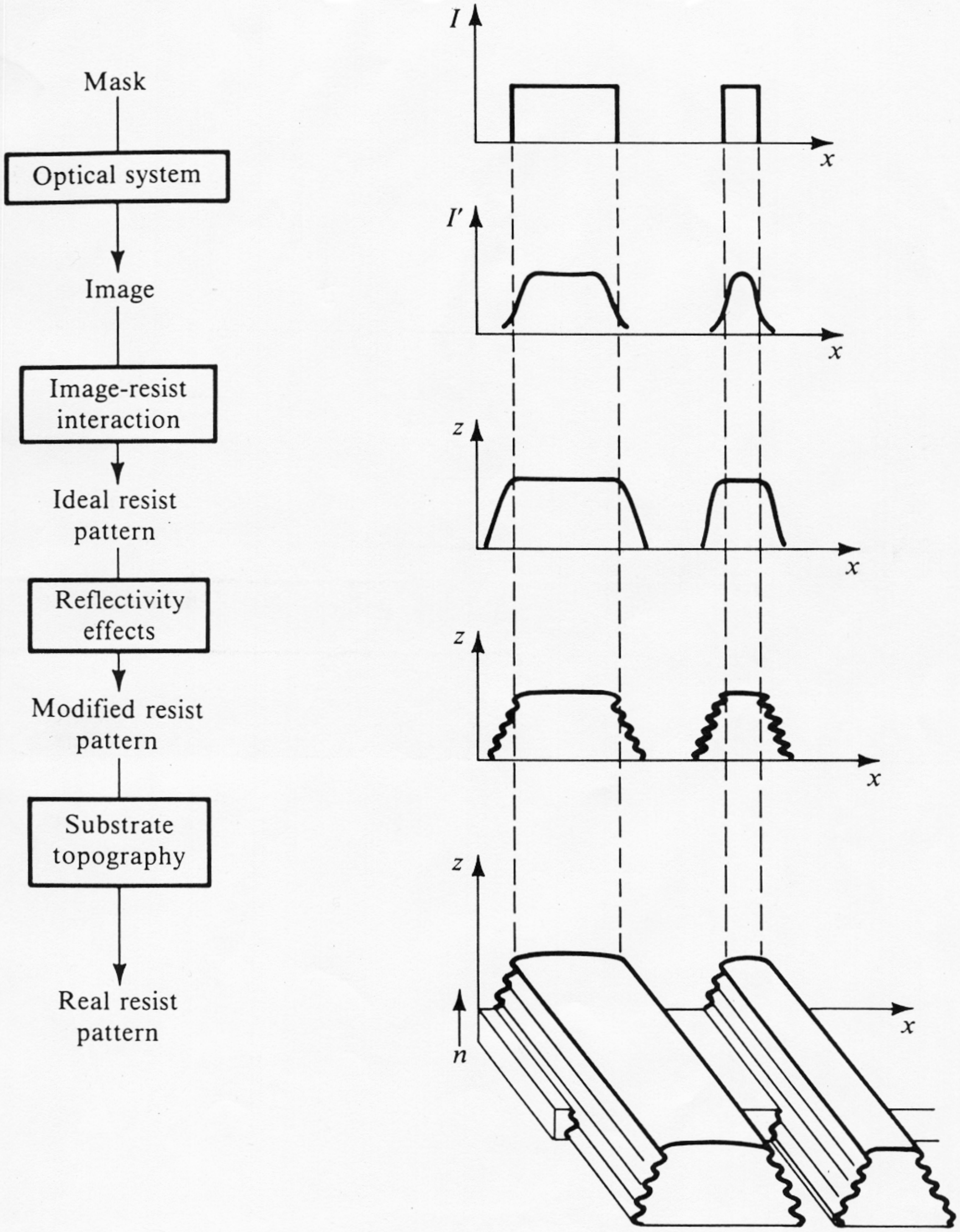


Figure 5-12 Factors affecting linewidth accuracy of resist images.

UV Reflection from Wafer Surface

- Wafer surface reflects UV back through resist
- Dull surface (oxide) small reflection & little effect
- Reflective surface (aluminum), significant effect
  exposure level much reduced
- At high resolution worry about
  optical interference in resist
- 1/4 wavelength interference effects create ripples in resist
- Creates standing wave patterns
- High resolution remove this: antireflection coatings
  multilayer resist (different index of refraction)

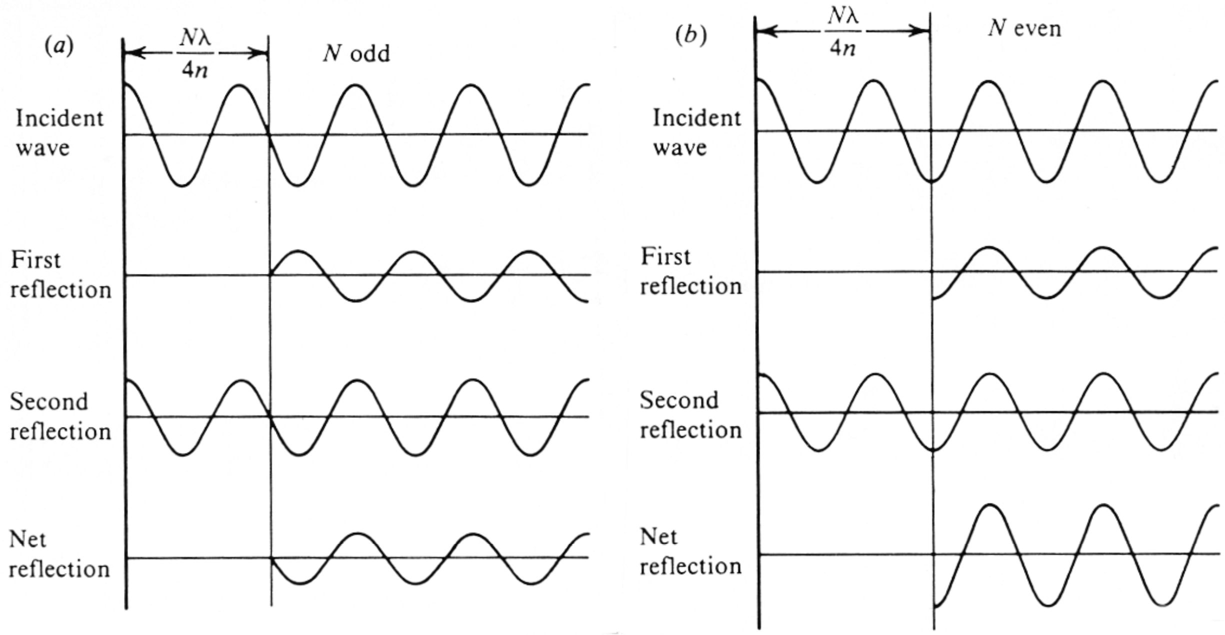
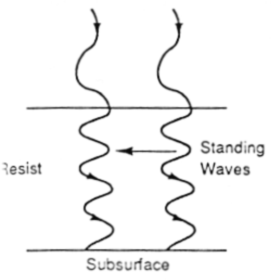
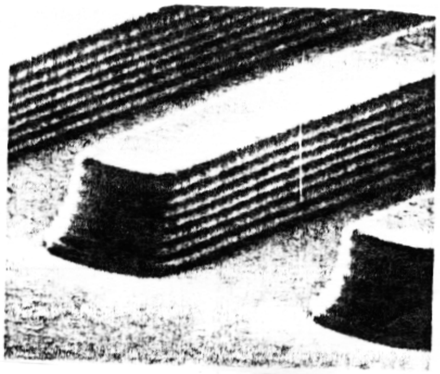


Figure 5-16 Standing wave effects in resist. (a) $z_0 = (N/4n)\lambda$, N odd. Destructive interference, low reflectivity, high absorption. (b) $z_0 = (N/4n)\lambda$, N even. Constructive interference, high reflectivity, low absorption.



(a)

igure 10.5 Standing-wave effect



Topology Effects on Resist

- Going over a step resist becomes very thick: piles up
- Uneven resist thickness - harder to expose, and develop evenly
- Also wider lines at crossover due to less development
- Reflection from adjacent structures reduces
  nearby structure width (notch in lines)
- Need to understand fab process & adjust layout to correct

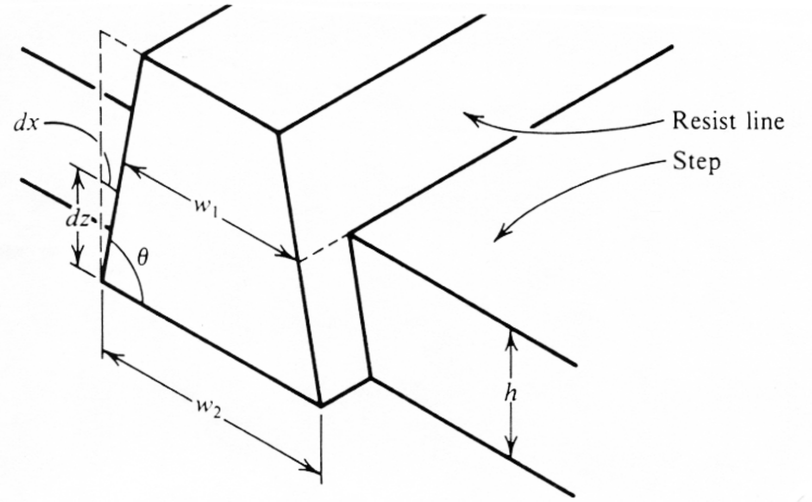


Figure 5-18 Geometrical effects on the linewidth of a resist line crossing a step.

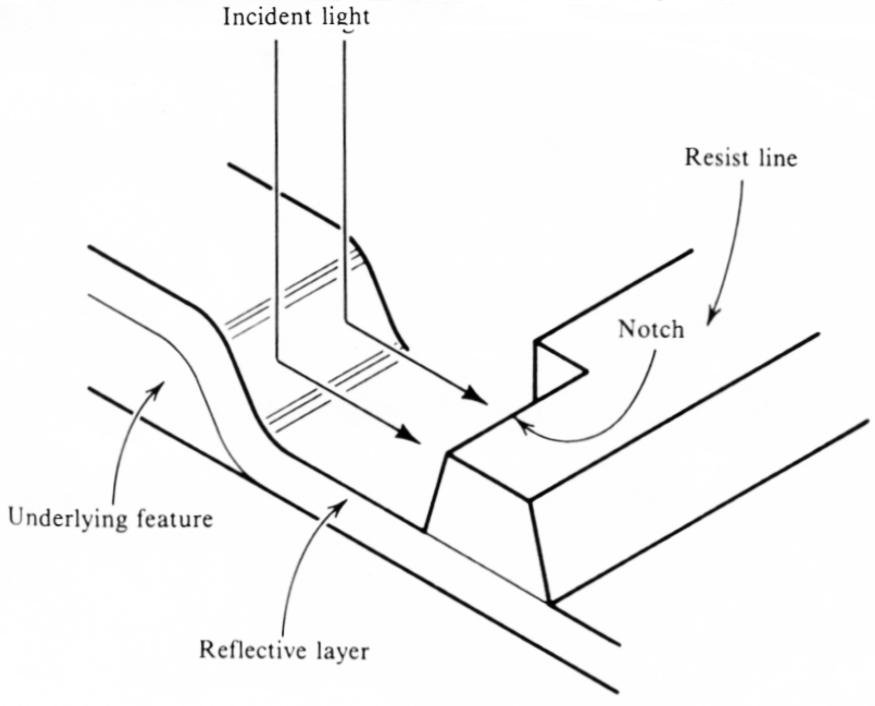


Figure 5-19 Line notching due to reflection of a nearby topological feature.

Mask Defects

- Mask defects the most deadly problem
- Repeat same defect on every wafer
- Typical problems
- Dirt on mask (may come from resist)
  solution: clean mask (easier with Chrome mask)
- Crack in glass, or scratched mask
  solution: replacement mask
- Photoemulsion masks last about 100 wafers
- Chrome almost indefinite: but more expensive
- Typical Mask cost $500-$1000

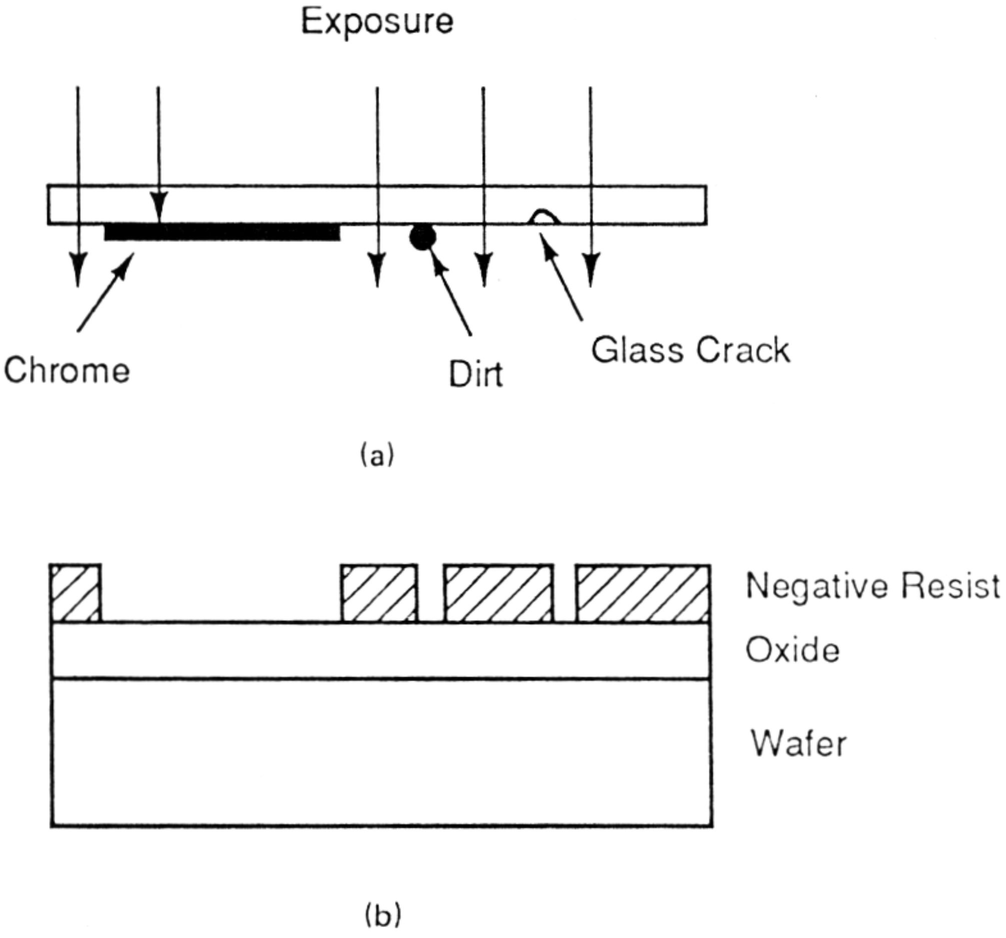
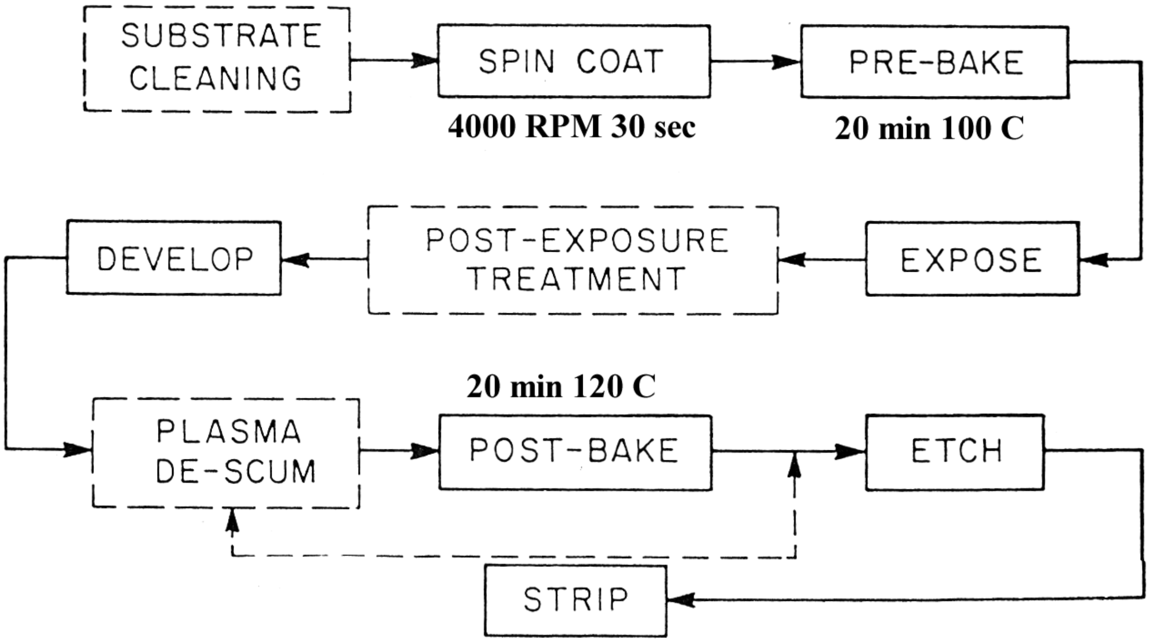


Figure 8.19 (*a*) Clear-field mask with dirt particle and glass crack, (*b*) result in negative resist after develop.

Photolith Hard Bake and Etching

- Sometimes do Plasma desum remove small remnant resist
- Sometimes expose edges additionally to remove edge bead
- Hard Bake makes resist tougher against etching
  drives off more solvent
- Typically 120^{o}C for 20 minutes
  Note: soft bake was at 100 ^{o}C
- If hard too short/or low temp does not resist etch
- If hard too long/or high temp trouble striping resist
- Etching next so must be hard enough to resist etchant eg acid
- Strip resist only with etch is desired level



4000 RPM 30 sec

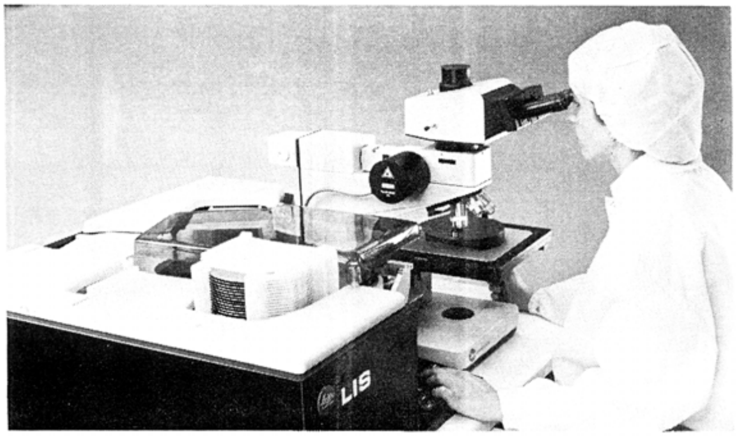
20 min 100 C

20 min 120 C

Fig. 14 Flow chart of a typical resist process. Steps in broken lines are not used for materials. Reprinted from Ref. 8 with permission of the American Chemical Society.

Wafer Inspection

- Always do test exposure at a level
- Calibrate light source/resist/developer for day
- Look for over/under development
- Centre of wafer: tends to underdevelopment
- Outer wafer: tends to overdevelopment
- Inspection done in yellow light often before hard bake
- Watch for resist defects:
  Pin holes, fish eyes, gel slugs, hard spots (after strip)
- Semiauto inspection stations
- Move to specified sites on wafer: check most difficult point
- Eg Leitz LIS, cost about $150,000 + film thickness measurement
- Full auto stations used computer image processing
- Identify defects based on expected images
- used for photolith and after etching



Photograph of a wafer inspection station.

Semi automated station

Automatic inspection

High Temperature Resist Flow

- At high Temperatures > 200 ^{o}C resist flows
- Creates sloped sidewalls
- Occurs in some processes (eg Ion Implantation)
- Heated resist hard to strip

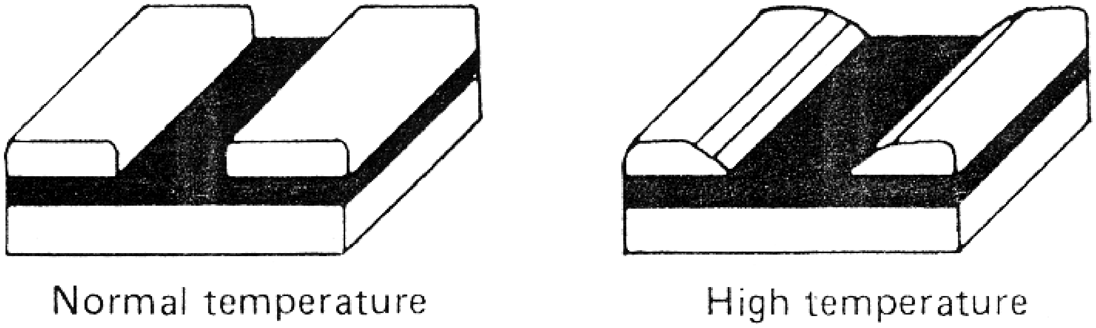


Figure 9.9 Resist flow at high temperature.

Photoresist Stripping

- Stripping extremely important for next process
- Major worry: remnant resist

Major Processes

- Solvent Strippers: Acetone (simple positive resists)
- Phenol-based organic strippers
- Inorganic strippers (Nitric/Sulfuric acids)
- Plasma Strippers: used in advanced fabs
  Creates an oxygen plasma that destroys organics
- Watch for resist "stringers" at step edges
- Some processes (eg high heat, Implant) make resist hard to strip
- Edge bead thick resist - very difficult to remove
  may make special long exposure of edge area only to remove

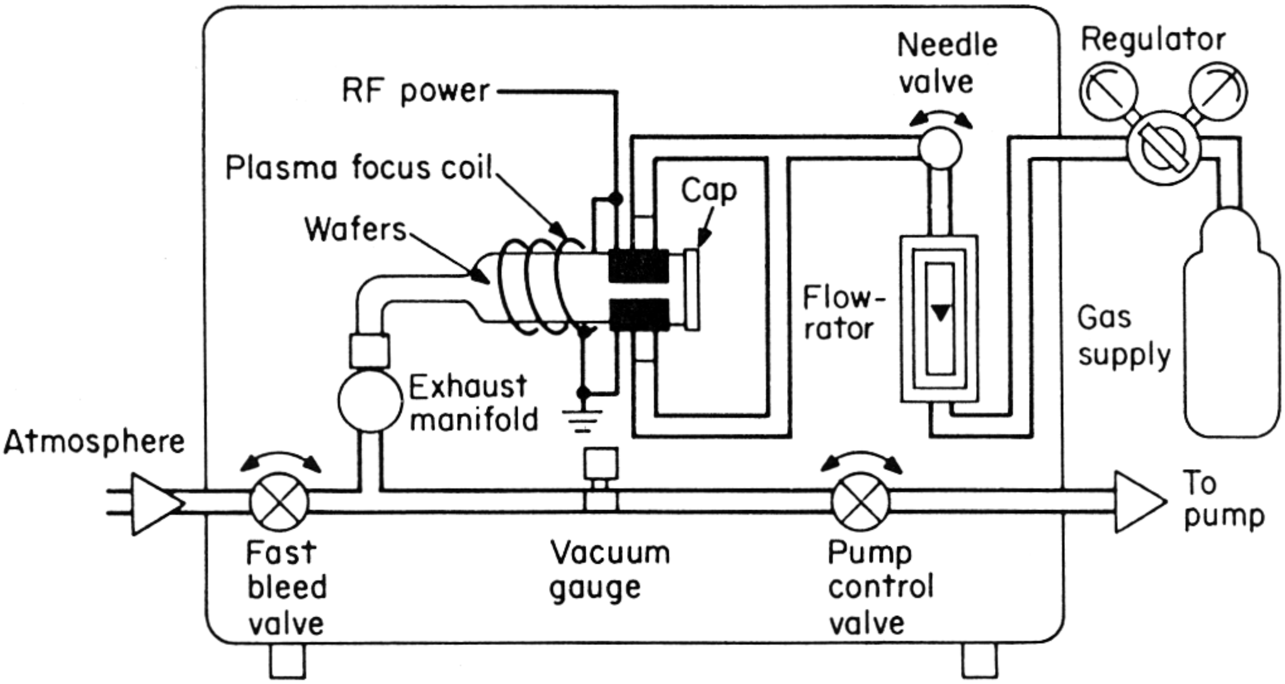


Figure 12.3 Plasma system diagrammatic cross section. (*Courtesy of LFE Corp.*)

Types of Exposure Systems

- The limit of any device is the minimum or critical feature size
- Typically that is the gate width of a MOS transistor
- Lithography usually sets the minimum geometry of devices
- Combination of the exposure system, mask and resist limits
- Mask aligner earliest & lowest cost exposure systems
- Vacuum Hard Contact: no shadow effects at edge
  but gets mask dirty
- Soft contact and Proximity good for >2-3 microns
- Projection systems: Optically project image using lens system
- Very expensive but low mask damage
- Shrinks image so much smaller structures
- Use 1:1 or 5:1 reduction (whole wafers)
- 5:1 or 10:1 reduction for step and repeat
- Now limitation becomes optical resolution of exposure system

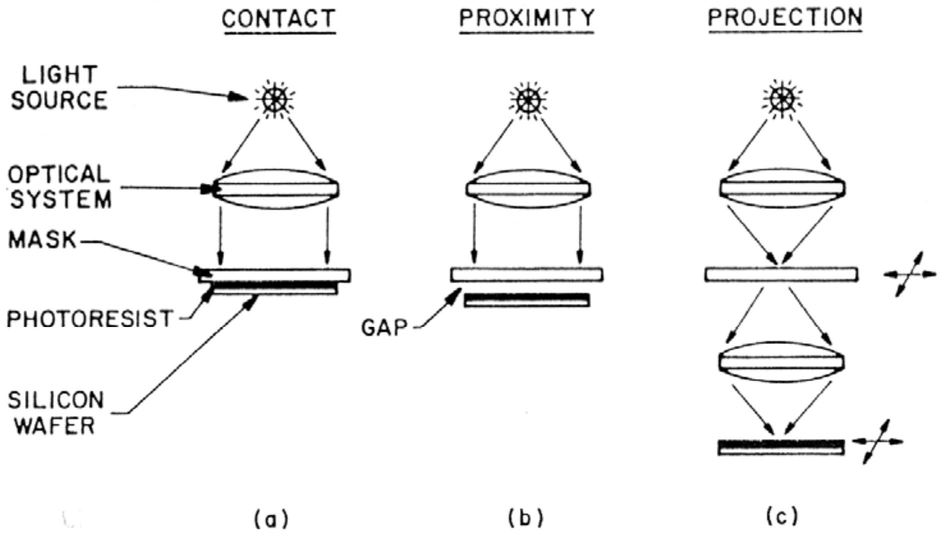
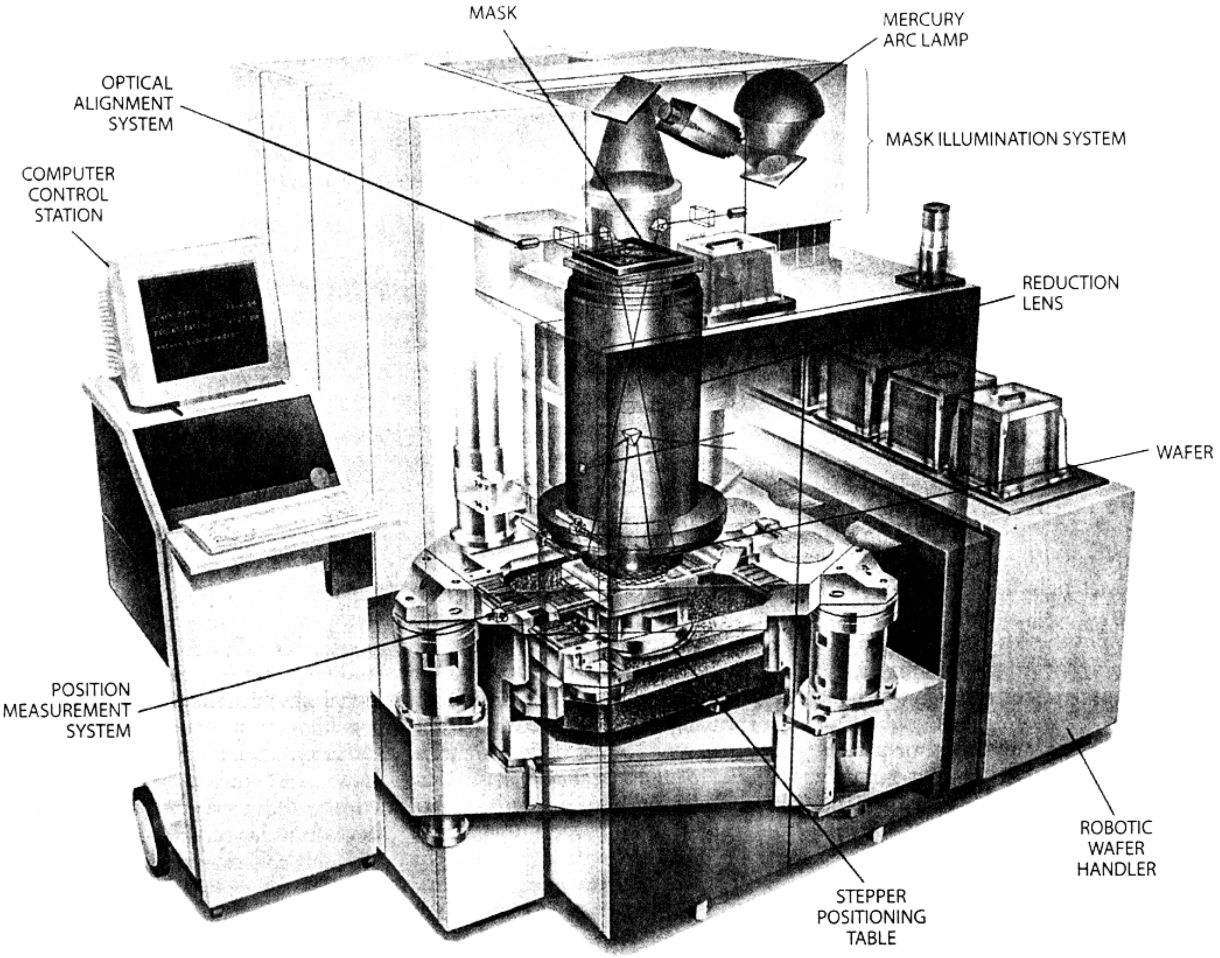


Fig. 11 Schematic of three optical lithographic techniques. (a) Contact. (b) Proximity. (c) Projection[27]. Copyright 1983, Bell Telephone Laboratories, Incorporated.

Wafer Steppers

- Called Direct Step on Wafer (DSW) or Steppers
- All systems < 2 microns
- Project one reticule (chip mask) print at a time
- Step to next chip site and repeat over wafer
- Reticules up to 3x3 cm now: may be one or several chips
- Table position uses laser interfereometry for < 0.1 micron
- Lens most expensive point

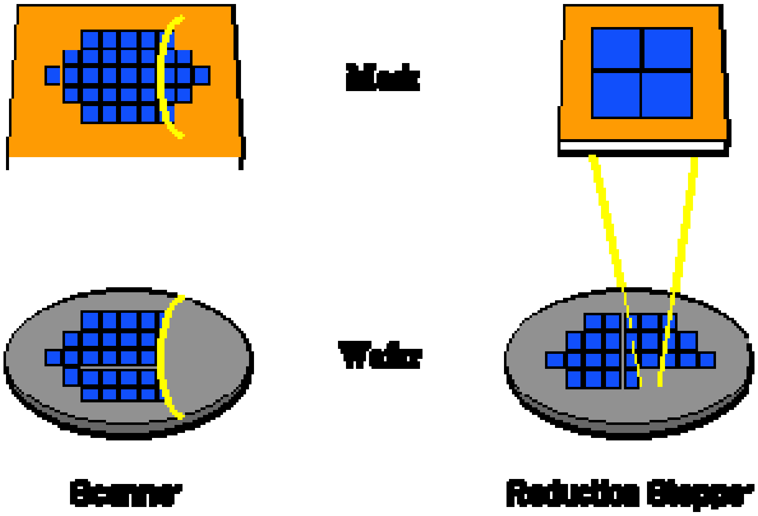


ASM LITHOGRAPHY

STEPPER, or photolithography machine, imprints circuit patterns on silicon wafers. Ultraviolet light from an arc lamp (or from a laser) passes through a mask bearing the image of the circuit. A sophisticated lens apparatus reduces the image and projects it onto part of a wafer. The table then moves, or "steps," to expose other chips.

Direct Step on Wafer (DSW)

- Typical cost $0.5-$10 million
- Cost depends on resolution and reticule area
- Smaller wafers steppers do small chip sizes
- Moving to laser light sources (single wavelength) for less expensive lenses



Projection Steppers Limits

- Lenses best every made: diffraction limited
- Important factor in lens is Numerical Aperature

$$NA = n \sin(\alpha)$$

- Typical NA 0.16 - 0.5 for steppers
- Smallest object projected set by

$$W_{\min} = k_1 \frac{\lambda}{NA}$$

- k_1 depends on resist and other factors ~0.7
- Depth of focus

$$\sigma = k_2 \frac{\lambda}{NA^2}$$

- k_2 also dependent on exposure system
- Thus shorter wavelength means more care with focus
- General optical rule Rayleigh Criteria ~ limit of resolutions $\lambda/2$
- So smallest Critical Dimension (CD) is set by wavelength

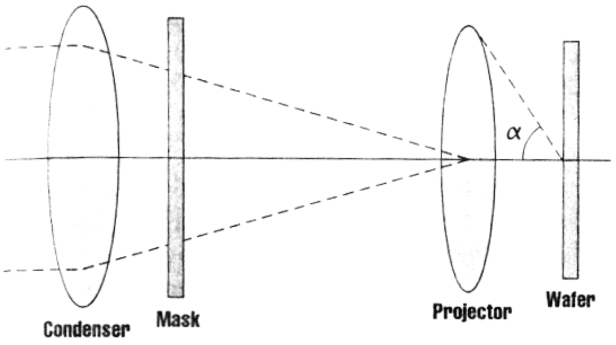
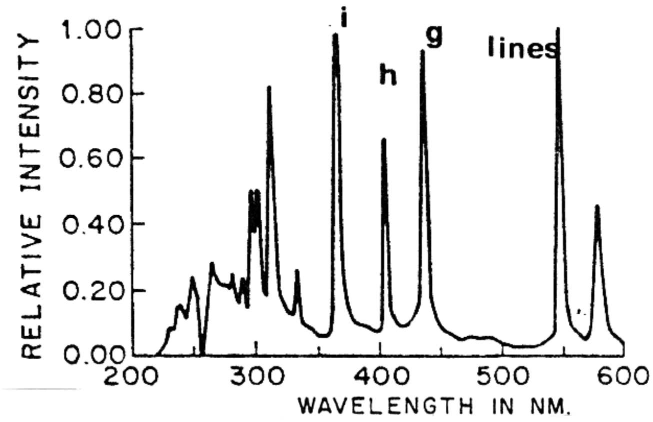


Figure 7-17 Schematic for the optical train of a simple projection printer.



high pressure mercury-arc spectrum.

Airy Disk Separation and the Rayleigh Criterion

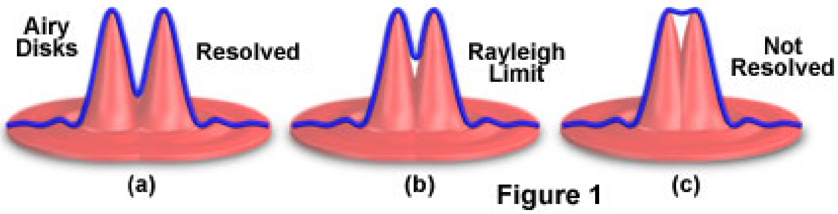
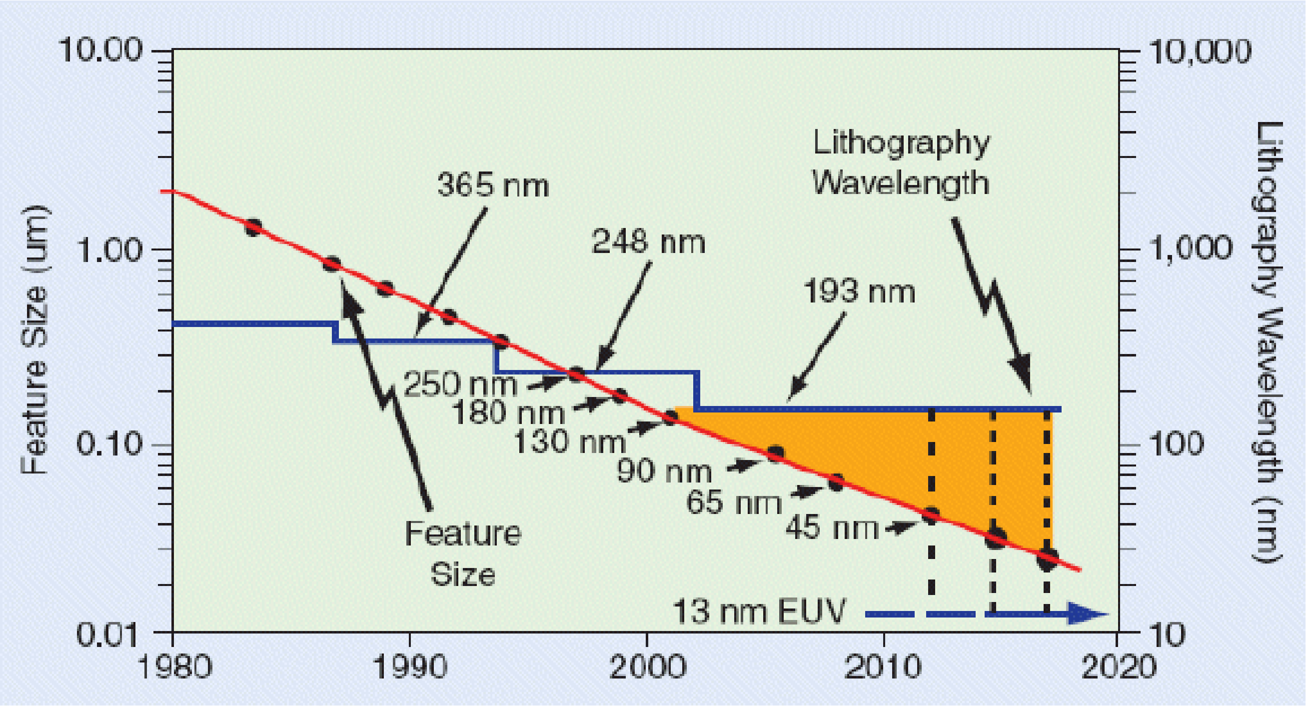


Figure 1

Wavelength and Steppers

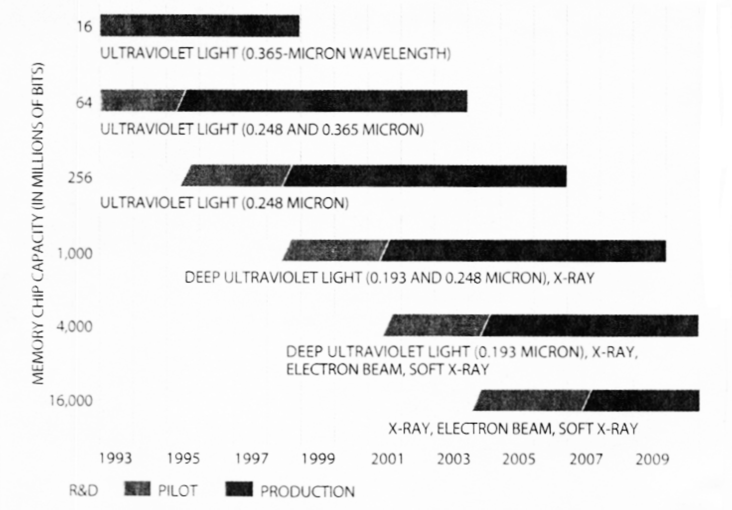
- First Steppers use Mercury Vapour lamp source
- Filters allow single line from source
- 1980: G line (439 nm) steppers > 0.8 microns
- 1990: I line (365 nm) steppers > 0.3 microns
- Now Excimer laser sources
- ~1994 KrF (248 nm) > 90nm,
- ~2001 ArF (193 nm) down to 90 nm (~λ/2)



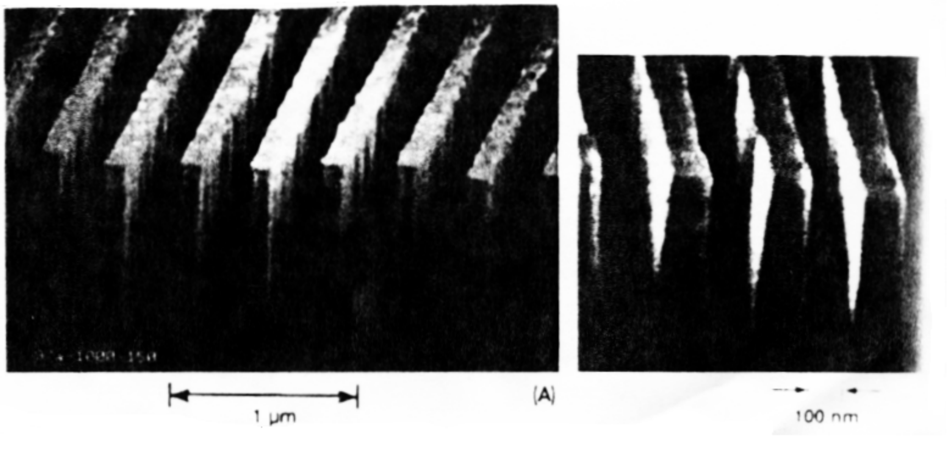
Ultratech 1700 Stepper: courtesy of Ultratech Stepper G line stepper

Comparison of Lithography Systems

- Putting in order of cost effectiveness
- Contact Mask aligner still lowest cost
  but resolution limited > 3 microns (80 Wafer/hr)
- 1:1, 5:1 Projections limited to > 1.5 microns
- 10:1 DSW now production standard to microns
  (50 wafers/hr typical)
- Deep UV (ArF 193 nm)
- Death of Optical Lithography often predicted
  but optical keep pushing limits
- Interference Phase shift masking pushing to 45 nm!
  below problem limit of transistor near 25 nm



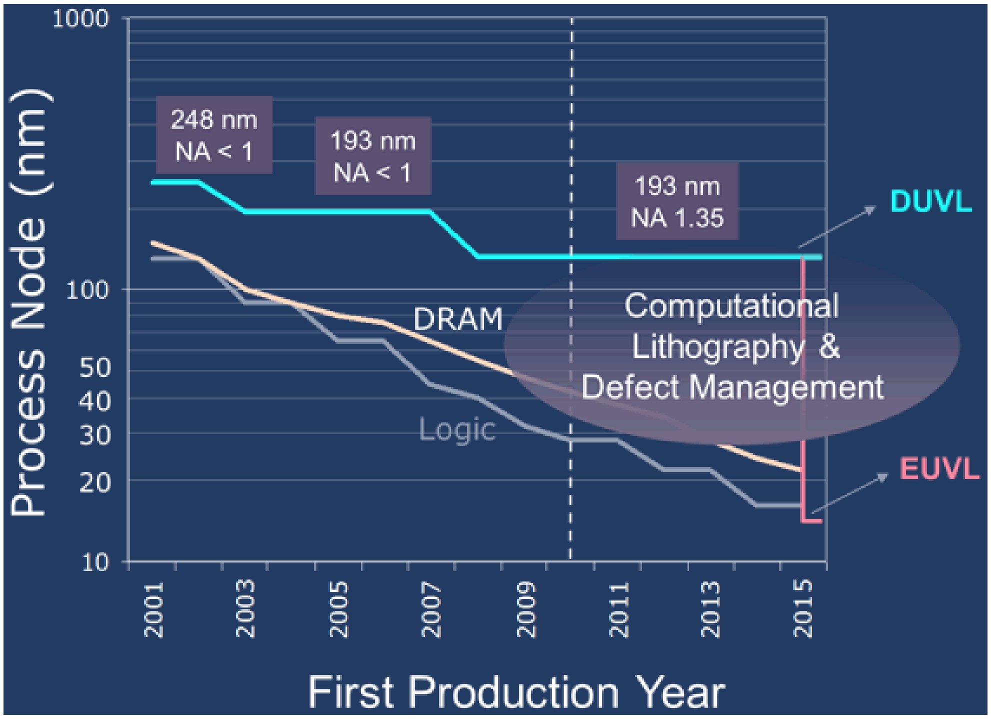
LITHOGRAPHY DEVELOPMENT in the U.S. calls for increasingly smaller wavelengths of light and other forms of electromagnetic energy to produce chips with ever larger memory capacity. The procession of chip generations will require moving to ever smaller wavelengths of ultraviolet light and then perhaps to x-rays or electron beams.



(a) 0.2 μm and (b) 0.15 μm lines imaged in 30 nm poly(n-butylsilyne)

Next Generation Lithography Project (NGL)

- Semitech (organization of main fab companies)
  Project for Next Generation Lithography (ie 2005 AD)
- Aims at device geometery below 35 nm (0.035 micron)
- 4 main contenters
- Extreme UV Optical EUV (13.4 nm)
- X-ray
- Scalpel (multiple e-beam systems by Lucent)
- Ion Projection Lithography
  Uses ion beams to project an image
- Current (2012) projection is EUV most likely to work but delayed
- Semitech Projections as of 2003 were:
- 180 nm (1995) 248 nm KrF Excimer DSW's
- 130 nm (~2001) 193 nm ArF Excimer DSW's
- 90 nm approx limit of 193 nm ArF’s
- 70 nm immersion lithography
- Phase shift masks now down to 40 nm
- Computational Lithography and Double exposure for 40-15 nm
- EUV 10 nm but has failed to work successfully



Immersion Lithography: A New Breakthrough

- Semitech 2003 assumed 157nm F_2 Excimer DSW's as next step
- Problem was 157 nm had lots of problems
- Lens materials fragile (CaF) F_2 Excimer difficult to use
- Old idea suddenly revived: **Immersion Lithography**
- Immerse lens & wafer in a high index fluid (DI water)
- Effective reduces wavelength of light by n (index of refraction)

$$\lambda_n = \frac{\lambda}{n}$$

- Use modified 193 nm steppers: same ArF Excimer & lens
- Now get 133 nm effective source ($n_{water} = 1.44$)
- Effectively increases Numerical Aperature

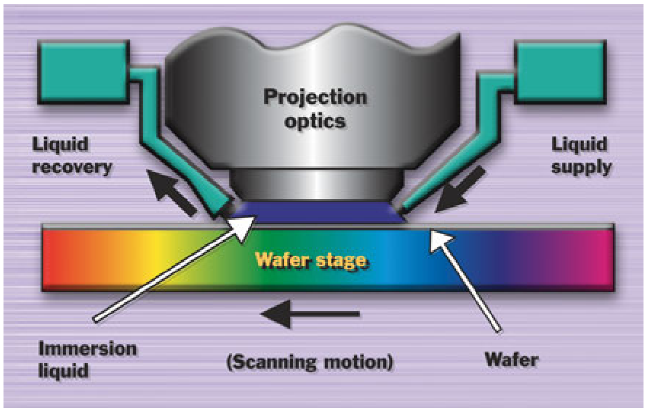
$$NA = n \ \sin(\alpha)$$

- NA goes from 0.5- 0.7 to 0.7 and targets > 1
- Since smallest object projected set by

$$W_{\min} = k_1 \frac{\lambda}{NA}$$

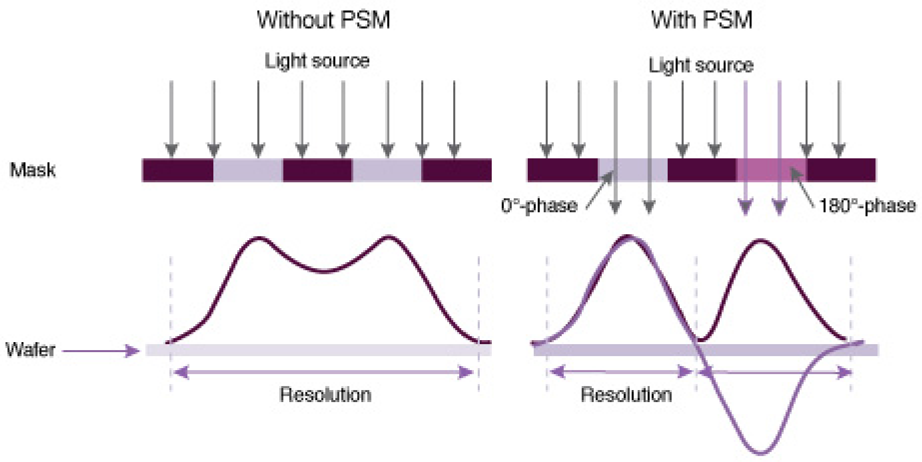
- Significantly increases resolution – possibly to 40 nm range
- Cost is reduced Depth of focus is reduced

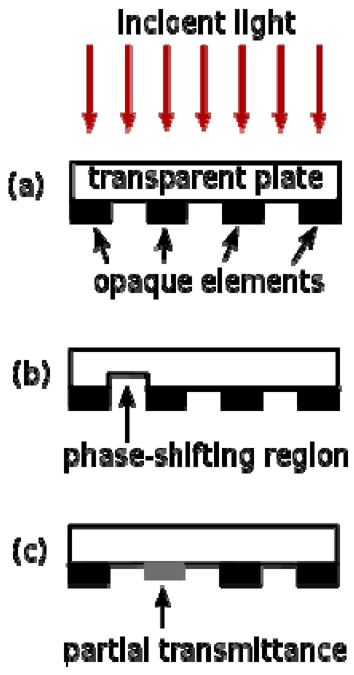
$$\sigma = k_2 \frac{\lambda}{NA^2}$$



Phase Shift Mask

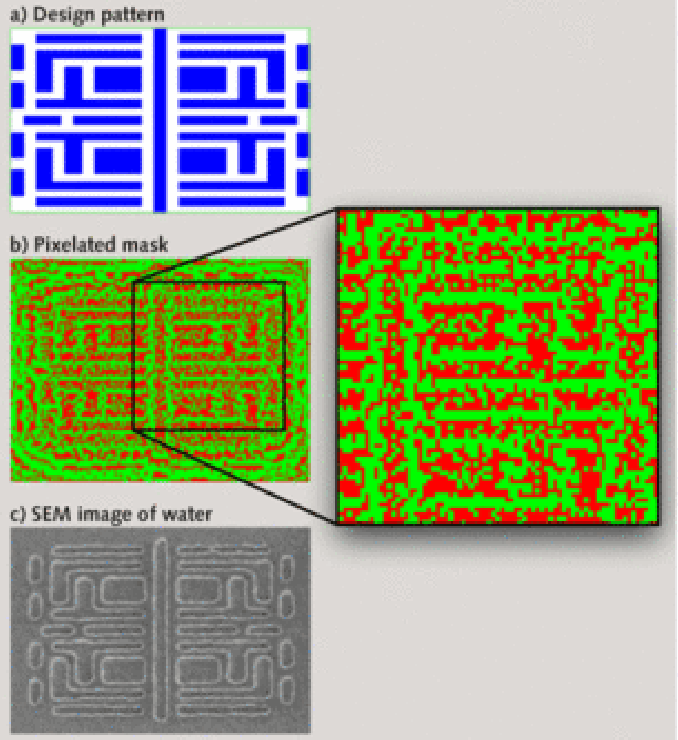
- Regular optical limits is ~λ/2 so 70 nm for immersion
- But what if change masks: add a layer that phase sifts the light
- If invert the phase of light then can make line < diffraction limit
- Get about ~λ/4 or 35 nm structures
- Create phase shift by etching mask glass
- Alternative adding semitransparent





Computational Lithography

- Failure to get shorter wavelengths than 195 immersion
- To reduce more from Phase shift use Computational Lithography
- Phase shift at limit creates distorted structure
- Instead design the optical pattern you want on the wafer
- Now compute using Emag wave pattern back through stepper
- Find the mask patter to create structure want in resist
- Very compute intensive operation – only on smallest structures
- With this get 20-25 nm structures

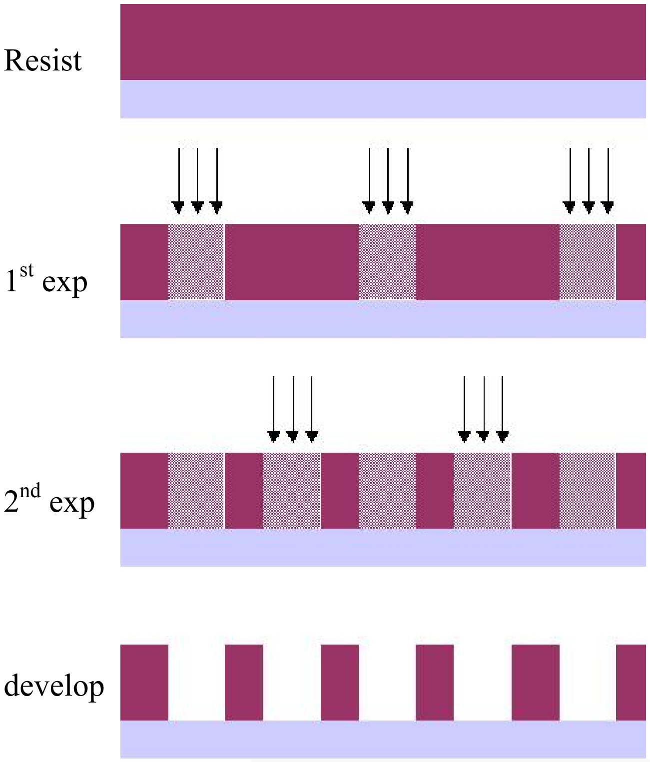


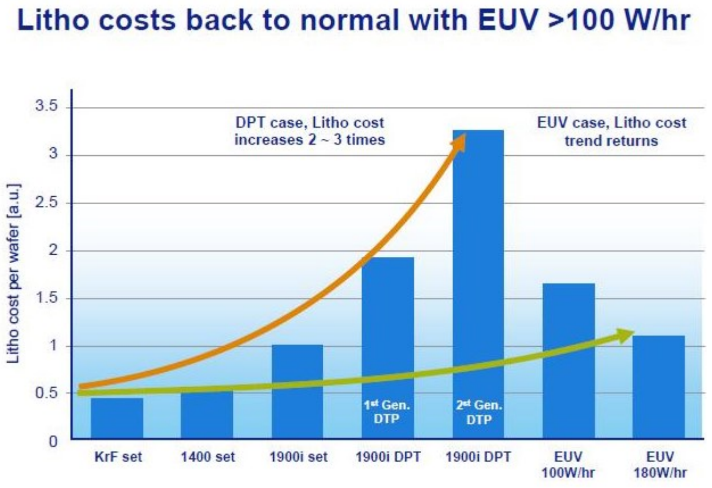
A portion of the 65nm metal 1 design (a) is converted to a pixelated phase mask design (b), where red represents 180° phase shift pits and green represents 0°, and projected by the stepper forming the resist image in (c).

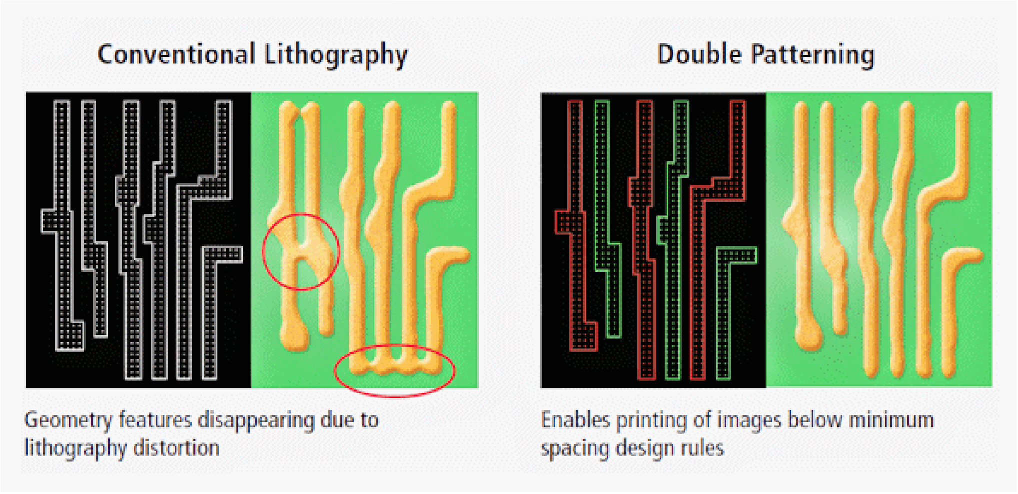
WaferNews source: Intel Corp.

Double Patterning Lithography

- Continual delay of EUV requires solutions for <20 nm
- Now using Double Patterning methods
- Useful for close spaced lines/patterns in on direction
- Expose odd patterns with first mask
- Expose even with 2nd mask – reduces diffraction in one direction
- Then develop pattern
- Problem – 2 masks/exposures – 2x to 3x costs!
- But need for 15nm





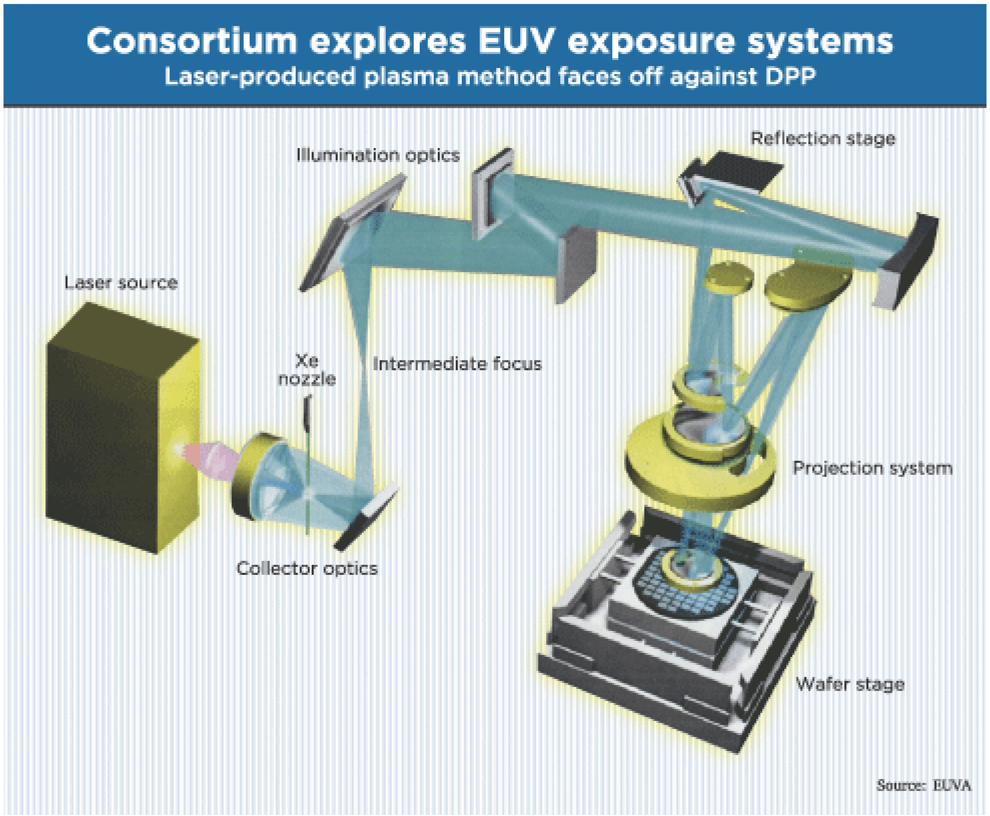


Geometry features disappearing due to lithography distortion

Enables printing of images below minimum spacing design rules

Extreme UV Lithography (EUV)

- Next Generation Lithography Extreme UV 13.5 nm
- Under development at Lawrence Livermore Lab since 2000
- Uses Laser Produced Plasma Source (LPS)
- Uses Nd:Yag laser focused on copper wire or Xeon gas
- Creates a plasma with 13.4 nm EUV emission
- Near X-ray but acts like light (not too penetrating)
- Must use grazing mirror reflectors for optics in 10X stepper
- Probably will exceed the ultimate transistor limits.
- Problem as of 2013 trouble getting the system to work well
- Not certain if EUV will get to 10 nm devices
- Transistor operation limit in 5-10 nm range



Consortium explores EUV exposure systems

Laser-produced plasma method faces off against DPP

Source: EUVA

Resists for Next Generation Lithography

- Use Thin Layer Imaging (TLI) process
- At 157 & 13 nm light only penetrates very thin layer
- Use an organic planerization layer (organic resist)

Refractory Bilayer Resist

- Thin Organio-Silicon Layer absorbs EUV
- Development removes exposed area
- Resist left behind contains silicon
- In O plasma converst to a SiO_2 glass
- O plasma transfers glass pattern to resist layer

TSI Silyatation

- Top organic imaging layer exposed
- Resist polymer cross links, preventing diffusion
- Silylation: aminosilane gas diffuses Si into unexposed
- O plasma converts to glass during patterning of lower resist

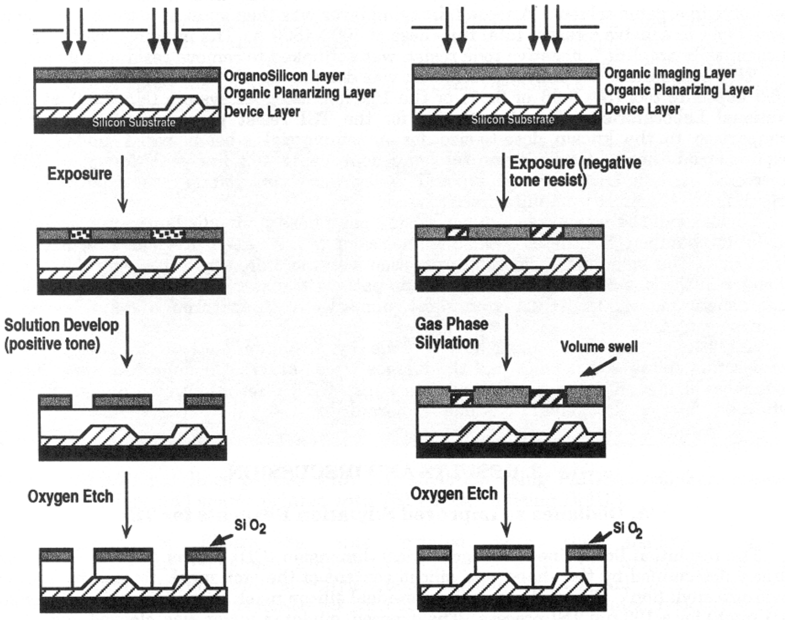
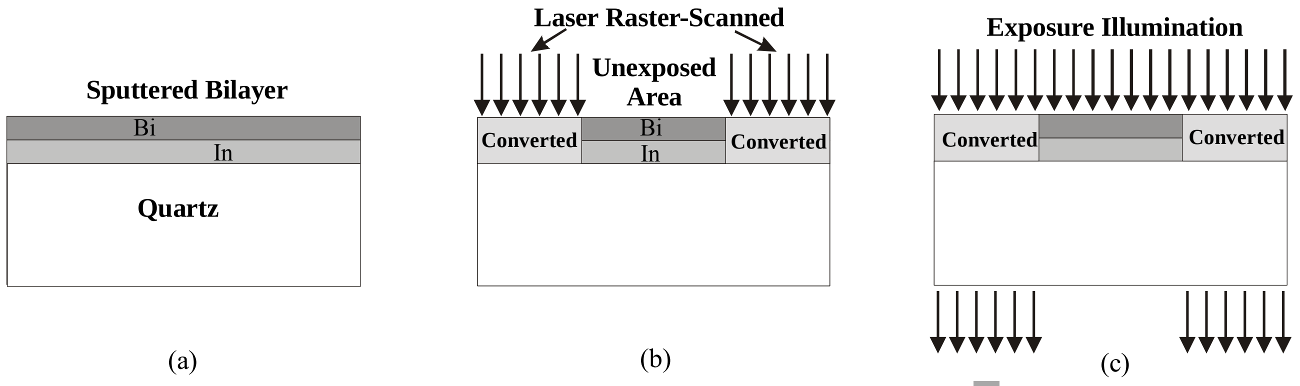


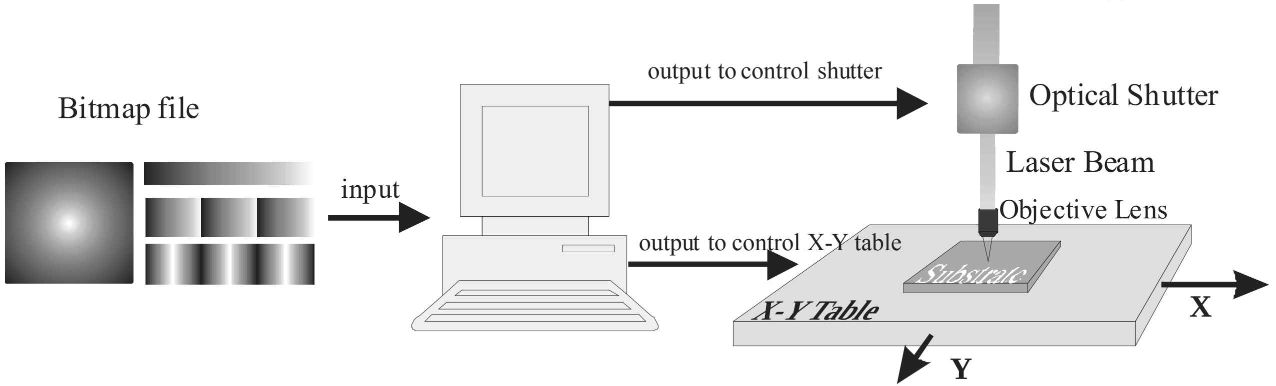
Figure 1 - General photoresist processing schemes for refractory bilayer (left) and TSI silylation (right).

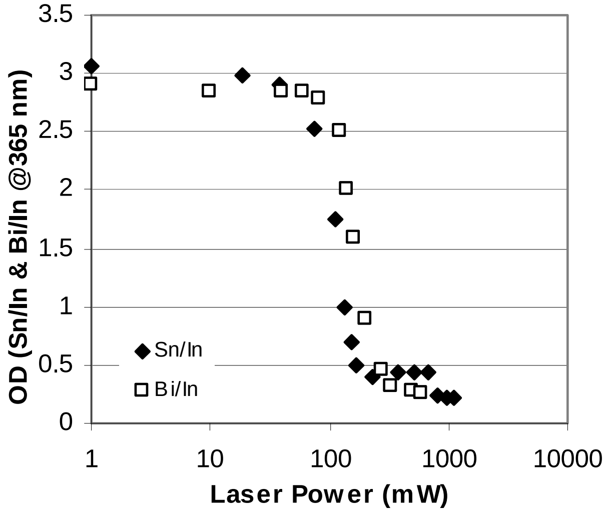
Henerson, SPIE 3331, pg 32 1998

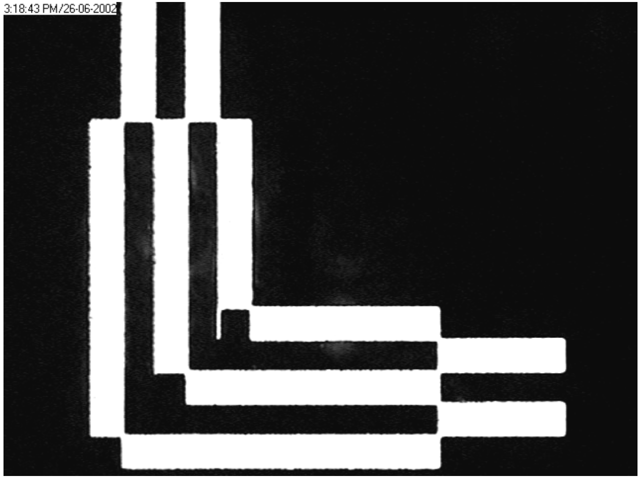
Laser Direct Write Photomasks

- Classic photomasks have are chrome cover quartz/glass plates
- Write pattern in resist on chrome (laser or e-beam)
- Develop resist, etch chrome (hard to prevent defects).
- Work in my lab a direct laser write photomask
- Put down ~15-100 nm film of Bismuth & Indium
- When hit with laser turns transparent: change from 3OD to 0.2 OD
- When laser hits Bi/In or Sn/In film creates transparent oxide



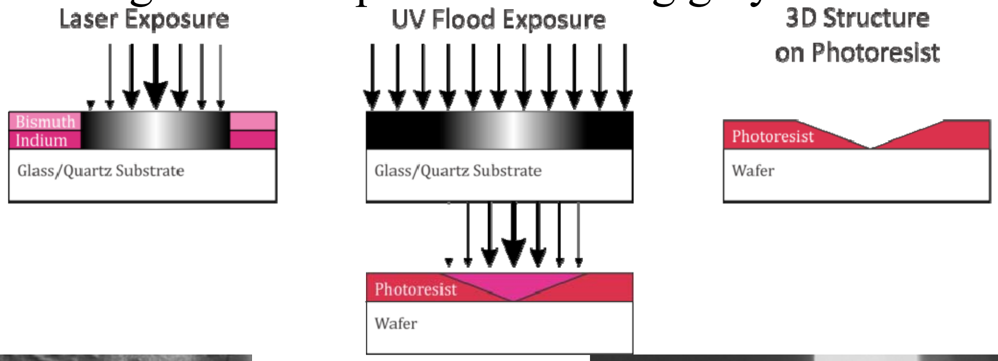


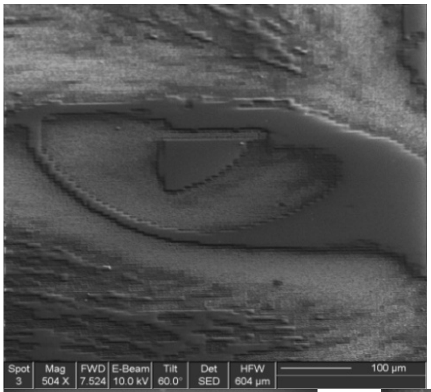


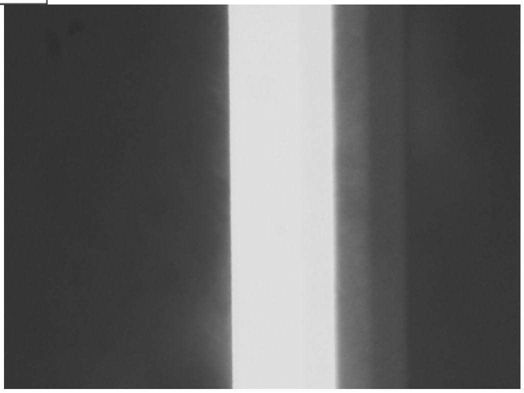


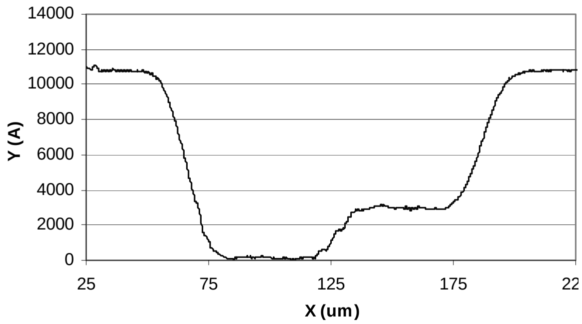
Bimetallic Grayscale Photomasks

- Grayscale masks contain many gray levels
- When hits photoresist developed thickness function of exposure
- Can create 3D microfabricated devices (eg. Microoptics, MEMS)
- Better OD range and cheaper than existing grayscales









Original picture

Grayscale mask