Ion Implantation

- Most modern devices doped using ion implanters
- Implant dopants by accelerating individual atoms (ions)
- Ionize gas sources (single +, 2+ or 3+ ionization)
- Use analyzer to selection charge/mass ratio (ie ionization)
- Accelerate dopant ions to very high voltages (10-600 KeV)
- Bend beam to remove neutral ions
- Raster scan target: implant all areas at specific doping – thus slow
- Just integrate charge to get total dopant level for wafer

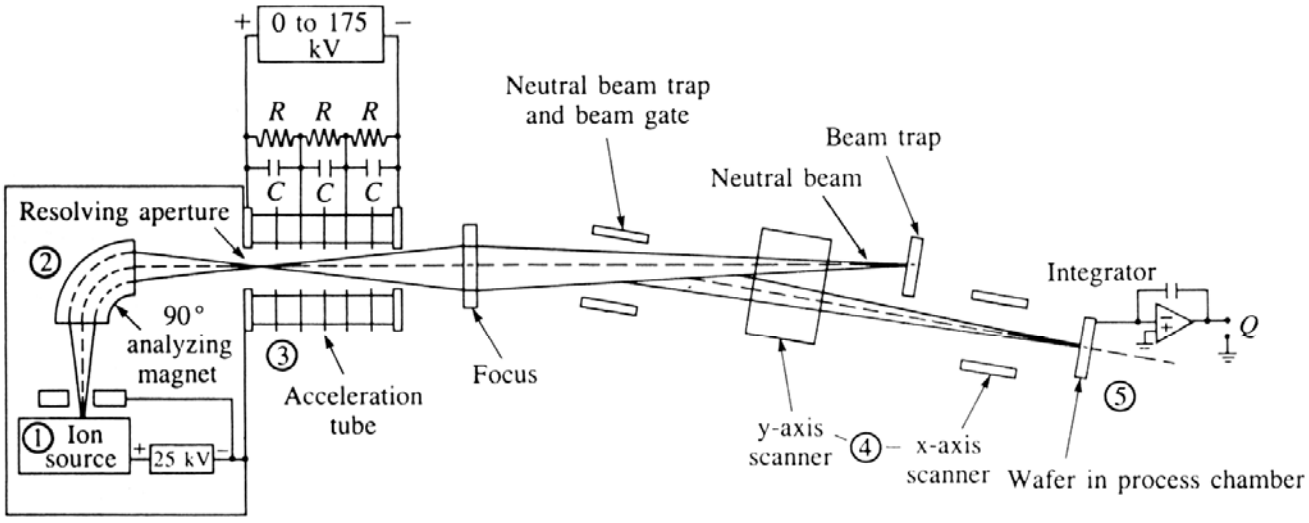


Fig. 5.1 Schematic drawing of a typical ion implanter showing (1) ion source, (2) mass spectrometer, (3) high-voltage accelerator column, (4) *x*- and *y*-axis deflection system, and (5) target chamber.

Ion Implanter

Implanter end station

Ion Implantation

Advantages

- Precise control of doping levels in both position and depth
- Measure dopants dose in atom/cm^2
- Much less dopant spreading (sideways & down)
- Regular diffusion spreading is several microns
- Hence implant needed for small structures – devices <2 μm

Disadvantages

- Implanters expensive $1 - $10 million
- To get depth may need high voltage/high current
  double or triple ionized (which gives lower rates)
- Heavy radiation damage to crystal
- Dopant need to be activated (tends to go interstitially)
- Implant creates high temperature in resist & loads it with dopant
- Hence resist very hard to strip
- Single wafer and raster scan – thus long time to implant
- Diffusion does many wafers at once, implant one at a time

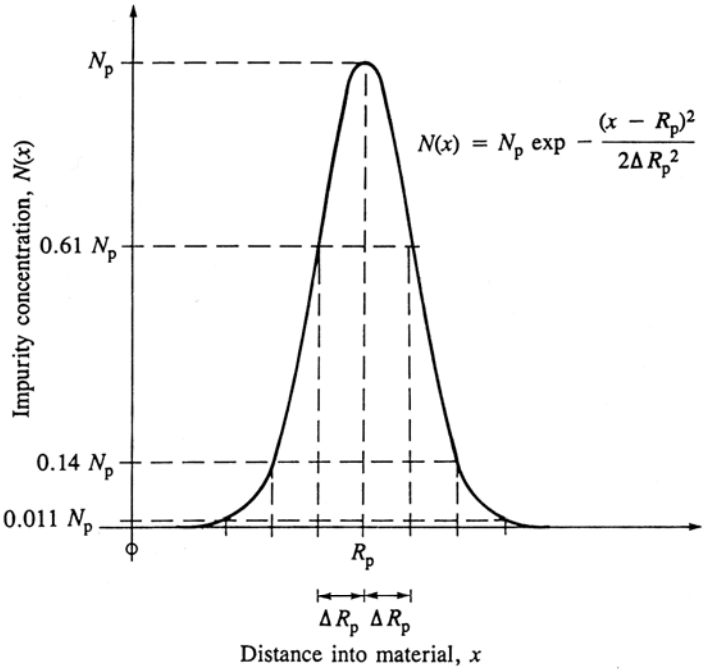


Fig. 5.2 Gaussian distribution resulting from ion implantation. The impurity is shown implanted completely below the wafer surface ($x = 0$).

Ion Implant useful Formulas

- Energy E_i in each ion is (in electron Volts)

$$E_i = \frac{1}{2}mv^2 = ZeV$$

Where V = accelerating voltage (Volts)
v = velocity of the ion
m = mass of the ion
Z = e charges on the ion (number of charges)
e = electron charge = 1.60×10^{-19} C

- Thus 1 eV = 1.60×10^{-19} Joules
- Source atoms are single isotope – ie same atomic weight
- Eg P^{31} phosphorus with 31 atomic weight (15 protons, 16 neutrons)
- Atom's mass is atomic weight times Atomic Mass Unit (amu)
- amu = 1.6605×10^{-27} kg
- Implant values are given as beam current in Amps
  current is same if either electrons or ions
- Total implant dose Q is

$$Q = \frac{It}{ZeA}$$

Where I = beam current (Amps)
t = implant time to scan area (sec)
A = area (sq cm)

- Energy from ions are deposited throughout stopping range

Dopant Range with Implanter

- Ions follow a Gaussian atomic stopping range

$$N(x) = \frac{Q}{\sqrt{2\pi}\,\Delta R_p} exp\left[-\frac{(x - R_p)^2}{2(\Delta R_p)^2} \right] \quad and \quad N_p = \frac{Q}{\sqrt{2\pi}\,\Delta R_p}$$

- R_p = Peak range (depth of the Gaussian peak)
- ΔR_p = Straggle of range width of Gaussian
- N_p = dopant density at the peak range
- Both R_p and ΔR_p are function of ion type, energy, and target (cross section for stopping in material)

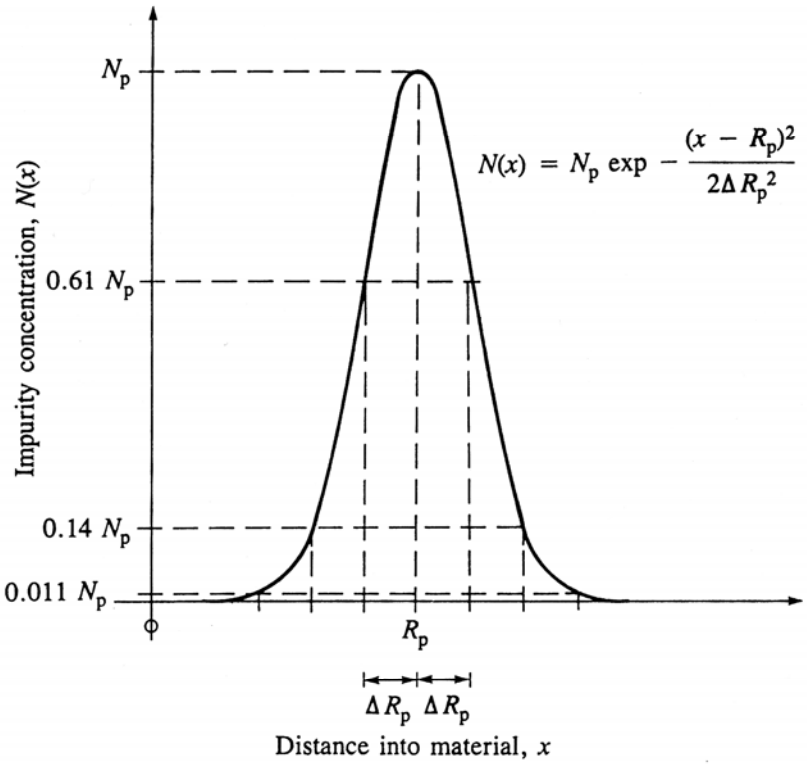


Fig. 5.2 Gaussian distribution resulting from ion implantation. The impurity is shown implanted completely below the wafer surface ($x = 0$).

Implanter Projected Range R_p

- Varies with accelerating voltage dopant and substrate material
- Ions & targets have different interaction cross sections
- Calculated using complex stopping Monte Carlo programs
- Different values for implanting silicon or glass
- Standard reference
- Gibbons, Johnson, and Mylroie, Projected Range Statistics, 2nd. Ed
- Brigham Young Univ has nice implant range/straggle calculator

http://www.cleanroom.byu.edu/rangestraggle.phtml

- Note values vary with table depending on calculation method

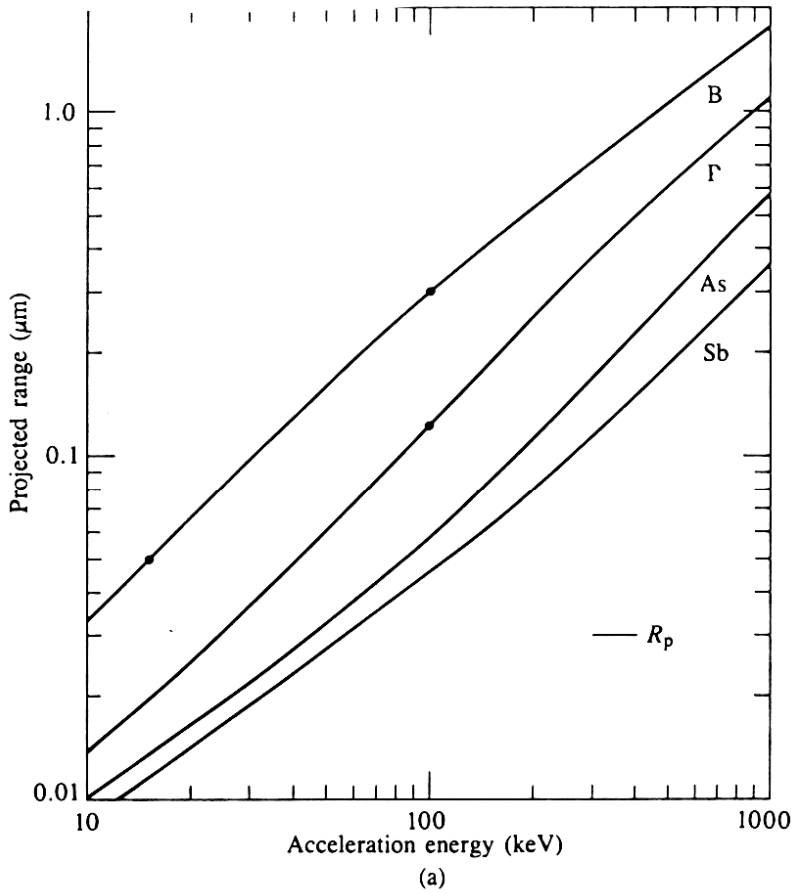
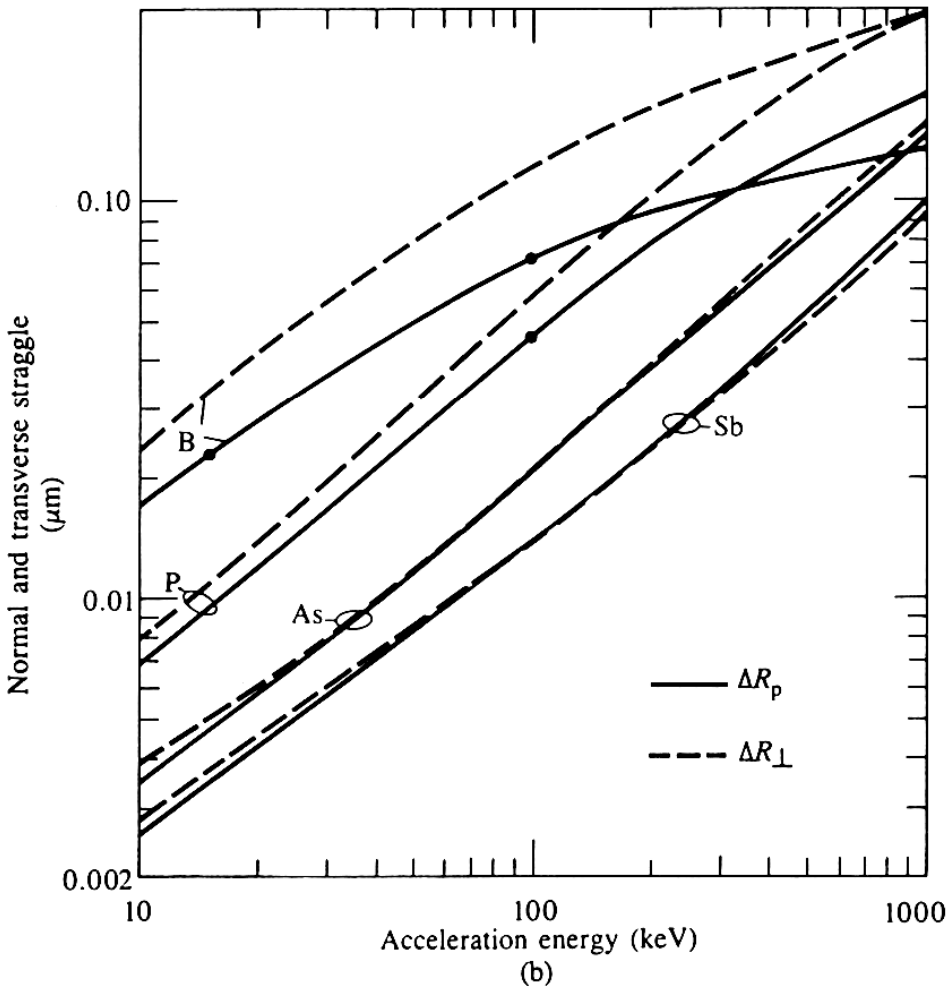


Fig. 5.3 Projected range and straggle calculations based on LSS theory. (a) Projected range R_p for boron, phosphorus, arsenic, and antimony in amorphous silicon. Results for SiO_2 and for silicon are virtually identical. (b) (On page 94) Vertical ΔR_p and transverse $\Delta R_\perp$ straggle for boron, phosphorus, arsenic, and antimony. Reprinted with permission from ref. [2].

Implanter Straggle ΔR_p

- Varies with accelerating voltage, dopant ion, & substrate
- Normal straggle ΔR_p is into depth
- Transverse straggle $\Delta R_\perp$ is sideways under mask edge



Range and Straggle Tables

- Implant R_p , ΔR_p for common ions and energies in Silicon & oxide

	P in Si		P in SiO_2		B in Si		B in SiO_2	
Energy (kEv)	**Rp**	**ΔRp**	**Rp**	**ΔRp**	**Rp**	**ΔRp**	**Rp**	**ΔRp**
10	0.0139	0.0069	0.0108	0.0048	0.0333	0.0171	0.0298	0.0143
20	0.0253	0.0119	0.0199	0.0084	0.0662	0.0283	0.0622	0.0252
30	0.0368	0.0166	0.0292	0.0119	0.0987	0.0371	0.0954	0.0342
40	0.0486	0.0212	0.0388	0.0152	0.1302	0.0443	0.1283	0.0418
50	0.0607	0.0256	0.0486	0.0185	0.1608	0.0504	0.1606	0.0483
60	0.0730	0.0298	0.0586	0.0216	0.1903	0.0556	0.1921	0.0540
70	0.0855	0.0340	0.0688	0.0247	0.2188	0.0601	0.2228	0.0590
80	0.0981	0.0380	0.0792	0.0276	0.2465	0.0641	0.2528	0.0634
90	0.1109	0.0418	0.0896	0.0305	0.2733	0.0677	0.2819	0.0674
100	0.1238	0.0456	0.1002	0.0333	0.2994	0.0710	0.3104	0.0710
110	0.1367	0.0492	0.1108	0.0360	0.3248	0.0739	0.3382	0.0743
120	0.1497	0.0528	0.1215	0.0387	0.3496	0.0766	0.3653	0.0774
130	0.1627	0.0562	0.132	0.0412	0.3737	0.0790	0.3919	0.0801
140	0.1727	0.0595	0.1429	0.0437	0.3974	0.0813	0.4179	0.0827
150	0.1888	0.0628	0.1537	0.0461	0.4205	0.0834	0.4434	0.0851

*Rp and ΔRp in μm

- Gibbons, Johnson, and Mylroie, Projected Range Statistics, 2nd. Ed
- http://fabweb.ece.uiuc.edu/gt/gt/gt15.aspx
- Implant R_p, ΔR_p, for 100 KeV Boron in different materials

TABLE 1
Boron ranges in various materials[13,14,15]

100 keV boron implantation				
Material	**Symbol**	**Density (g/cm³)**	**R_p(Å)**	**ΔR_p(Å)**
Silicon	Si	2.33	2968	735
Silicon dioxide	SiO_2	2.23	3068	666
Silicon nitride	Si_3N_4	3.45	1883	408
Photoresist AZ111	$C_8H_{12}O$	1.37	10569	1202
Titanium	Ti	4.52	2546	951
Titanium silicide	$TiSi_2$	4.04	2154	563
Tungsten	W	19.3	824	618
Tungsten silicide	WSi_2	9.86	1440	555

Spreading of Implant Dopant from Opening

- Scattering of ions causes dopant to spread to side: $\Delta R_\perp$
- Note peak begins to die off before edge of mask
- Spreading limits how close doped areas can be made
- Here assuming no implant through mask (not always true)

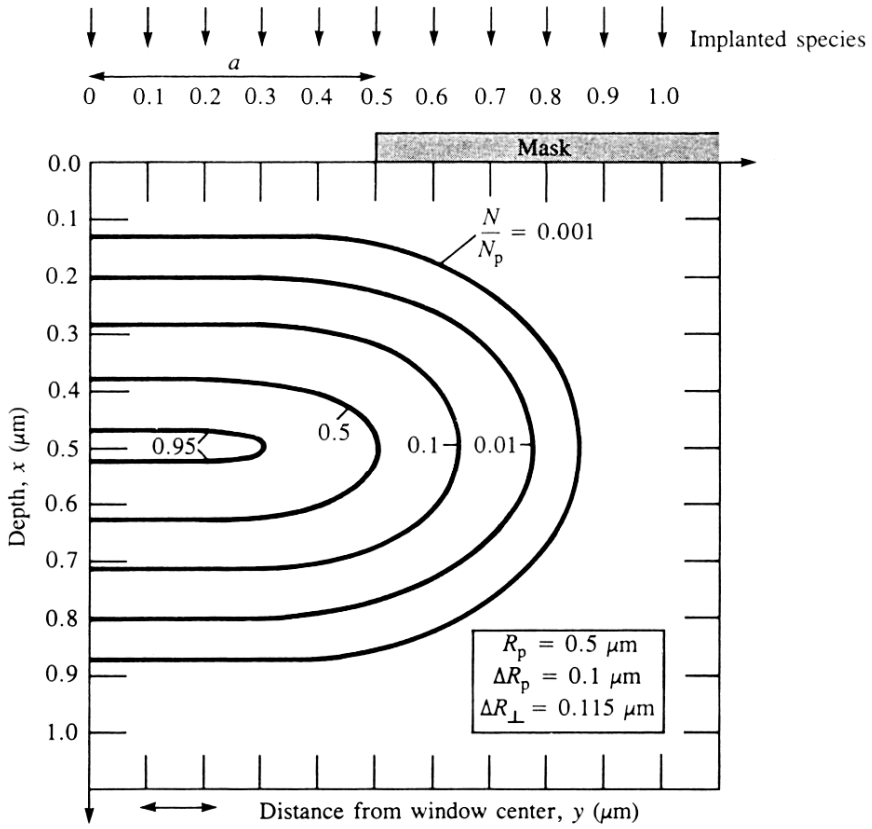


Fig. 5.4 Contours of equal ion concentration for an implantation into silicon through a 1-μm window. The profiles are symmetrical about the x-axis and were calculated using eq. (5.4), which is taken from ref. [4].

Table 9-1 Ion implantation characteristics of common silicon dopants

Ion	Isotopes: Weight (amu)	Isotopes: Abundance (%)	Range and straggle (nm): At 30 eV R_P	At 30 eV ΔR_P	At 30 eV $\Delta R_\perp$	At 100 eV R_P	At 100 eV ΔR_P	At 100 eV $\Delta R_\perp$	$\Delta R_P/\Delta E$ (approx.) (nm keV^{-1})
B^+	10.01	19.78	106.5	39.0	46.5	307	69.0	87.1	3.1†
	11.01	80.22							
P^+	30.97	100	42.0	19.5	16.9	135	53.5	47.1	1.1
As^+	74.92	100	23.3	9.0	6.4	67.8	26.1	18.7	0.6
Sb^+	120.90	57.25	20.8	6.2	4.6	50.7	15.8	10.8	0.45
	122.90	42.75							

† Boron range varies sublinearly with energy above about 100 eV.

Implant Penetration through Mask

- Implant has dopant profile in mask but for mask material
- Note resist much less stopping power than oxide
- May result in penetration below mask: get tail of Gaussian
- Two important issues for penetration through mask
- $N(x_0)$ (at the silicon surface) must be $<N_B$ – wafer background
- Otherwise get junction at the surface
- Also total Si dopant must be small fraction of Q (typically <0.1%)
- Calculate using (when $x_0 > R_p$)

$$Q(> x_0) = \frac{Q}{2} erfc\left[\frac{(x - R_p)}{2(\Delta R_p)}\right]$$

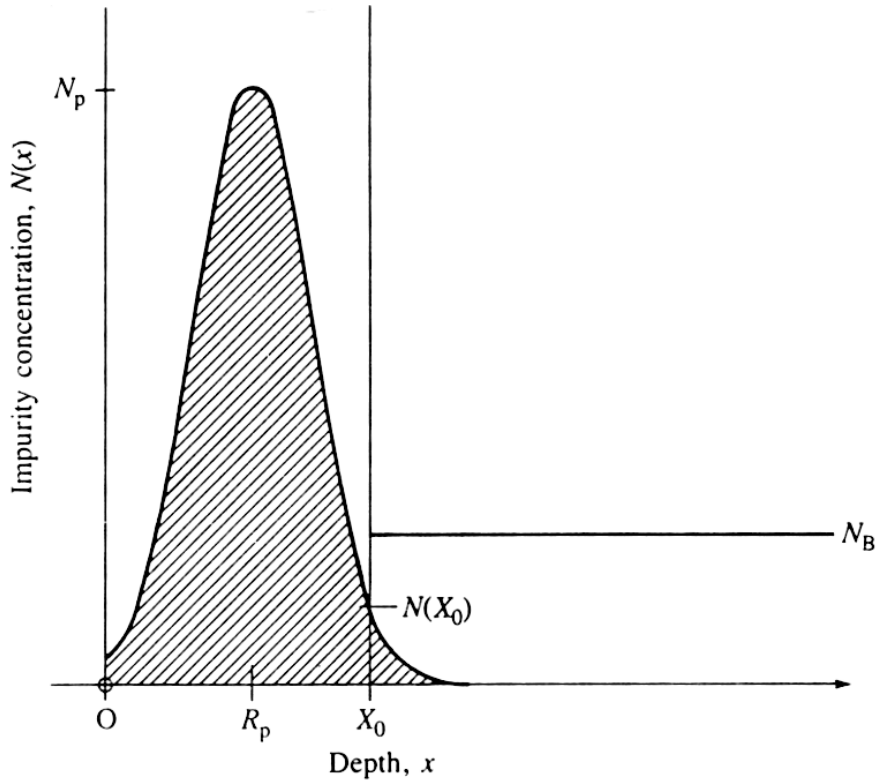
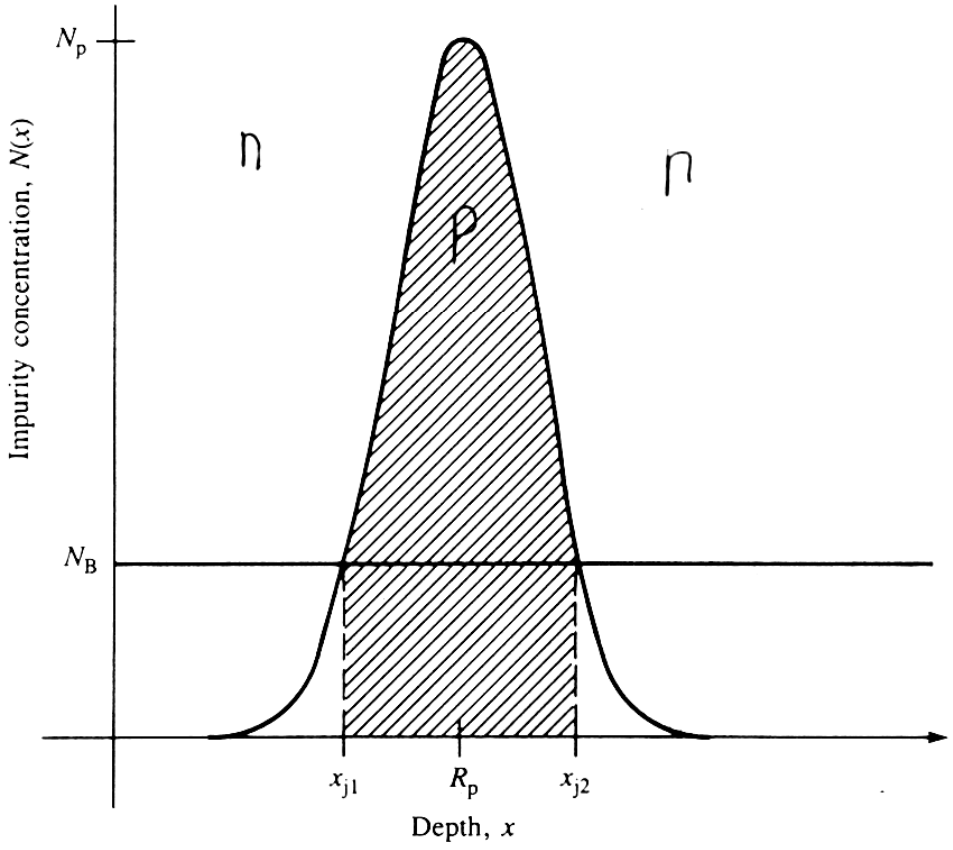


Fig. 5.5 Implanted impurity profile with implant peak in the oxide. The barrier material must be thick enough to ensure that the concentration in the tail of the distribution is much less than N_B.

Buried Junctions with Implant

- Peak implant dopant is not at surface
- Thus can get n p n junctions with 1 implant
- Junction where implant falls below background N_b



ig. 5.6 Junction formation by impurity implantation in silicon. Two *pn* junctions are formed t x_{j1} and x_{j2}.

Implant Variation with Crystal Angle

- <110> axis has holes in structure
- Called Channeling of dopant
- Solved by putting off axis implant

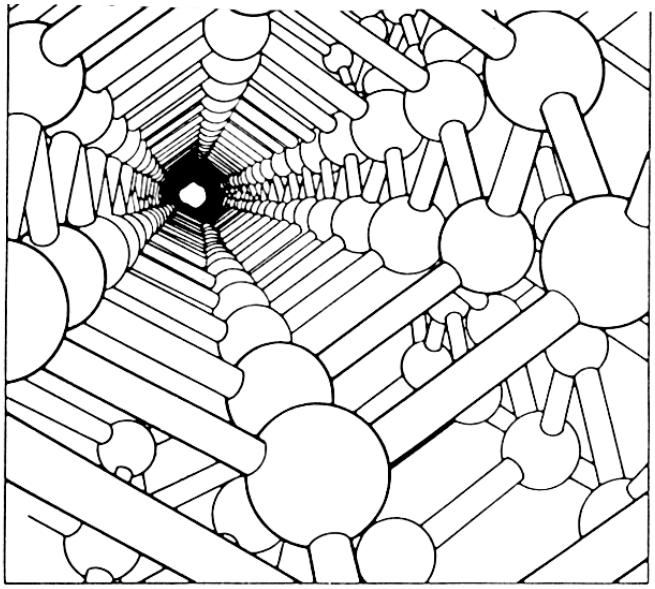


Fig. 5.7 The silicon lattice viewed along the ⟨110⟩ axis. From THE ARCHITECTURE OF MOLECULES by Linus Pauling and Roger Hayward. Copyright © 1964 W. H. Freeman and Company. Reprinted with permission from refs. [3a] and [3b].

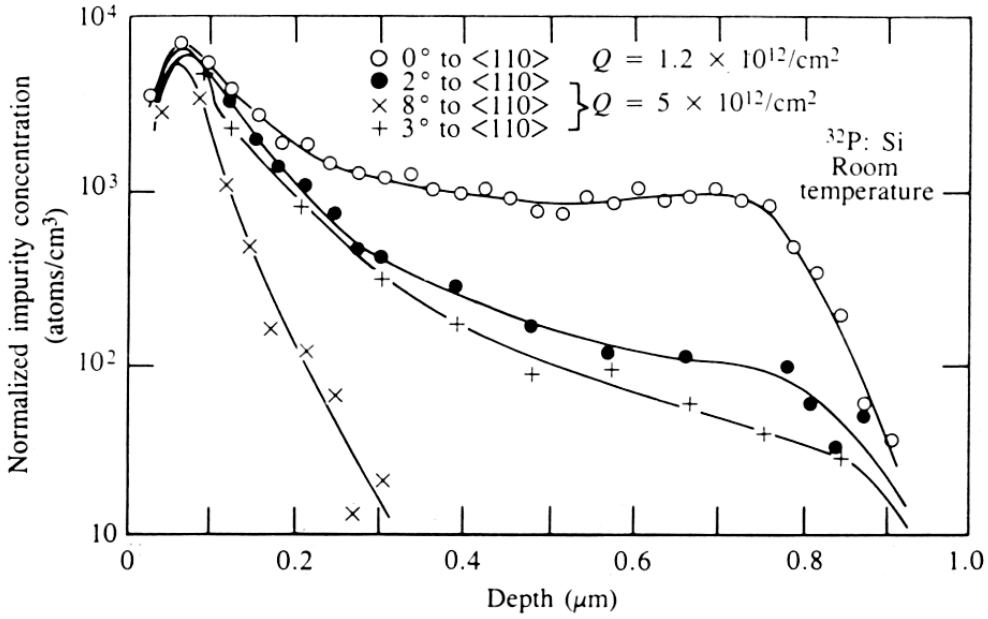


Fig. 5.8 Phosphorus impurity profiles for 40-keV implantations at various angles from the ⟨110⟩ axis. Copyright 1968 by National Research Council of Canada. Reprinted with permission from

Dopant Depth with Implanter Voltage

- Higher implant voltages: greater depth
- Note deviation from true Gaussian:
- Light ions (eg Boron) backscatter from Si
- More dopant on surface side than with Gaussian
- Heavy ions (eg. Arsenic) forward scattered (more As deeper)

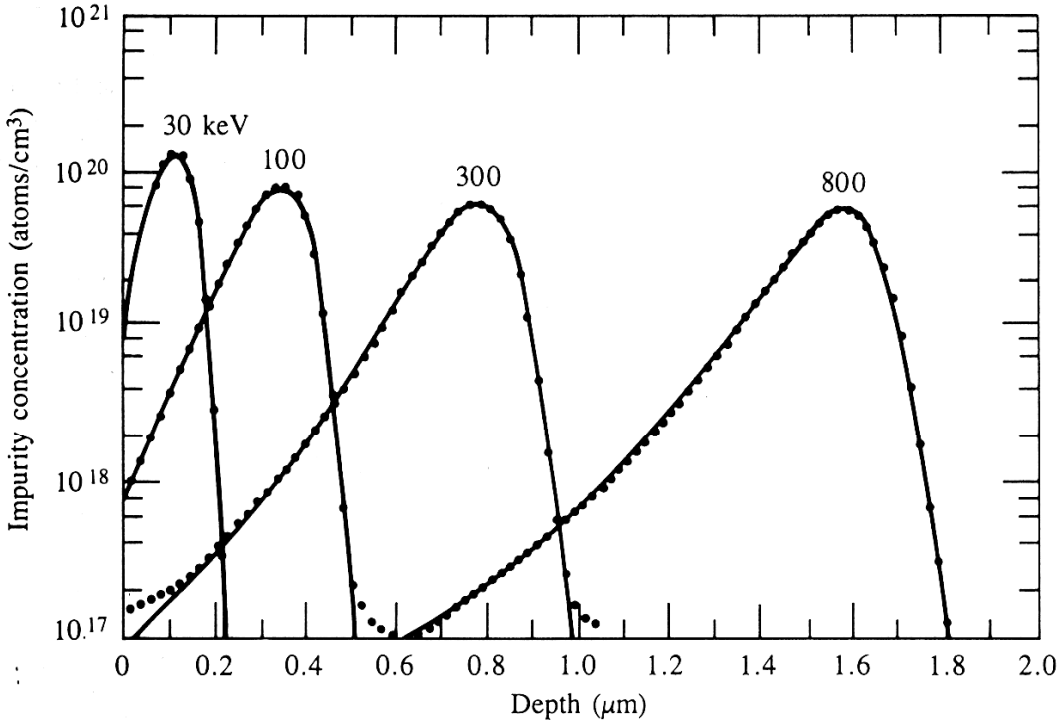


Fig. 5.10 Measured boron impurity distributions compared with four-moment (Pearson IV) distribution functions. The boron was implanted into amorphous silicon without annealing. Reprinted with permission from Philips Journal of Research.[8]

Calculation of Implant Effect

- Use Monte Carlo method to show ion spread
- Trace path of single ion as moves through crystal
- Random process included
- Launch a few million ions and measure final distribution
- eg program: Pearson Type IV distributions

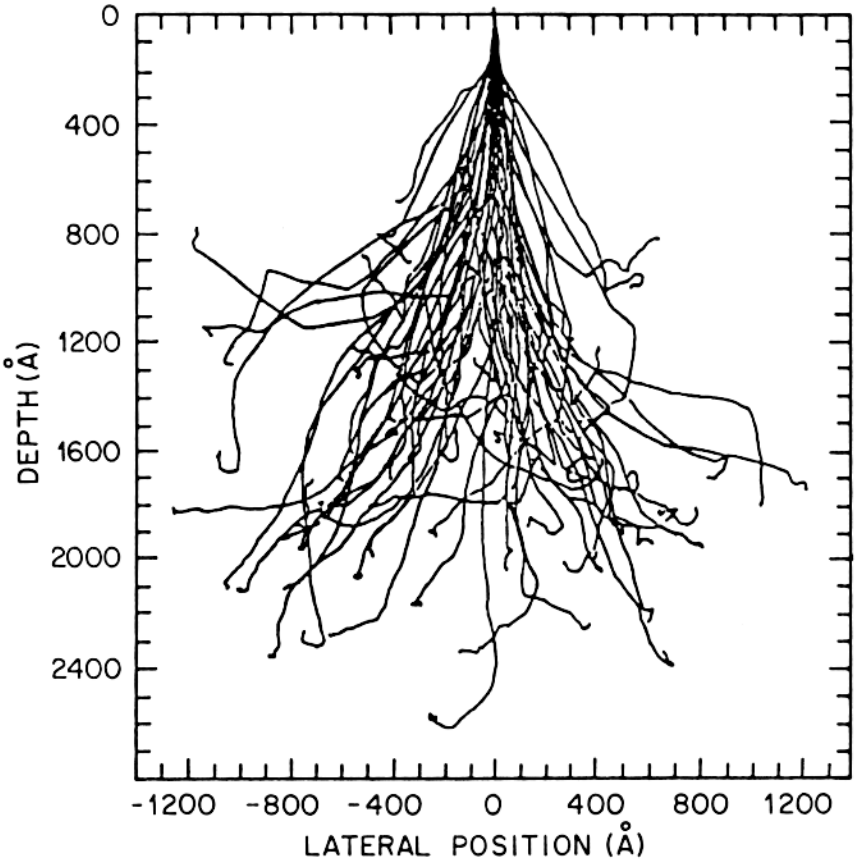


FIGURE 1
Monte Carlo calculation of 128 ion tracks for 50 keV boron implanted into silicon.

Crystal Damage of Implant

- Low does: only local damage – little effect on crystal
- Medium does: large damage at ion point and in path
- High dose: destroys crystal structure of silicon
- Increasing implants, increasing damage
- Damage areas reduce carrier velocity, create traps
- Gives poor semiconductor device characteristics

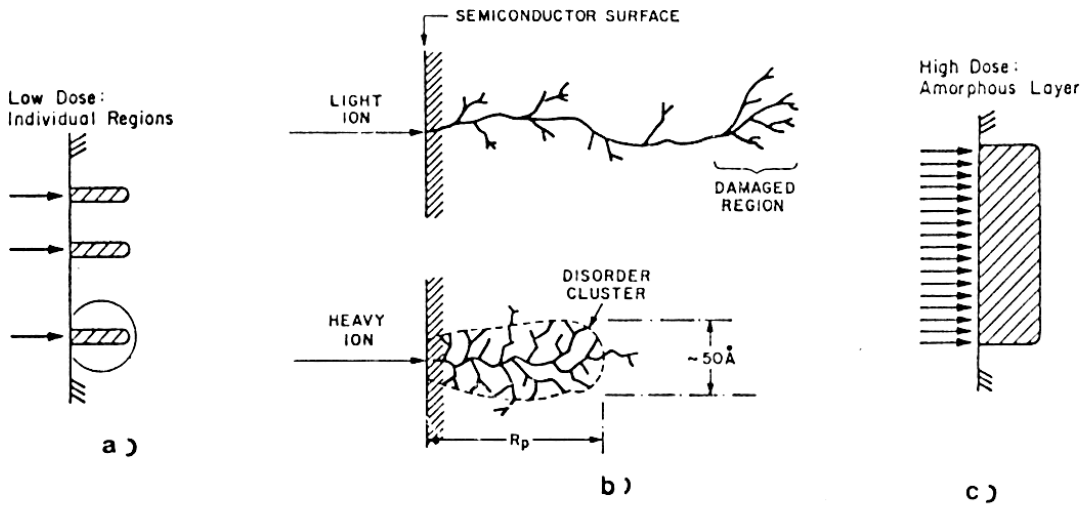


Fig. 16 Schematic representation of the disorder produced by ion implantation. (a) Low dose; (b) light ions - individual regions with degree of disorder increasing as ions penetrate deeper into substrate, heavy ions - individual regions of more uniform disorder along entire ion trajectory. (c) Heavy doses - formation of amorphous layer.

Implant Crystal Damage

- Implant badly damages crystal
- Can turn single crystal Si into amorphous film
- Reduced by heating target - anneals out damage
- Also remove damage by raising crystal temperature after implant

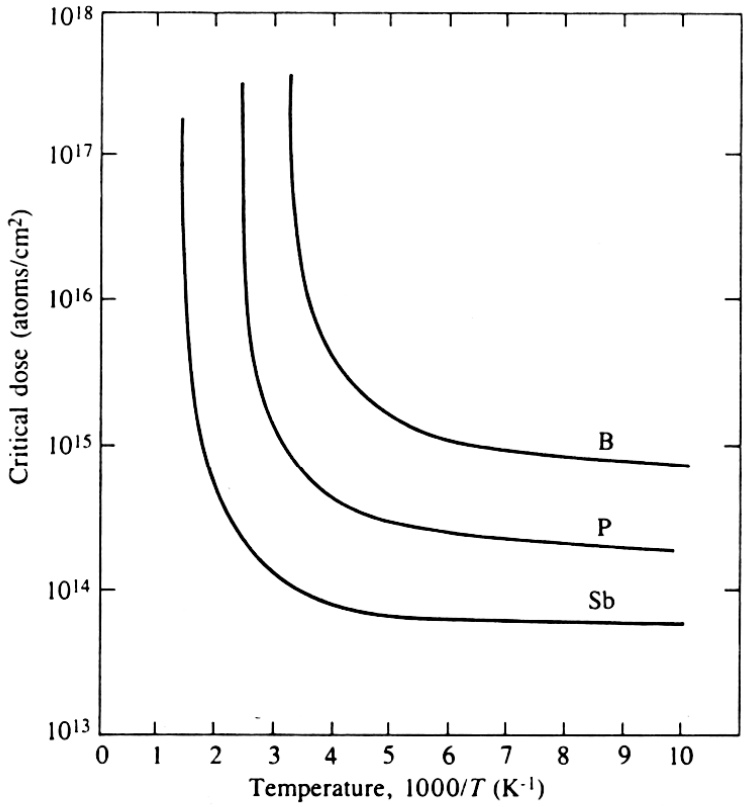


Fig. 5.9 A plot of the dose required to form an amorphous layer on silicon versus reciprocal target temperature. Arsenic falls between phosphorus and antimony. Copyright 1970 by Plenum Publishing Corporation. Reprinted with permission from ref. [6].

Ion Implant and Dopant Locations

- Recall dopant atoms must be substitutional: for activation
- Ion implant tends to create Interstitial dopant: pushes out Si
- Interstitial mplant ions do not contribute carriers
- True Interstitial dopant atoms: not activated

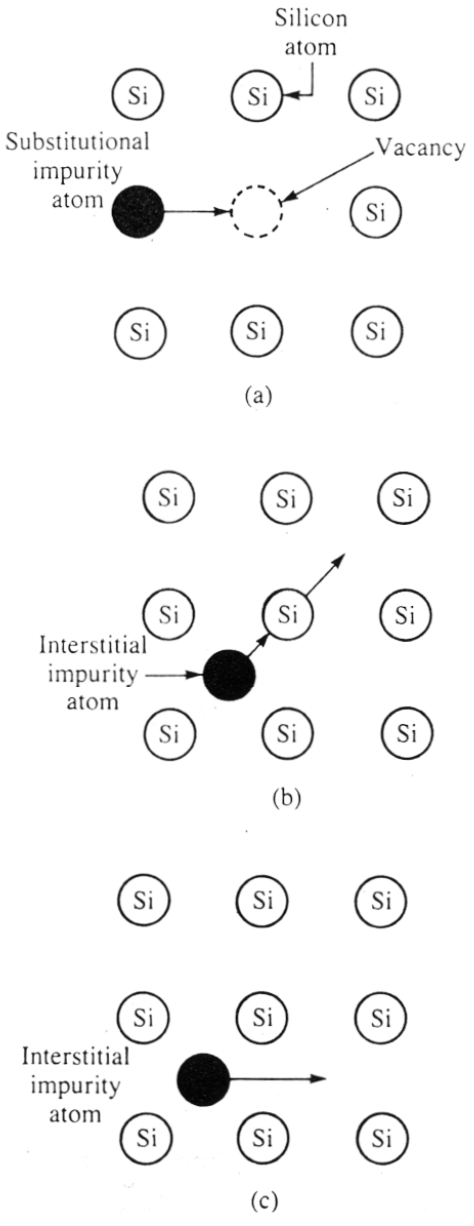


Fig. 4.1 Atomic diffusion in a two-dimensional lattice. (a) Substitutional diffusion, in which the impurity moves among vacancies in the lattice; (b) interstitialcy mechanism, in which the impurity atom replaces a silicon atom in the lattice, and the silicon atom is displaced to an interstitial site; (c) interstitial diffusion, in which impurity atoms do not replace atoms in the crystal lattice.

Annealing Damage & Activating Dopants

- Need to heat surface to remove damage & activate dopant
- As implant level increases activation ratio decreases
- Heat moves dopant atoms into substitution positions - activates
- By $10^{14}/cm^2$ less than 10% activated at implant
- Hence heating needed to activate
- Must reach a critical temperature ~800-900°C

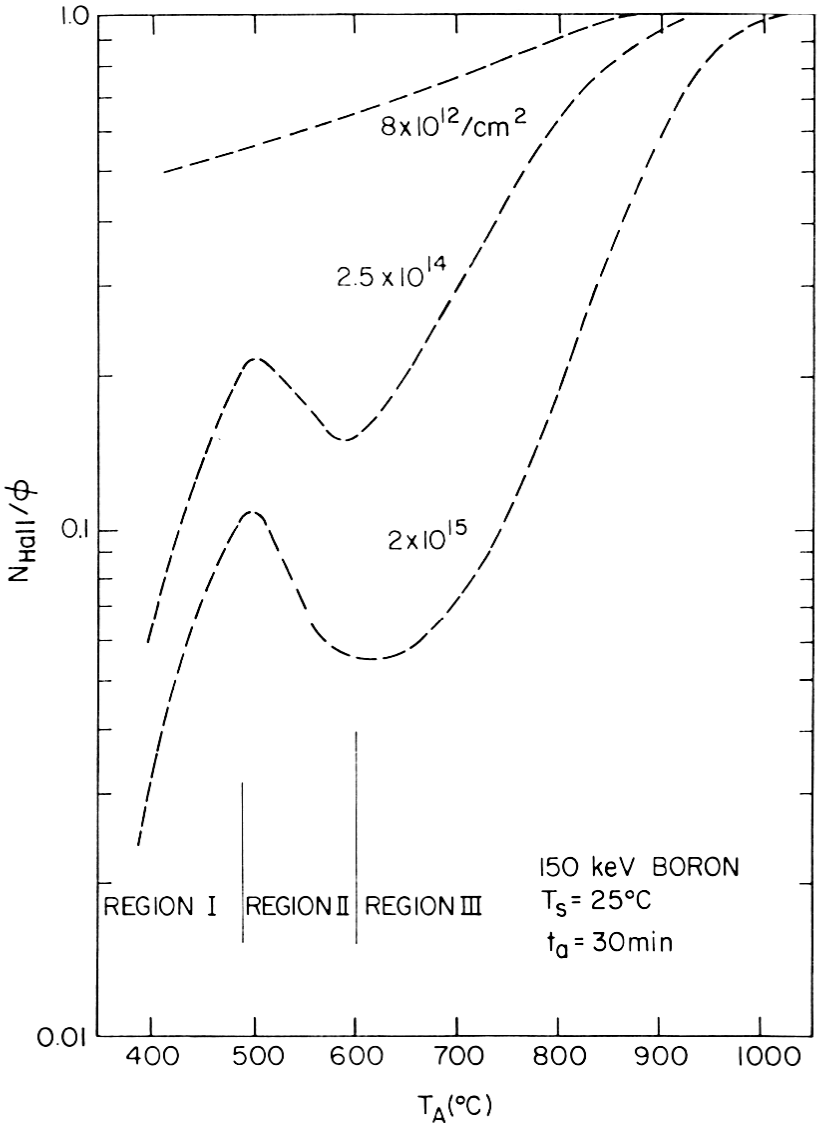


FIGURE 25
Isochronal annealing of boron. The fraction of activated dopant is plotted against anneal temperature for different implant doses. (*After Seidel and MacRae, Ref. 42.*)

Implant Activation Defect Healing

- Heating to remove crystal electrical damage - Primary Damage
- At low implants done in a furnace
- Dopant activation second requirement
- Problem: High temperature cause dopant to diffuse
- Thus activation changes dopant profiles!
- Became real problem in sub micron devices

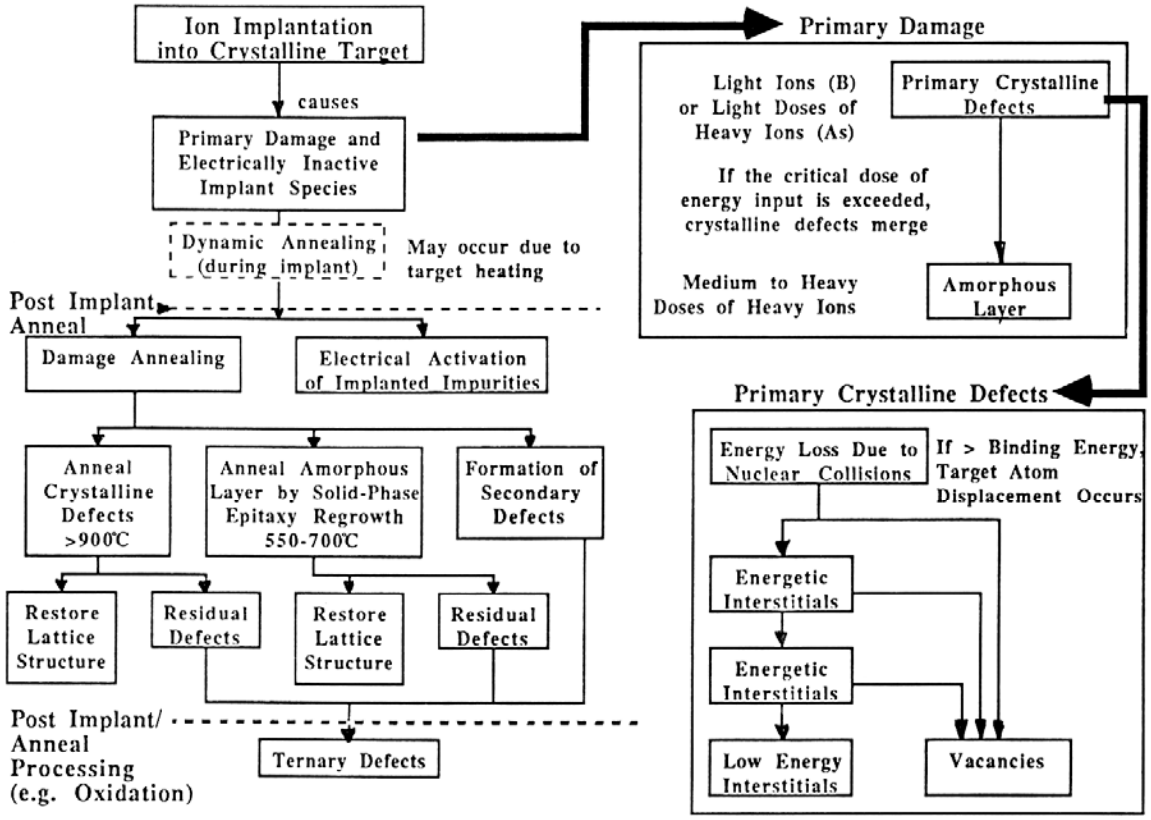


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Fig. 15 Ion implantation damage and annealing.

Implant Activation Defect Healing

Rapid Thermal Annealing

- Furnace activation moves dopant around: changes profile
- Use high intensity light to heat only dopant surface
- Light penetrates only few microns thus heats only surface
- Reach high local temperature: rapid healing/activation
- Rapidly cools when light off – wafer itself is cool
- Little chance for dopant diffusion

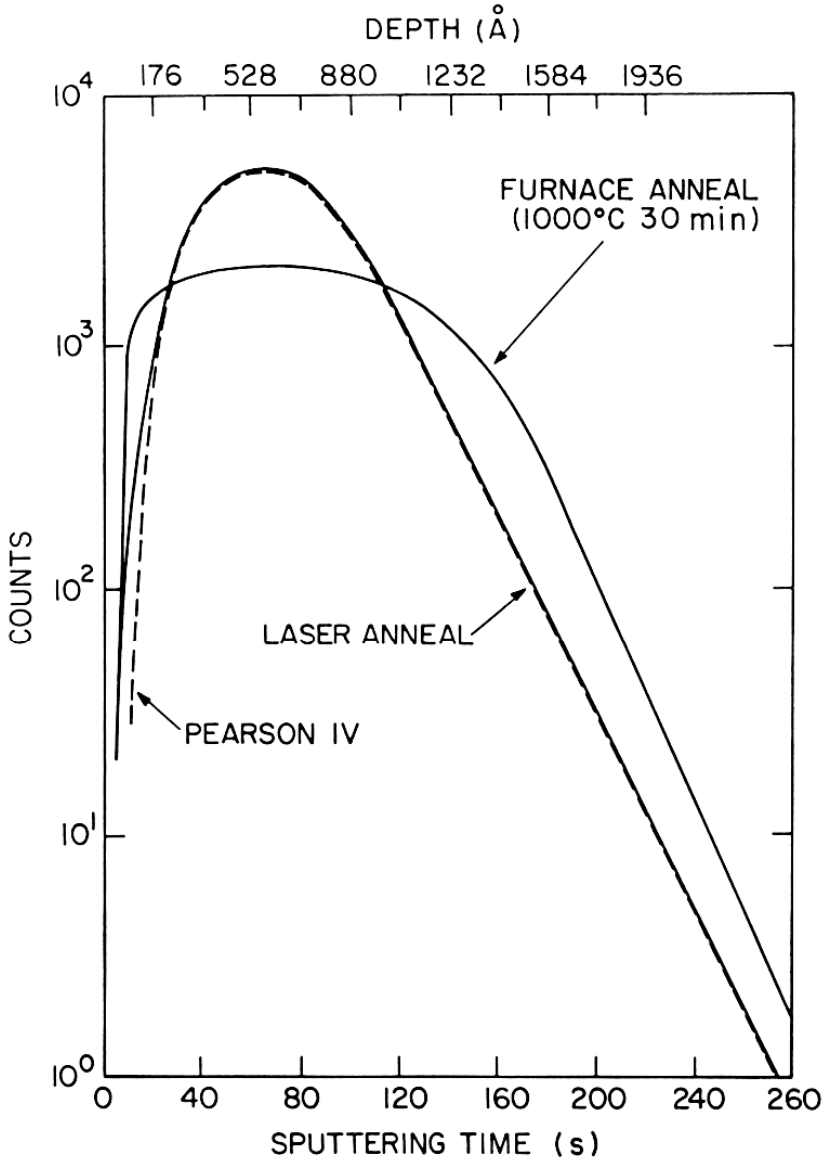


FIGURE 27
Comparison of annealed profiles using furnace and scanned-laser RTA methods. Laser annealing activates the dopant without significant diffusion. (*After Gat et al., Ref. 46.*)

Rapid Thermal Annealing Systems

- Lasers expensive, heat small area
- Instead use array of Halogen Heat Lamps
- Raises temperature of whole surface in seconds
  Can actually melt wafer surface
- Water cool back of target
- As only heat surface (not whole wafer) cools quickly

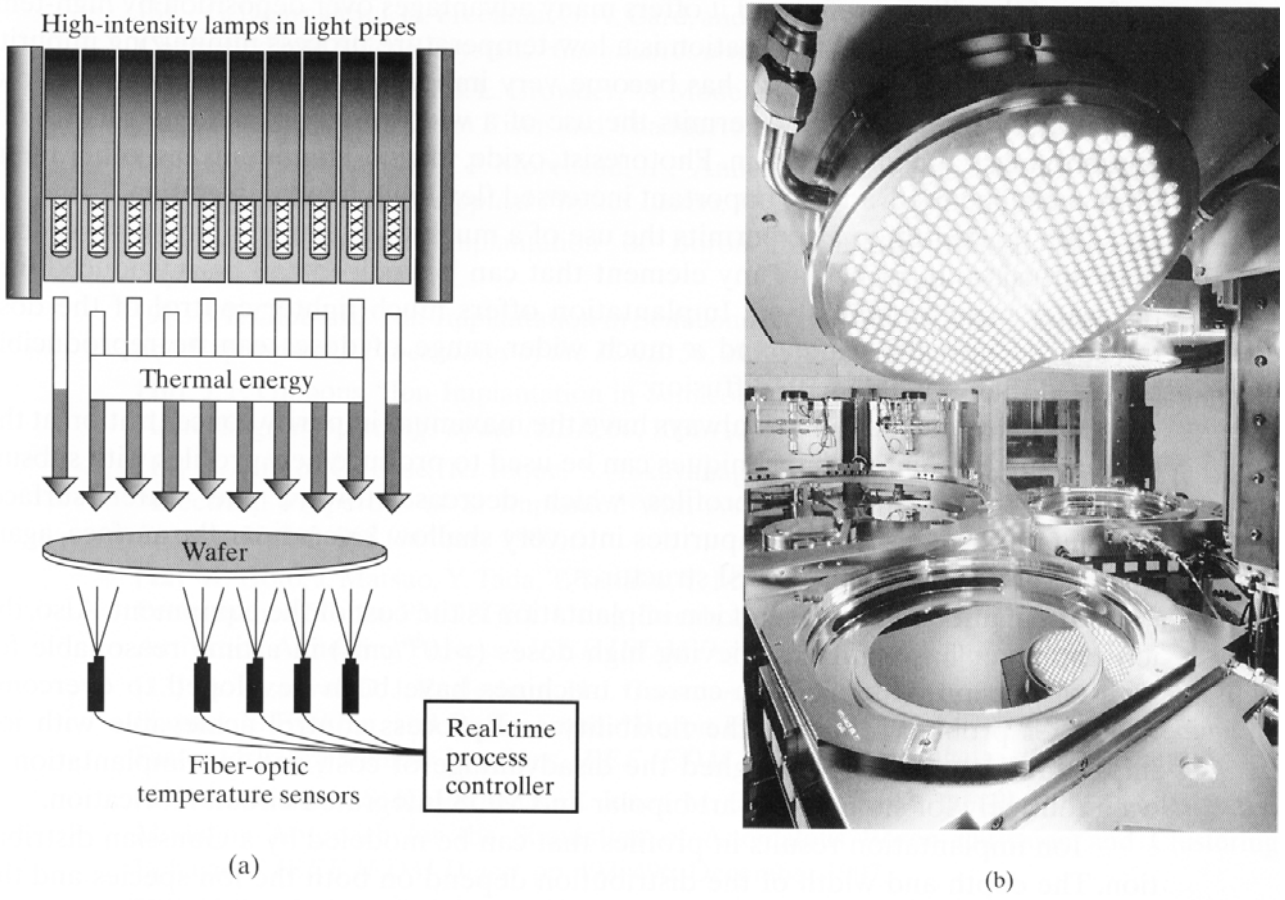
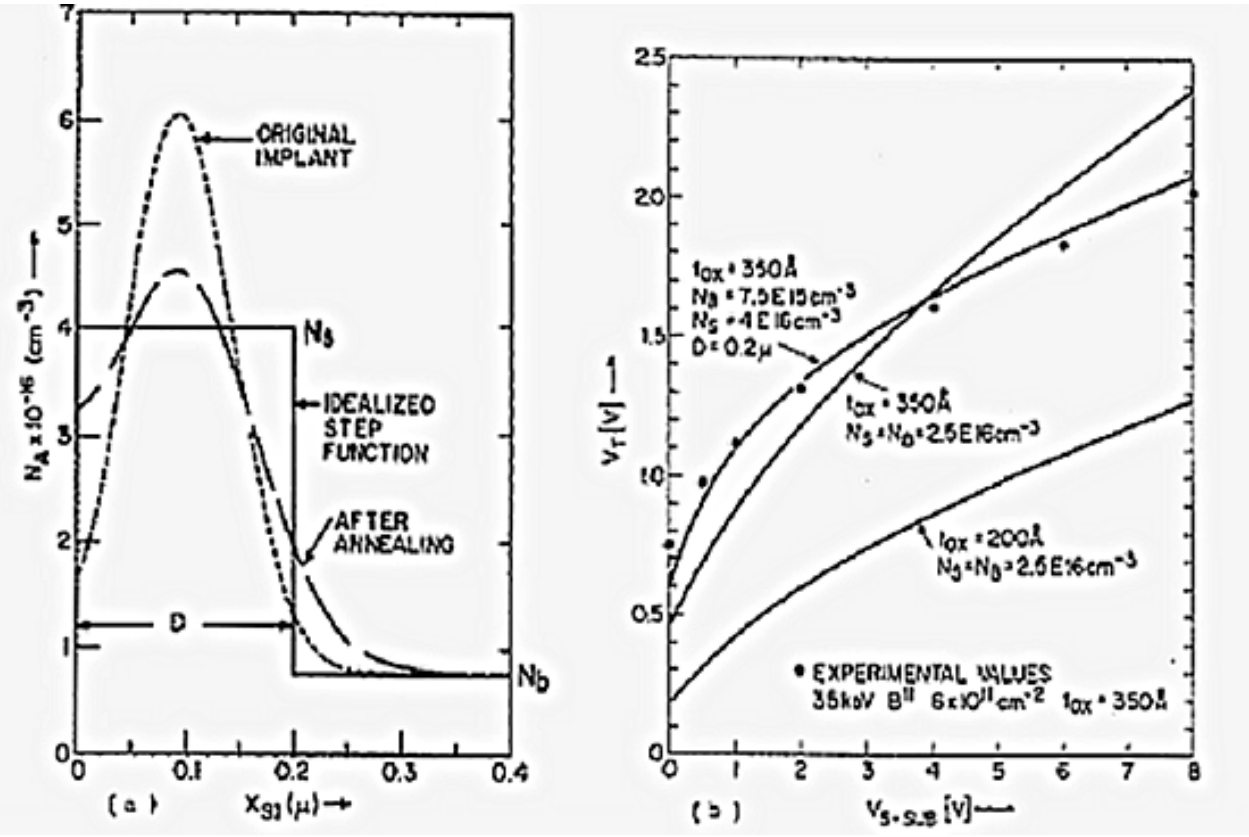


FIGURE 5.12

(a) Concept of a rapid thermal processing (RTP) system. (b) Applied Materials 300 mm RTP System. (Courtesy Applied Materials, Inc.)

Dopant Movement in Later Processes

- All later thermal processes change dopant positions
- Any thermal processe causes diffusion
- Hence must adjust profile to take into account later processes
- Called process integration



Oxidation Dopant Segregation

- Furnace oxidization changes dopant profile
- Oxidation causes N dopant to pile up at surface
- Oxidation: P dopant depletion because dopant move into oxide

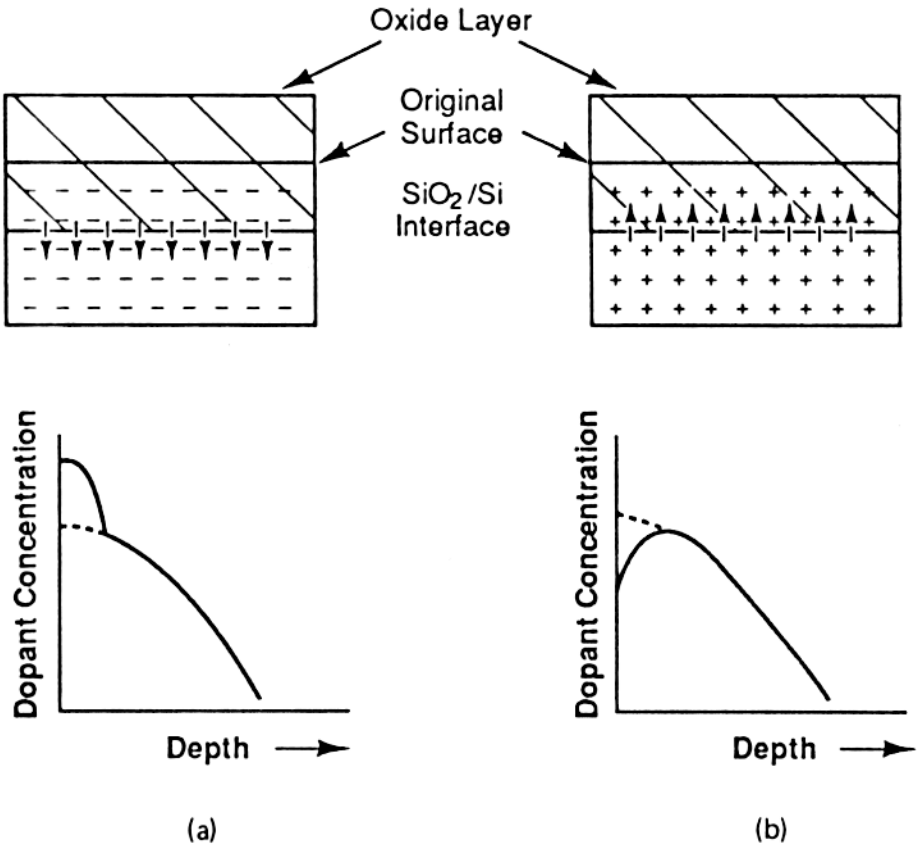
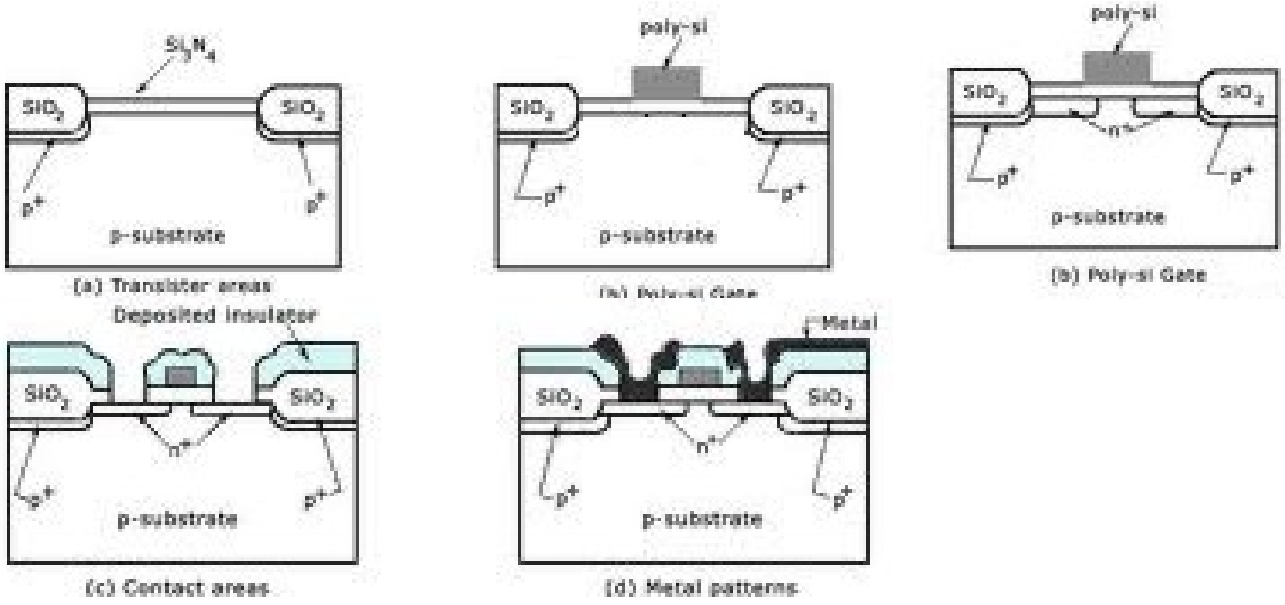


Figure 11.26 Pile-up and depletion of dopants during oxidation. (*a*) Pile-up of N-type dopants; (*b*) depletion of P-type dopants.

Silicon Etching (Ruska Ch. 6)

- Silicon etching important: for micromachining and IC's
- CMOS requires Poly Crystalline Silicon as a conductor
- Called Poly Si
- Modest resistance conductor depending on doping
- Usually highly doped silicon
- Poly Silicon etches similar to single crystal Si
- Changes depend on crystal size and doping
- Poly gate conductor creates self aligned process
- Deposit and define the gate on the gate insulator
- Gate creates the mask to position source/drain implant
- Now source & drain aligned to gate – self aligned
- Older processes – gate deposed after source/drain
- Hard to align gate to channel – poor transistor characteristics

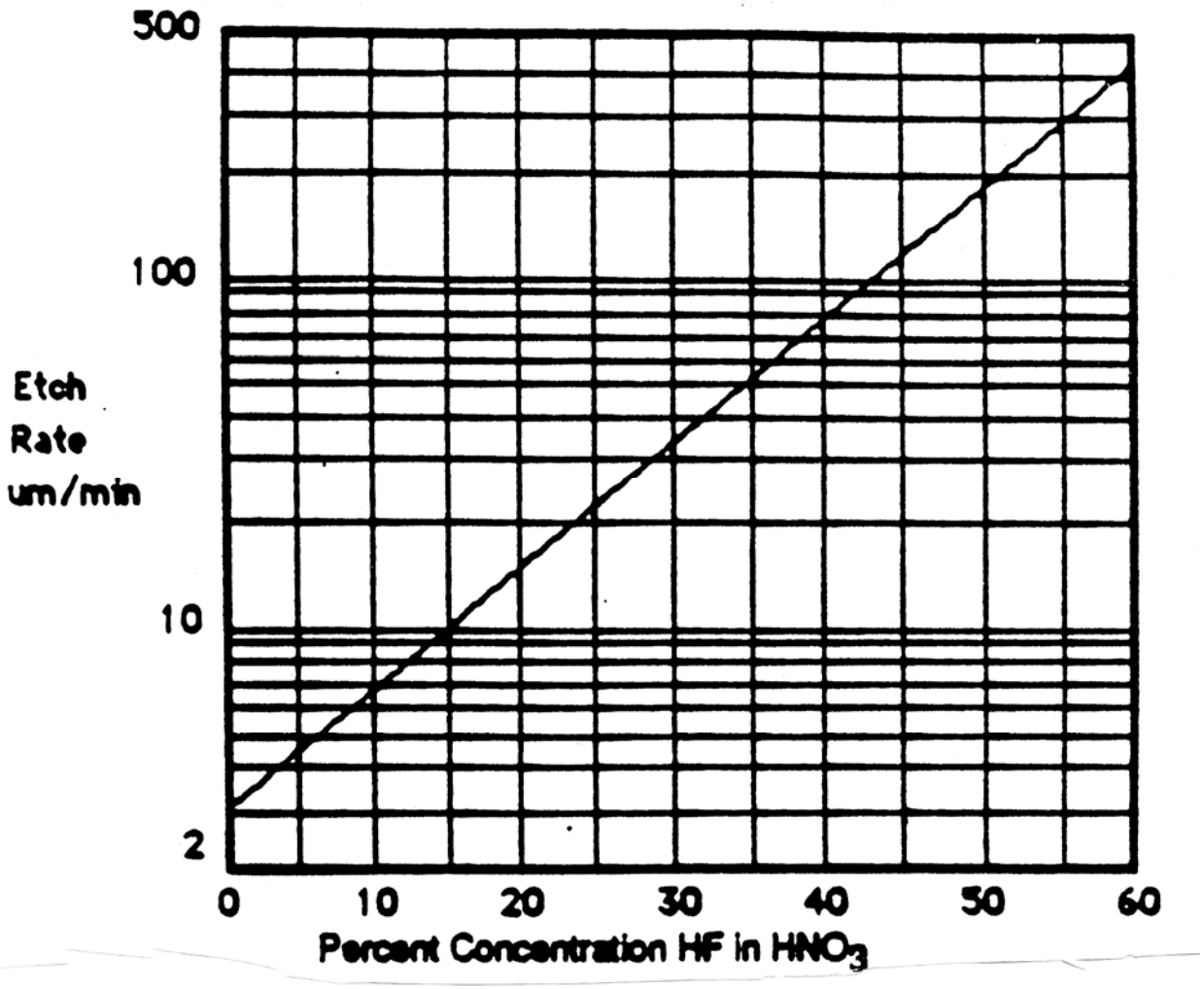


Etching Silicon

- Typical etch: HF and HNO_3 (nitric acid) combination
- Oxidation/reduction reaction
- Nitric oxidizes the silicon
- HF removes the oxide formed

$$3Si + 4\ HNO_3 + 18HF \rightarrow 3H_2SiF_6 + 4\ NO + 8H_2O$$

- Ratio of HF/Nitric set etch rate



Typical Isotropic Silicon Etches

- Typically dilute with Acetic acid CH_3COOH
- Reduces the etch rate

2A. Isotropic Silicon Etches

Table 16

	Formula	Comments
1	HF, HNO_3	See diagram
2	HF, HNO_3, H_2O or CH_3COOH	Various combinations give different etch rates
3	900 ml HNO_3, 95 ml HF, 5 ml CH_3COOH, 14g $NaClO_2$	15 um/min
4	745 ml HNO_3, 105 ml HF, 75 ml CH_3COOH, 75 ml $HClO_4$	170 A/sec
5	50 ml HF, 50 ml CH_3COOH, 200 mg $KMnO_4$ (fresh)	Epi Etching 0.2 um/min
6	108 ml HF, 350g NH_4F per L H_2O	Epi Etching n type 0.2-0.6 ohm-cm; 0.43 A/min p type 0.4 ohm-cm; 0.45 A/min p type 15 ohm-cm; 0.23 A/min

Diluted HF/Nitric/Acetic

- Etch rates depend on dilution

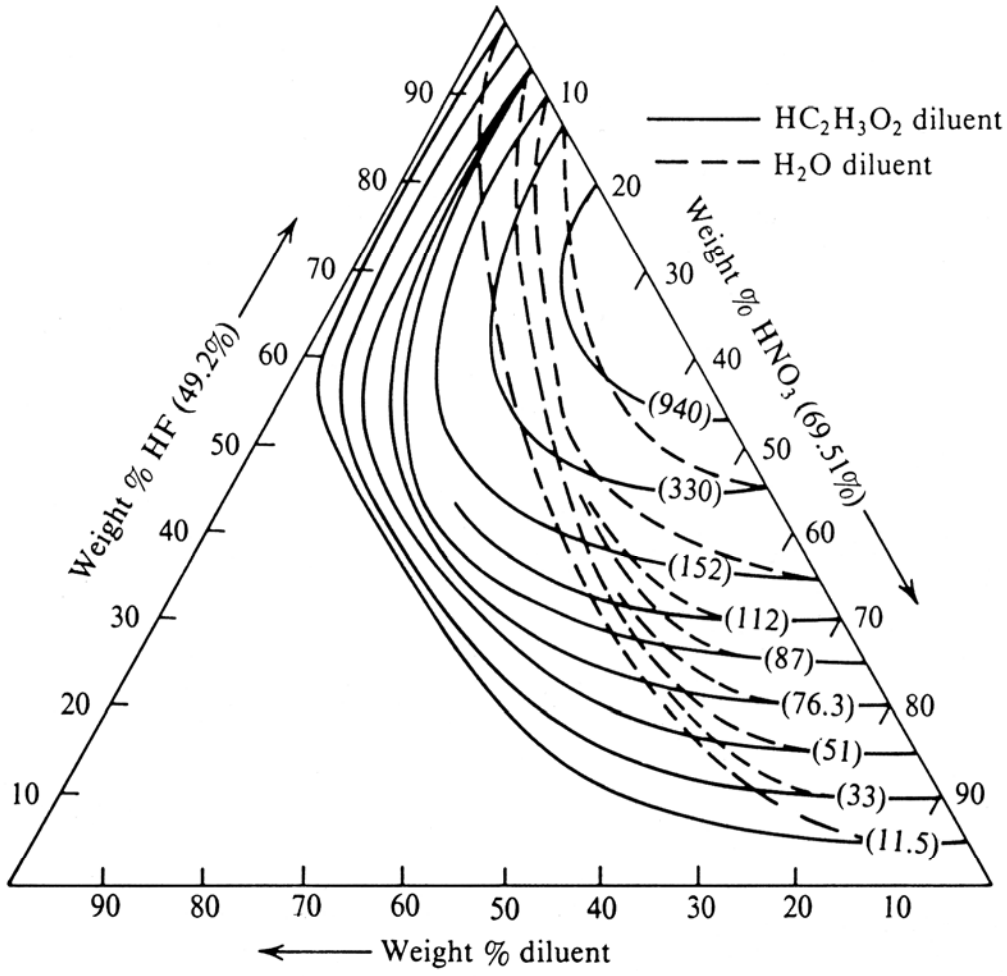


Figure 6-8 Etch rates for single-crystal silicon as a function of HF, HNO_3, and diluent concentrations. These etch rates are for dual-sided etching and must be divided by 2 to obtain the etch rate on a single surface. (*Reference 8. Reprinted by permission of the publisher, The Electrochemical Society, Inc.*)

Common PolySilicon Etches

- Similar to single crystal
- Must control etch rate

POLYSILICON ETCHES
Table 7

	Formula	Comments
1	Shipley remover 1112A	See Shipley data sheet
2	70.4% HNO_3, 28% H_2O, 1.4% HF	21°C
3	100 ml HNO_3, 40 ml H_20, 28 ml HF	8000 A/min
4	33 ml CH_3COOH, 26 ml $HN0_3$ 1 ml HF	1500 A/min
5	6 ml H_20_2, 10 ml NH_4F, 1 ml HF	2000 A/min
6	80% $HN0_3$, 20% HBF_4 1.0 g1l NH_4BF_4	20°C
7	IM solutions Tetramethylammonium Hydroxide	25-45°C

Anisotropic Etching of Silicon

- Etching that proceeds along crystalline planes
- typically <111> plane slowest
- <100> fastest (ratio 30:1 to 100:1)
- Used extensively in micromachining & power transistors
- <100> wafers get "V" groves
- <110> wafers get vertical side walls

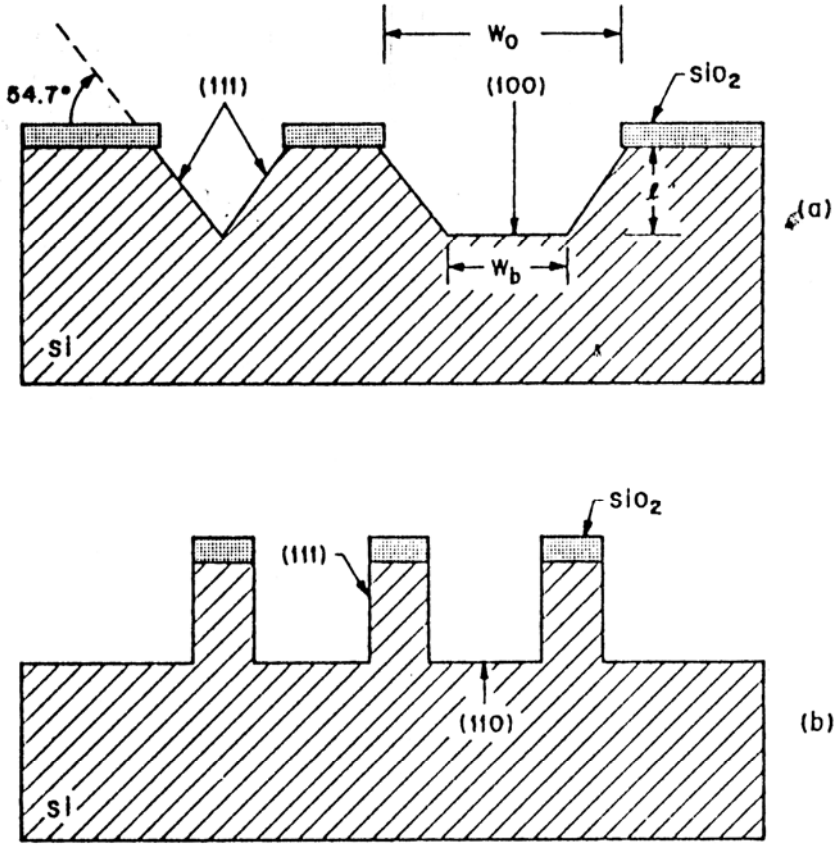


Fig. 14 Orientation-dependent Si etching (a) etch pattern profiles on <100>-Si, (b) profiles on <110>-Si[22]. (© 1978 IEEE).

Typical Anisotropic Etchants of Silicon

- EDP (Ethylenediamine Pyrocatecol & water) most common
- Advantages: attacks silicon, not oxide or aluminum
- Disadvantage: poisonous
- Potassium Hydroxide (KOH)
- Advantages: good crystal plane selectivity silicon
- Advantages: attacks aluminum

Table 6-2 Some formulations for crystallographically selective etching of silicon

Ingredients	Composition	Temperature (°C)	Relative rate 100	110	111	Absolute rate†	Reference
KOH in water/ isopropanol	19 wt. % KOH	80	—	*400*	1	0.59 μm sec^{-1}	9
N_2H_4/water	100 g/50 mliters	100	*10*	1	—	0.3	10
Ethylenediamine/ Pyrocatecol/ water	17 mliters 3 g 8 mliters	110	*50*	30	3	50	11

† Etch rate for fastest-etching orientation, i.e., the one italicized under relative rate.

Aluminum Multilayer Structures

- Aluminum most common conductor in CMOS
- Conductive and easy to deposit
- Easy to etch
- Used to make contacts to source/drain, gates
- Problem is in making multilevel structures
- Need to create intermetal insulator (typically glass)
- Must make contact between Al layers
- Aluminum grows a protective insulating oxide
- Just depositing one metal film on another does not make contact

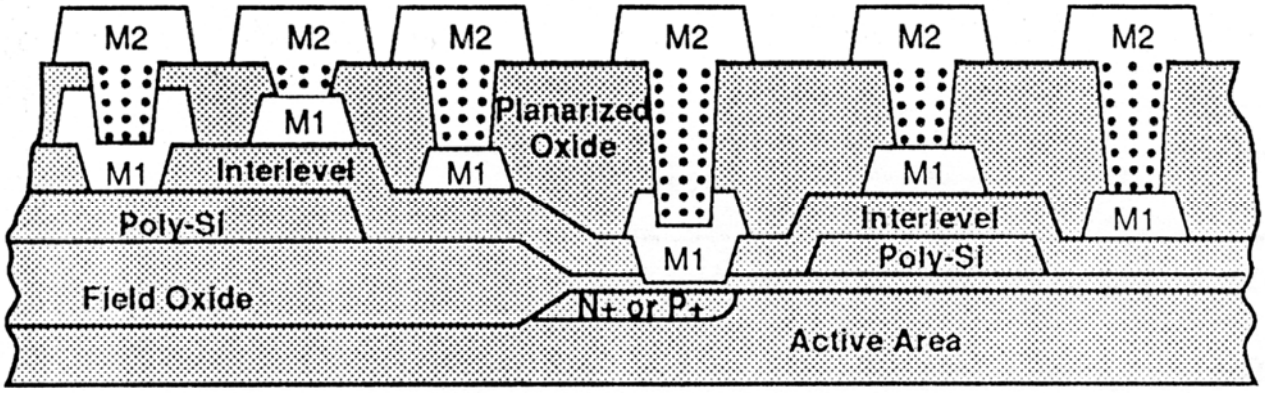
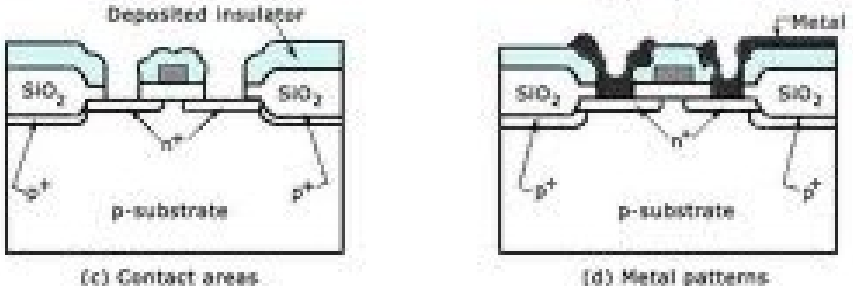
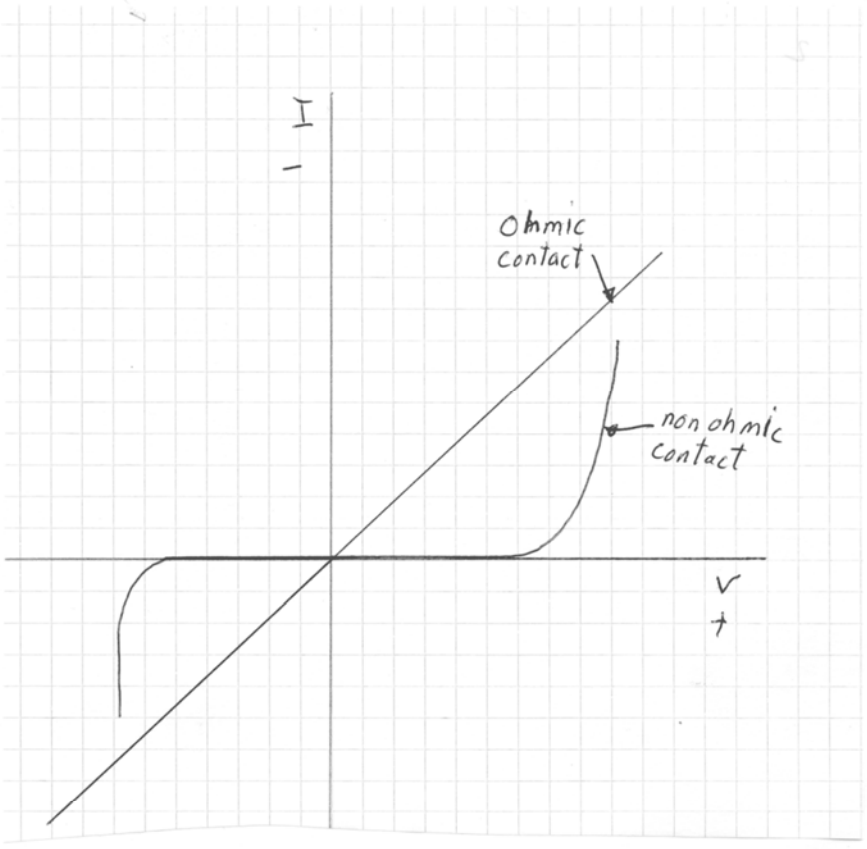


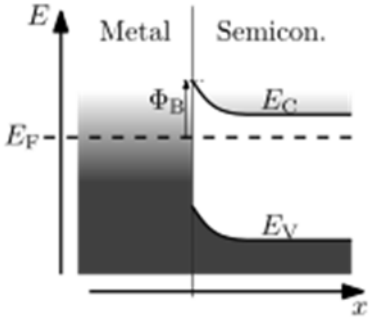
Figure 13.2 Cross section of typical planarized two-level metal VLSI structure showing range of via depths after planarization. (*Courtesy of Solid State Technology.*)



Ohmic Contacts

- Aluminum oxide can create diode like contacts
- Want a pure Ohmic contact (linear resistance)
- Most initial metal/Si are diode like Schottky diode contacts
- Caused by potential barrier of metal/semiconductor
- Often one directional (if 2 direction thin oxide barrier instead)
- Get this by sinter in dry nitrogen at end
- Typical 450ºC for 30 minutes
- Removes the oxide, creates ohmic contact





Aluminum Alloys

- Pure aluminum has reliability problems
- Sinter & high temperature creates difficulties
- Add Copper and Silicon
- Makes it much harder to etch

Table 1. PROPERTIES OF ALUMINUM AND ALUMINUM ALLOY THIN FILMS

Name	Symbol	Melting Point (°C)	Al /Si Eutectic (°C)	Density (g/cm^3)	Resistivity ($\mu\Omega$–cm)
Aluminum	Al	660	577	2.70	2.7
Aluminum/ 4% Copper	Al 4%Cu	650	~577	2.95	3.0
Aluminum/ 2% Silicon	Al 2%Si	640	~577	2.69	2.9
Aluminum/ 4% Copper 2% Silicon	Al 4%Cu 2%Si		~577	2.93	3.2

Aluminum Spike Through

- When Aluminum heated penetrates silicon
- Si moves in Al, Al into Si
- Get spikes which can short junctions
- Suppressed by adding 1-2% Si to Al

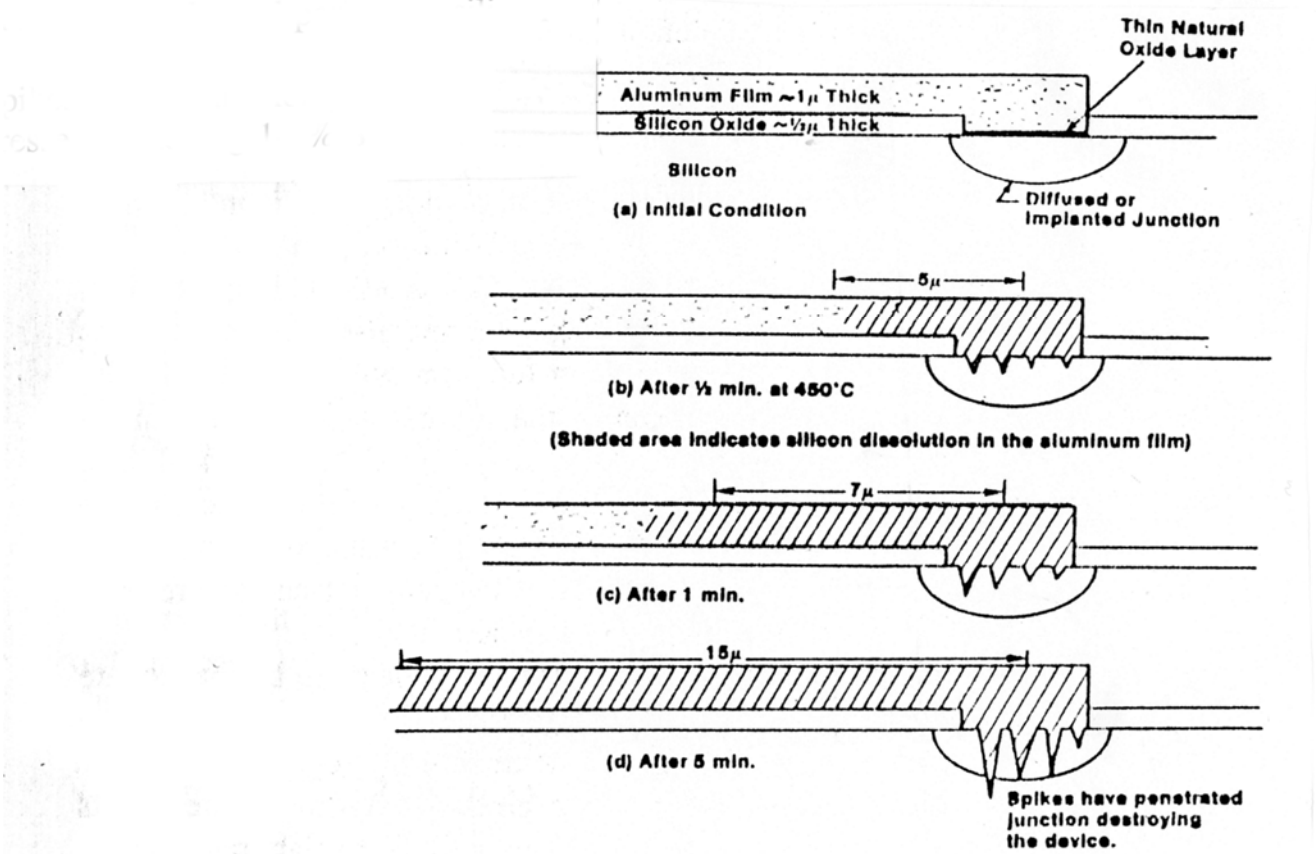


Fig. 2 Junction spiking and silicon migration during contact sintering.

Phase diagram

- Silicon 1.5% Aluminum Eutectic
- Lowest melting point alloy

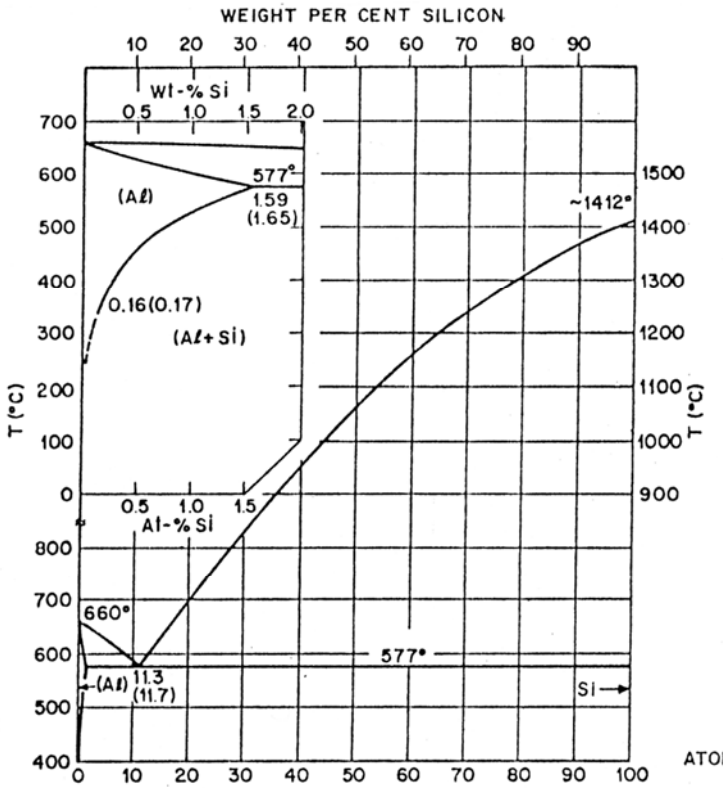


Fig. 1 Phase diagram of the aluminum-silicon system. From M. Hansen and A. Anderko, *Constitution of Binary Alloys*, 1958. Reprinted with permission of McGraw-Hill Book Co.

Preventing Spike Through

- Adding Si to Al prevents spikes
- Also put down Barrier metal layers
- Tungstan, Molybdenum most common
- Refractory metals

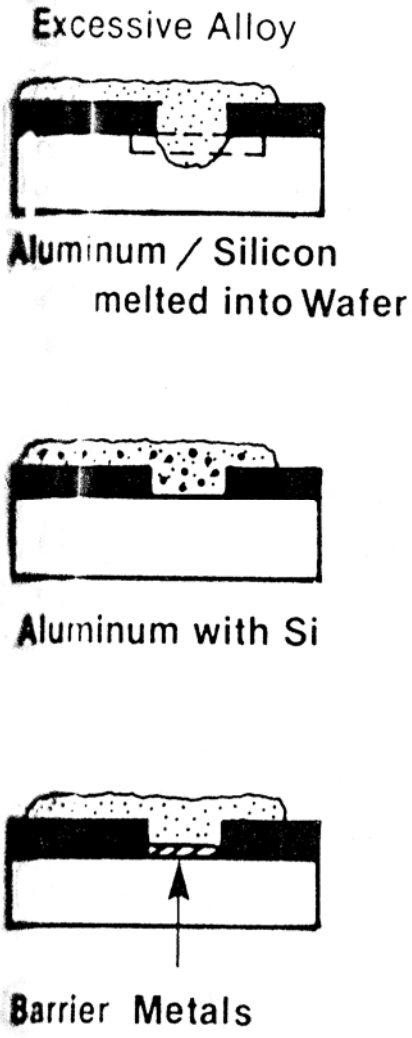


Figure 13.6 Eutectic alloying of aluminum and silicon contacts.

Aluminum and Hillocks

- When Al heated grows Hillocks
- Spikes up to 1 micron high!
- Can punch through intermetal glass layers
- Add copper to suppress
- Also for electromigration:
  tendency of metal to move when current applied
- Problem is Si/copper makes etching difficult

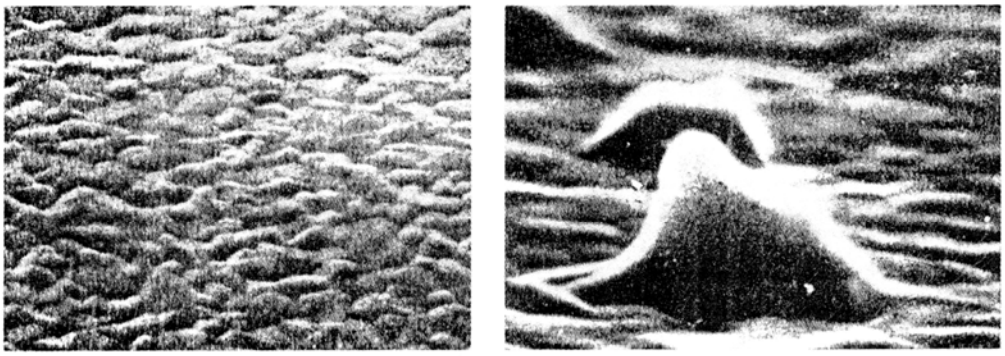
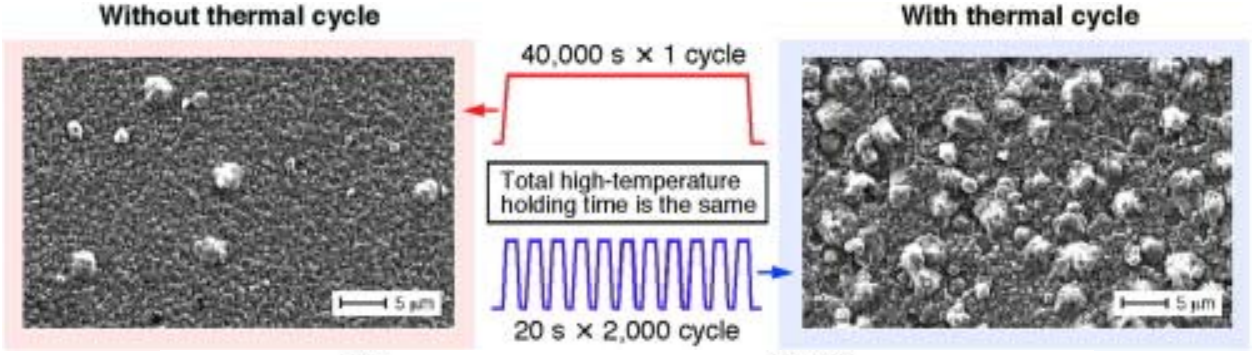
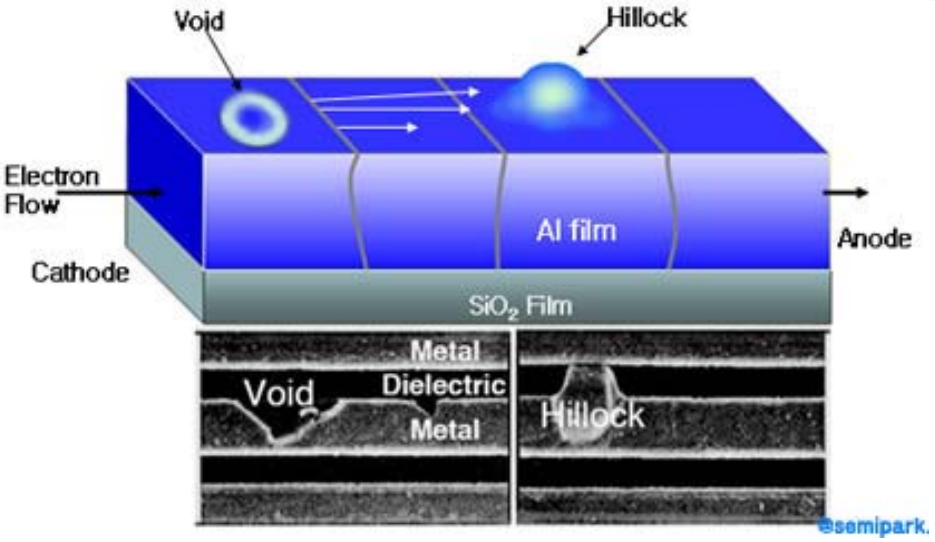


Fig. 36 Comparison of hillock-free and hillock containing films.





Aluminum Etching

- Oxidation: removal of electrons or ions from material

$$M \rightarrow M^{+} + e^{-}$$

- Reduction: addition of electrons to reactant
- Redox reaction: both oxidation and reduction
- Aluminum etches are redox reactions

$$6H^{+} + Al \rightarrow 3\ H_2 + Al^{3+}$$

- Must remove aluminum oxide for reaction

Typical Aluminum Etchants

- Most are Phosphoric Acid based (H_3PO_4)
- Acetic for dilution
- Note: without oxide Al would etch in water

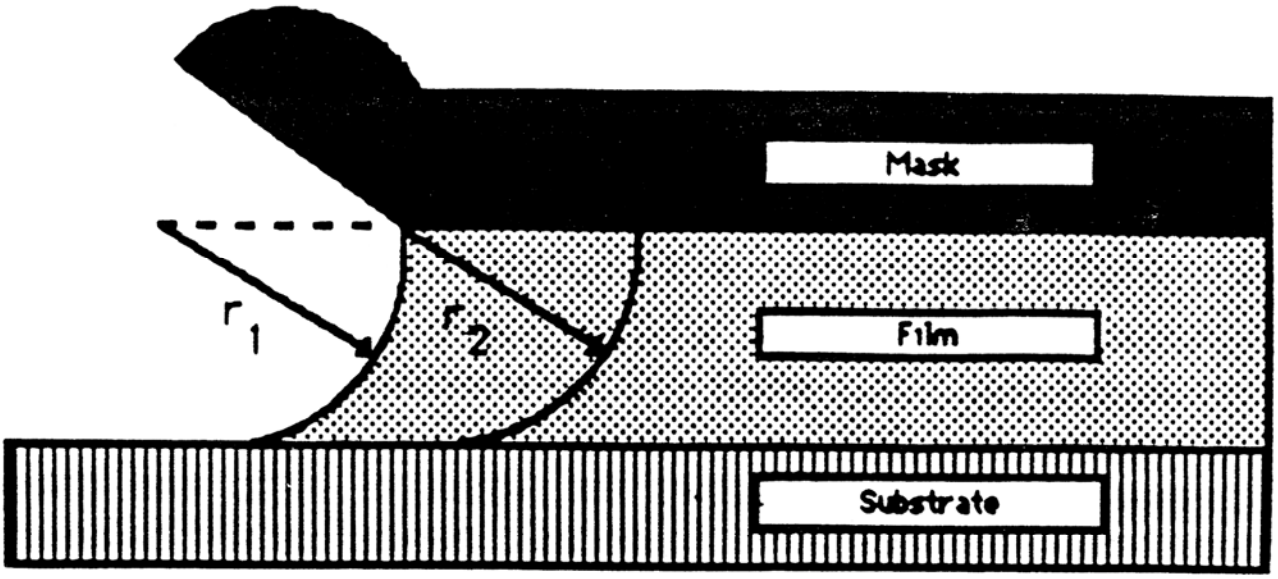
FORMULAS FOR ALUMINUM ETCHING

Table 11

	Formula	Comments
	Phosphoric Acid Based Solutions	
1	77 ml H_3PO_4, 20 ml CH_3COOH, 8 ml HNO_3	40 - 60°C
2	73 ml H_3PO_4, 3.5 ml CH_3COOH, 4 ml HNO_3, 19.5 ml H_20	40 - 60°C
3	90 ml H_3PO_4, 5 ml HNO_3, 5 ml H_20	40 - 60°C
4	80 ml H_3PO_4, 5 ml CH_3COOH, 5 ml HNO_3, 10 ml H_20	40 - 60°C
5	80 ml H_3PO_4, 5 ml HNO_3, 15 ml H_20	40 - 60°C
6	40 ml H_3PO_4, 40 ml CH_3COOH, 10 ml HNO_3, 10 ml H_20	40 - 60°C
7	75 ml H_3PO_4, 5 ml HNO_3, 20 ml H_20	40°C

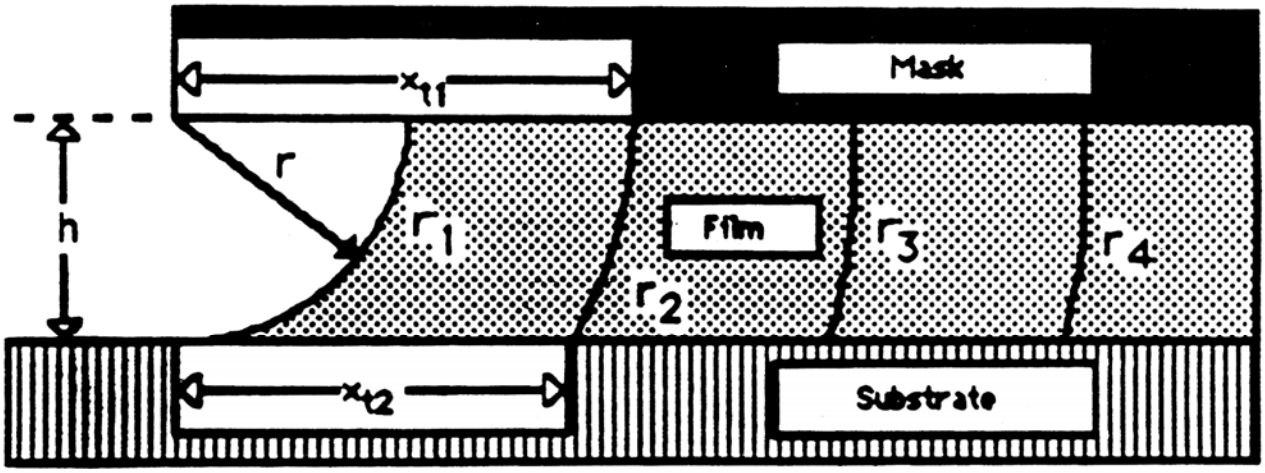
Creating a Sloped Sidewall for Al

- Want sloped sidewall for step coverage
- Thus over etch aluminum
- Allow resist to lose adhesion



Moving Interface Etching

Fig 17a



Stationary Interface Etching

Fig 17b

Sand Removal in AlSi or AlSiCu

- Metal etch leaves Al rich Si sand
- Copper makes reaction worse
- must remove with a "sand remover" wet etch
  29% H_2O, 70% HF, 1% HNO_3

Lift Off Techniques

- Put defined resist below metal deposition
- Al goes through holes
- Then dissolve resist
- Extra Al floats away
- Problem is the "Sky is Falling Syndrome"
- Material left behind gets held on the surface
- Lands on surface when pulled from liquid

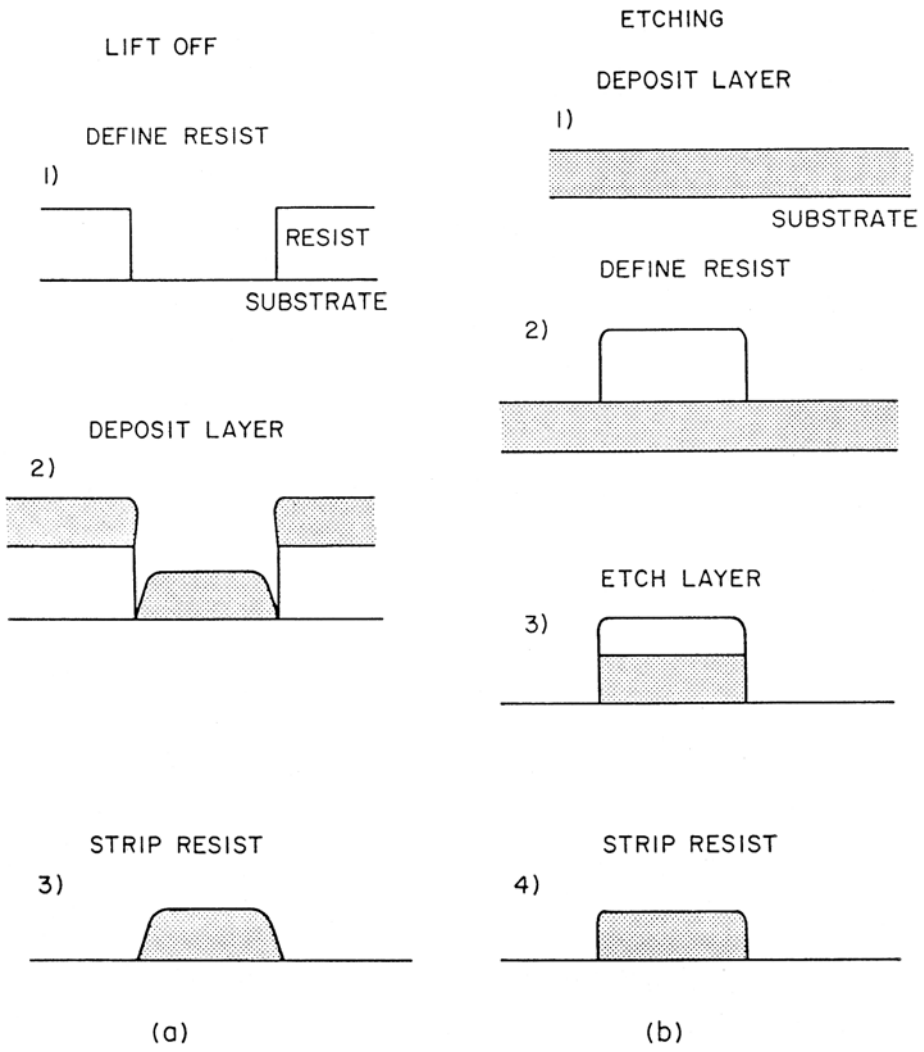


FIGURE 9
A schematic representation of two techniques for transferring resist features into a layer. (a) Shows the resist/deposition strip sequence of lift off, and (b) shows the deposit/resist/etch/strip sequence of etching.