1. Introduction to Research

Microelectronic capacitive-type sensors [1] are becoming commonly used components of many Systems-on-Chip (SoC). Their function is to detect changes of a capacitance due to various physical or chemical phenomena being exploited within a sensor/transducer. Examples include measurement of internal capacitances of semiconductor devices used as sensors, measurements of 2-D and 3-D parasitic capacitances of interconnects within integrated circuits, measurements of capacitance change due to incidence of particles or bubbles on the surface of electrodes of chemical, biochemical and microfluidic sensors, etc. Some of the capacitance measurement techniques can be substantially miniaturized [2] allowing for integration of signal processing circuitry with the capacitive sensors, in effect resulting in large-area arrays of capacitive sensors integrated with read-out electronics on a single chip. These capacitive sensor arrays find applications in highly integrated Lab-on-Chip (LoC) systems [3], miniature electrical tomography systems [4], MEMS inertial sensors, and capacitive fingerprint sensors [5].

Measuring a capacitance change has been done in many ways, depending mostly on application and the required accuracy. A Charge-Based Capacitance Measurement (CBCM) [6] has been proposed initially to measure femto- and atto-Farad level parasitic interconnect capacitances in VLSI chips.

![CBCM basic test circuit](image)

The CBCM test circuit (Fig.1) operates in two phases. In the Phase 1, the n-MOS transistor is off but the p-MOS transistor is on and it charges the unknown capacitor $C$ with the current $I$, which is measured with the ammeter. In the phase 2, the p-MOS transistor is off but the n-MOS transistor is on, discharging the capacitor $C$. If the clock voltages $V_P$ and $V_N$ have a frequency $f$, then the capacitance $C$ can be evaluated from the relation:

$$I = C \cdot V_{DD} \cdot f$$
The important feature of the CBCM method is that both n-MOS and p-MOS transistors must be driven by non-overlapping signals (Fig.2), hence eliminating the possibility of short circuit current between $V_{DD}$ and $V_{SS}$.

![Figure 2. Example of non-overlapping CBCM signals $V_N$ and $V_p$ [6].](image)

The CBCM method can be also used to measure a difference of two capacitances (Fig.3), allowing practically to eliminate parasitic capacitances of interconnects always present in integrated circuits, as well as all other capacitances that one does not want to measure.

![Figure 3. The concept of differential CBCM measurement.](image)

Typical data obtained using the CBCM method (Fig.4) display the measured current as a function of both power supply $V_{DD}$ and signal frequency $f$. In the submicron CMOS technologies $V_{DD}$ is rather small, however frequency can be high, potentially alleviating the problem of accurate measurement of small currents on-chip. In the past, the attempted solution was to convert current to voltage by using an integrator and either to amplify the voltage signal [4] or to use ΣΔ readout circuit [3]. New avenues should possibly exploit current-domain and time- or frequency-domain signal processing, and they will be attempted in this project.
2. NSERC USRA Candidate Requirements

The research work in the Summer 2015 project will involve investigating on-chip metrology for capacitive sensors, starting from the CBCM method outlined above. Other methods can be added to the project, depending on results and time. The activities include:

- literature study (25%)
- circuit simulation (50%)
- reporting results (25%)

The project has a potential to contribute to student's Thesis (if the candidate is interested) and also result in possible publication (depending on results).

The student interested in this project should be familiar with microelectronic circuits, CMOS technology and CMOS devices, usually being taught in such ENSC courses as ENSC 325, ENSC 425, ENSC 450, and/or equivalent Directed Studies courses. Knowledge of CMOS circuit industry-standard simulation software (HSPICE - available in ESIL on Linux workstations) is an important asset for the project, and candidates with this experience will be given priority. For the candidates who are familiar with other versions of SPICE this project may be an opportunity to learn HSPICE.

References


