Packaging and Ball Bonding

- Gold wire makes contact from bonding pads on chip to package
- Gold wire is formed into ball to make contact
- Uses an ultrasonic process & heat
- Process called "Ball Bonding"

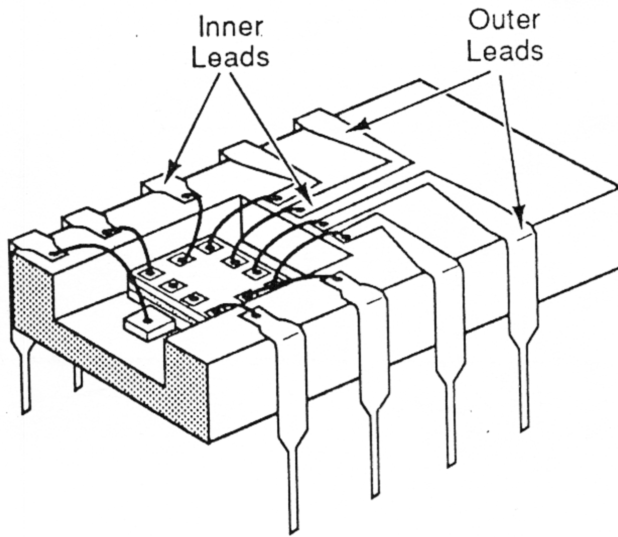
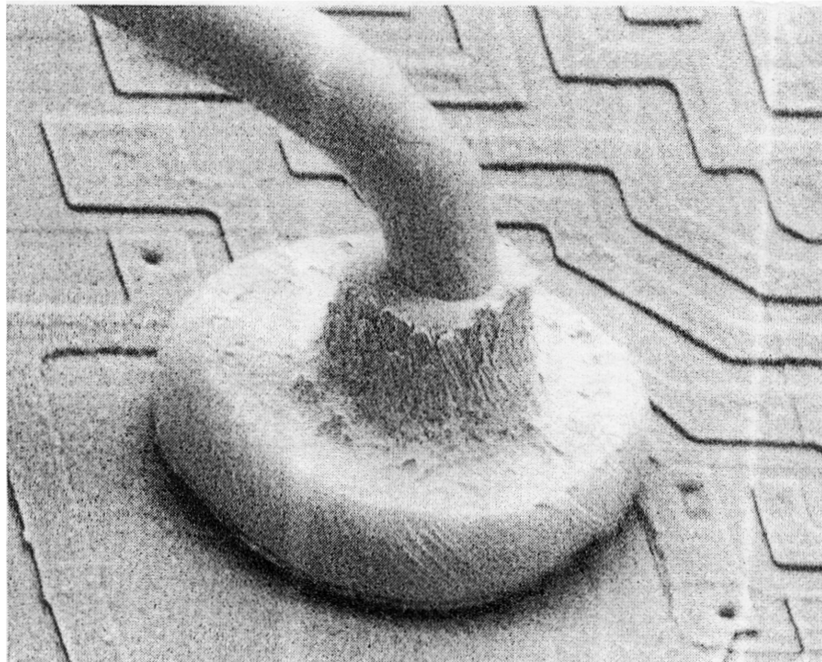


Figure 18.14 Inner and outer leads.

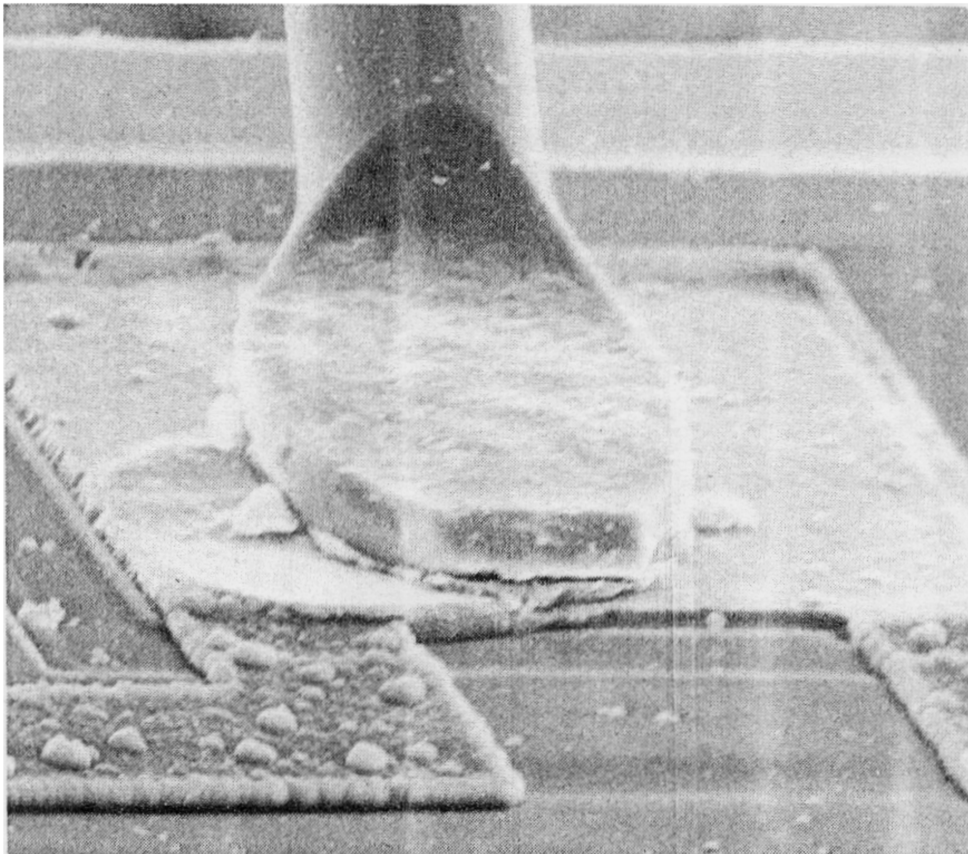
Fig. 13-7 SEM picture of ball-bonded 25-μm gold wire.



Wedge Bonding

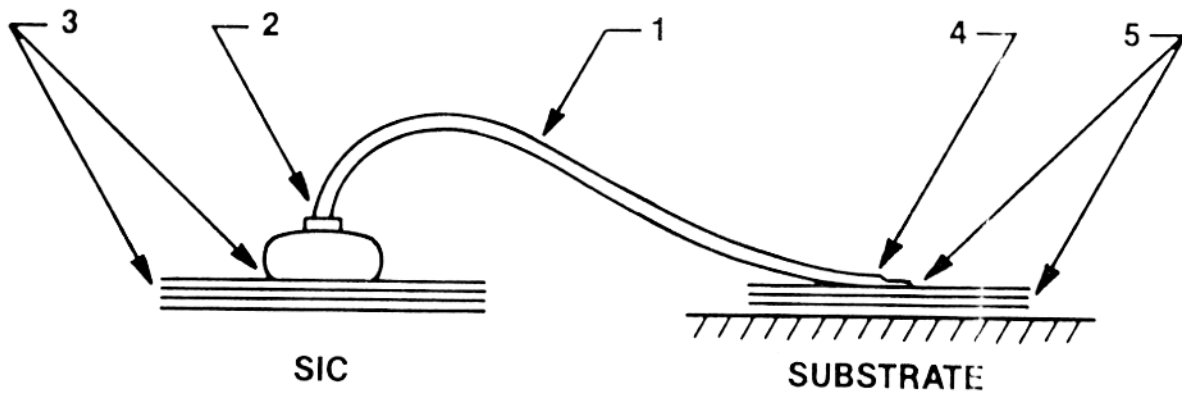
- Use also gold wire
- Flatten wire
- Wedge usually on package, ball on chip
- Note wire elevated above surface

Fig. 13-6 SEM micrograph of 25-μm Au wire ultrasonically bonded to an Al pad.



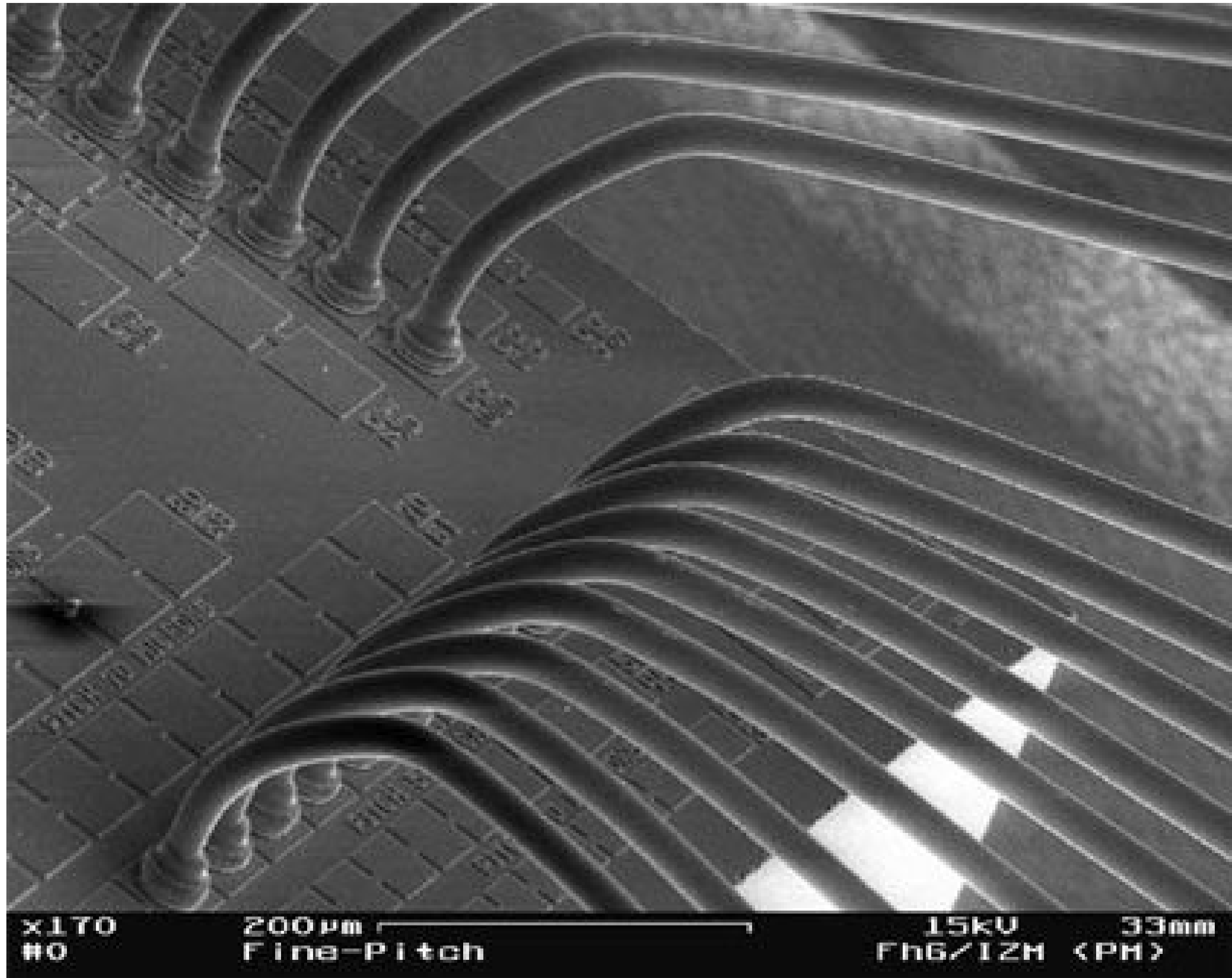
Basic Ball Bonding

- Ball on chip
- Wedge on package
- Bonds that do not make contact are largest packaging failure
- Get 25-50% lose in dicing and packaging in many chips.
- More bonds, more likely some fail.



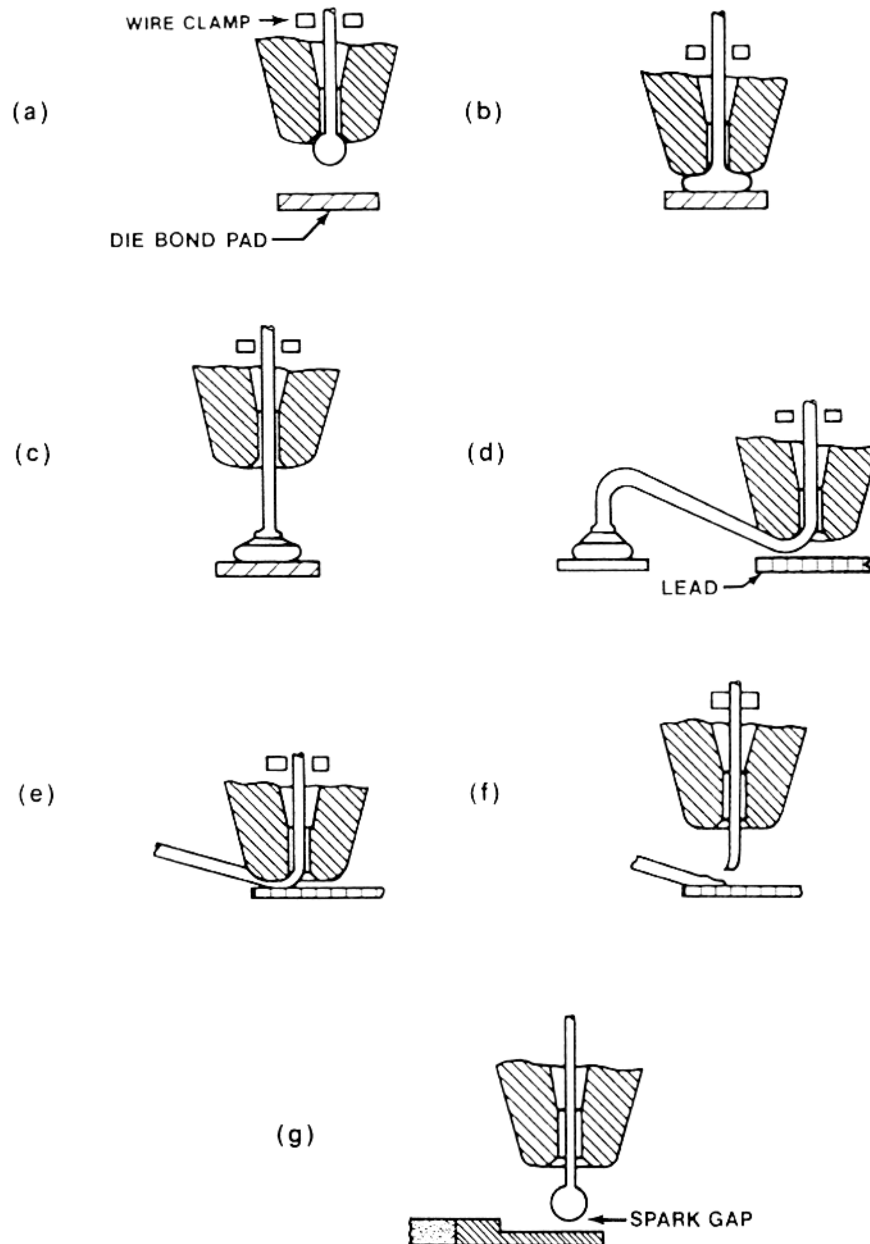
Wires on Package

- Close spacing of wires difficult with high pin count
- Limitation is set by angle the bonds must come in at



Ball Bonder Cycle

- (a) Start with ball on wire in anvil (capillary) over pad
- (b) Anvil presses ball onto pad with ultrasonic to create bond
- (c) Release with and move vertically
- (d) Move wire to lead pad on package
- (e & f) Create wedge bond at lead with anvil & break wire
- (g) Spark melts wire to create new ball



Ball Bonder

- Manual Ball Bonder ~$50-$100K
- Takes skilled operator about 5 minutes per bond

Head Movement in Ball & Wedge Bonder

- Ball bonder head moves x, y, z
- Wedge bonder head moves only z, stage x,y

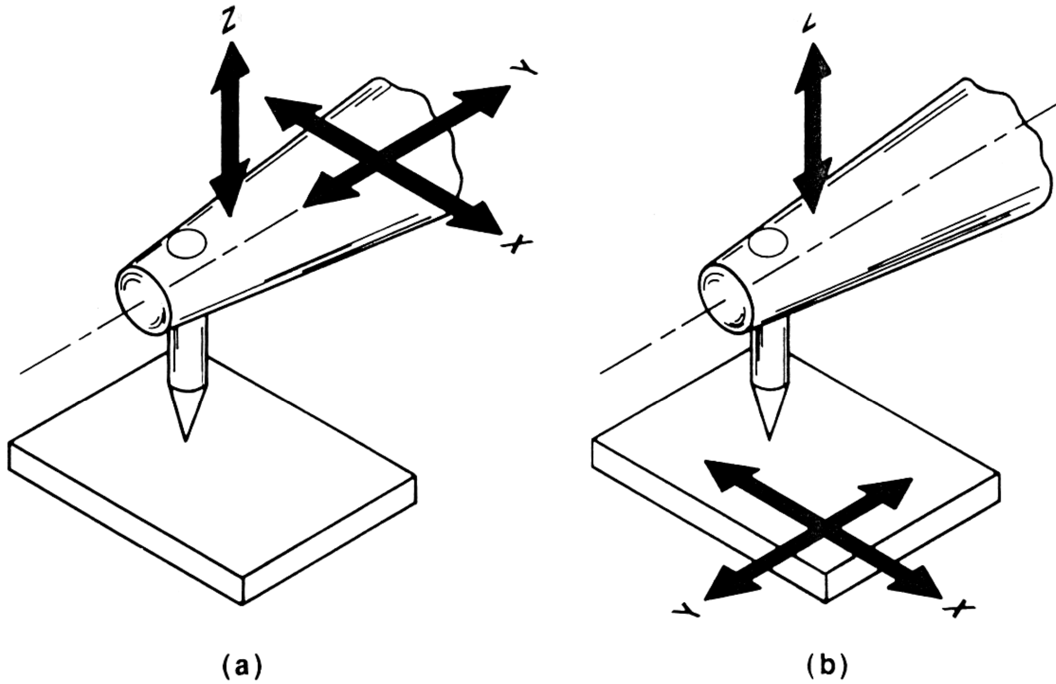


FIGURE 25
Comparison between head motions of a ball-to-wedge bonder (a) and a wedge-to-wedge bonder (b). (*After Nachon and Tai, Ref. 37.*)

Position of Bonds

- Layout of bonding diagram very important on chips
- Need to know what chip pads go to which package pins

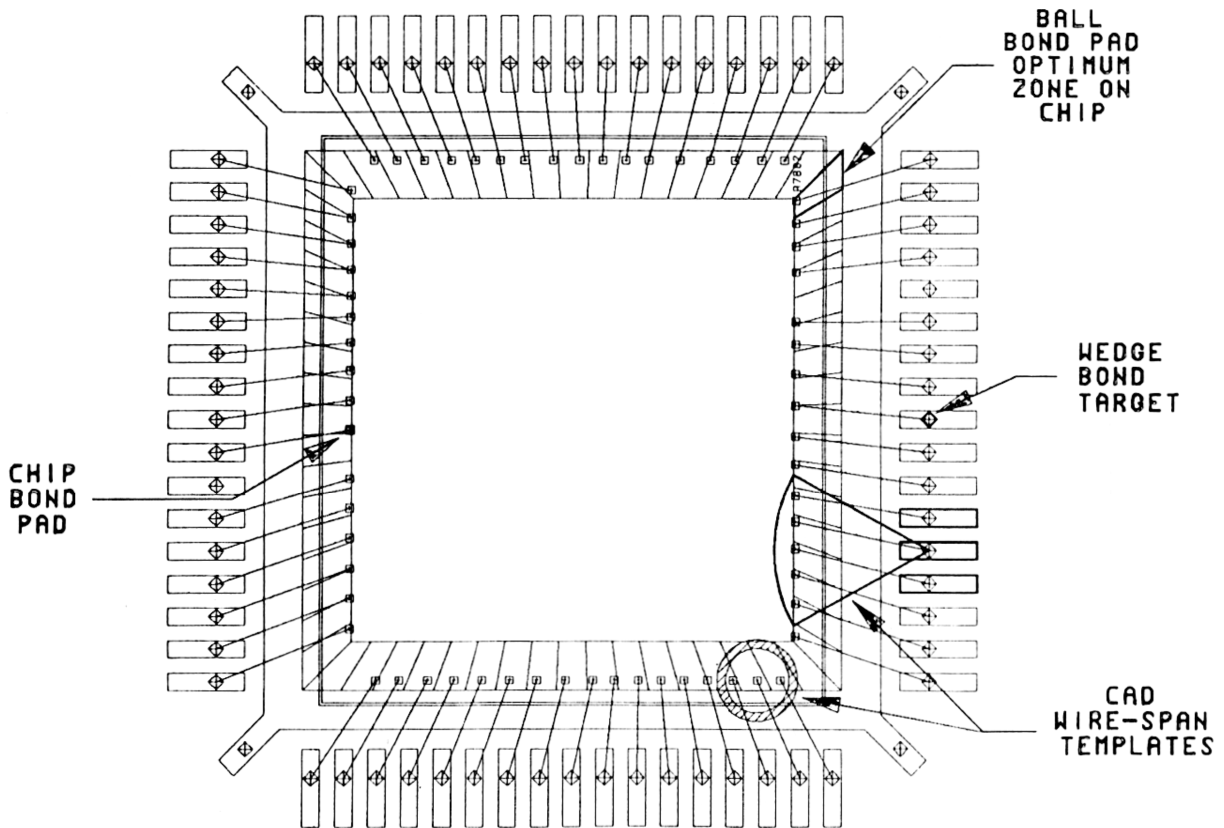


FIGURE 9
CAD template for positioning bonding pads on the die in their optimum location to achieve high assembly yields and high reliability performance. Use of the template assures the device designer that wire-span lengths meet the design rules (*Courtesy of AT&T Bell Laboratories*.)

Angle Limitations on Bonds

- Angle of bonds determines limit of bonding possibility

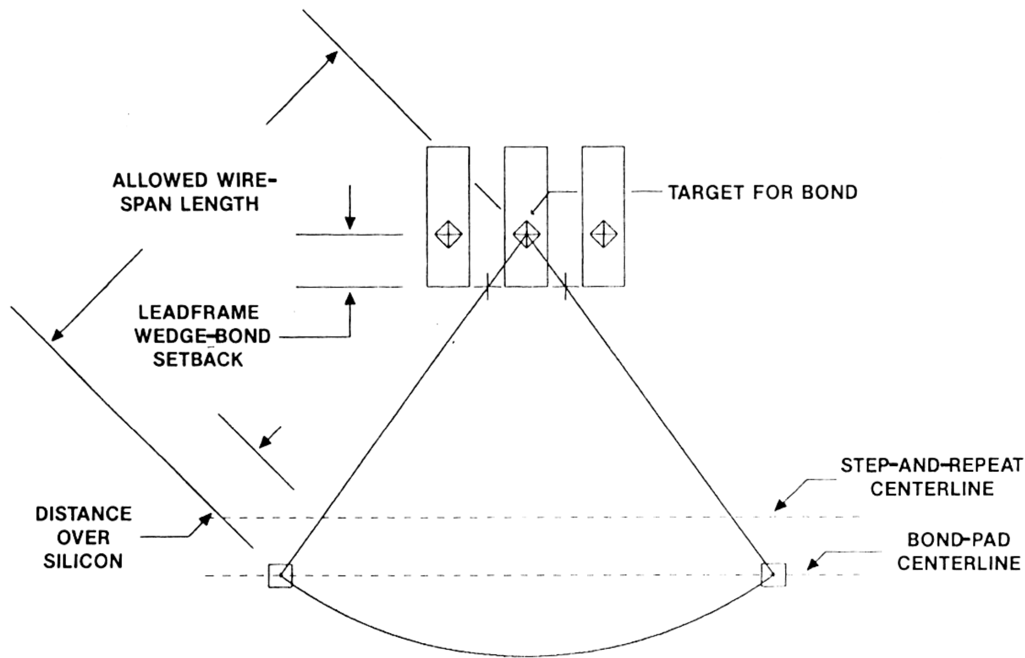


FIGURE 10
CAD template for checking adherence to wire-span guidelines. The template also provides an extended zone (beyond the optimum shown in Fig. 9) for those cases where location in the optimum zone is not compatible with the device layout. The maximum distance to the step-and-repeat centerline is controlled to minimize wire shorts to the die edge (*Courtesy of AT&T Bell Laboratories.*)

Corners of Chips: Problem bonding area

- Corners where bonds often limited

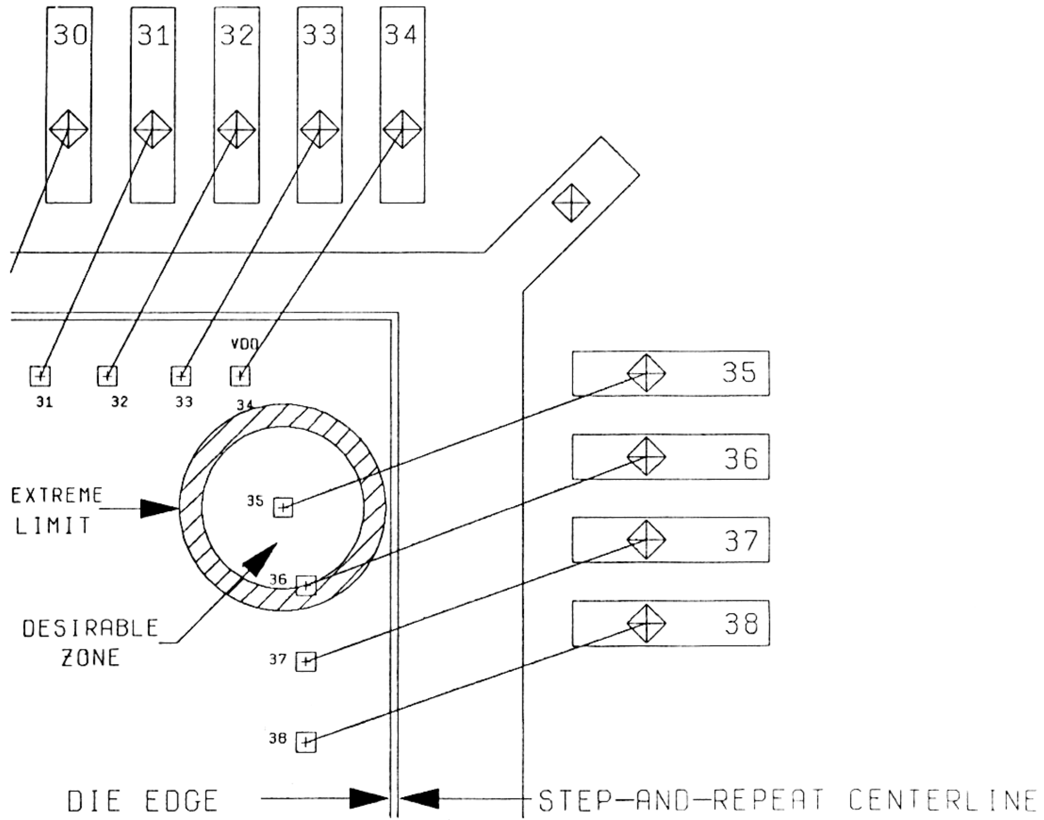


FIGURE 11

CAD template for checking the maximum distance that a wire spans over silicon, to minimize edge shorting. This example shows a violation of the guidelines. A correction would be to move the bonding pad to the right until the circle template became tangent to the step-and-repeat centerline (*Courtesy of AT&T Bell Laboratories*.)

Microprocessors, Logic & Bond Count increase

- DRAM pin count is steady due to multiplexing of addresses
- Enhanced by use of SIM modules
- Microprocessor and Logic tend towards Rent's rule

$$IO\ Pins = \alpha(Gate\ Count)^{\beta}$$

Typically: α=4.5, β=0.5

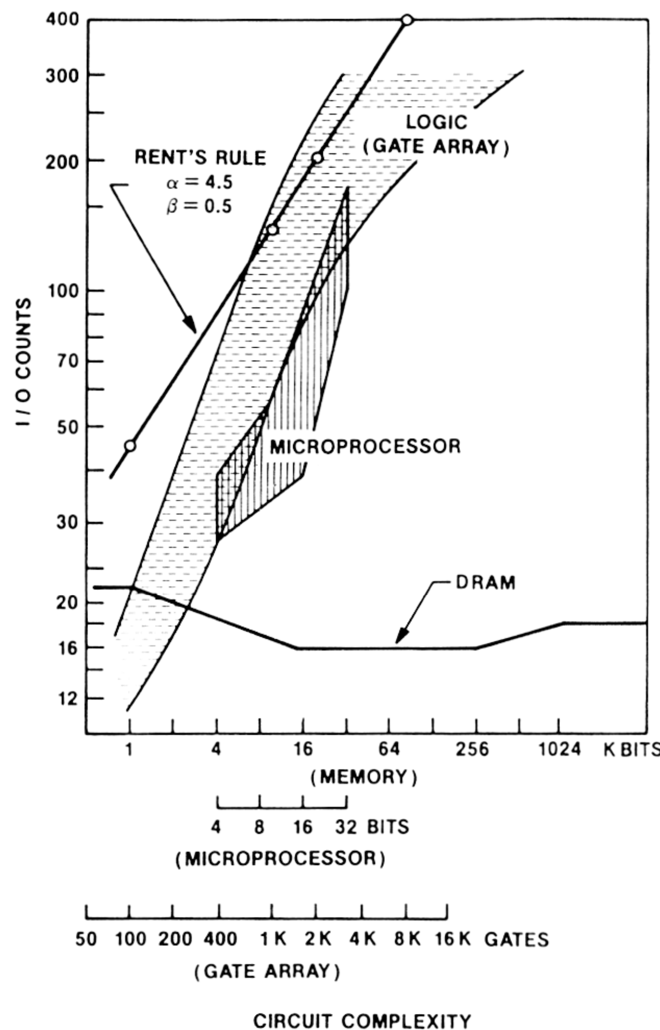
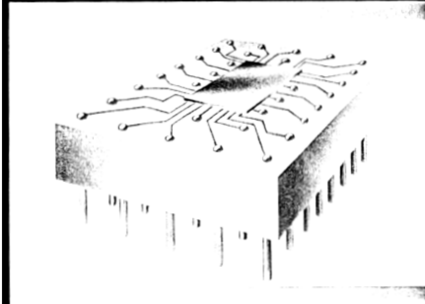


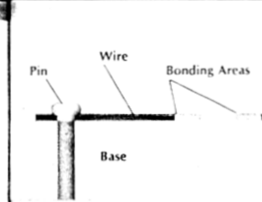
FIGURE 2
Comparison of I/O requirements for logic, microprocessor, and memory devices (DRAM) as a function of circuit complexity (*Courtesy of Kyocera International, Inc.*)

Other Bonding

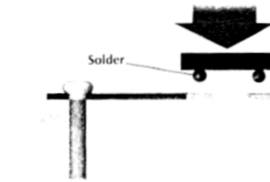
- Tape Automated Bonding: All bonds at once
- Flip Chip Indium solder ball mounting

Flip-Chip Bonding

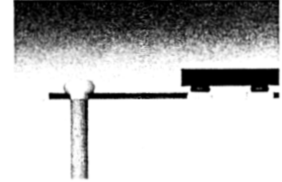




nlike leads extend through the ceramic base ed in this type of bonding. The lower ends the pins will plug into a circuit board; the ps are linked by fine wires to bonding areas the surface of the ceramic.

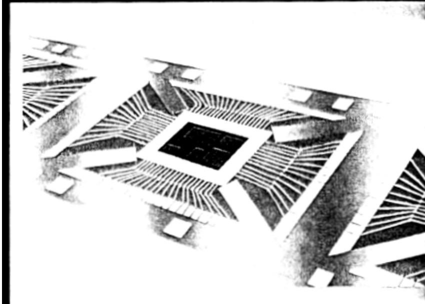


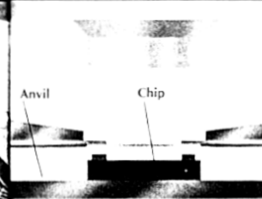
Balls of molten solder are deposited on raised contact pads on the underside of the chip and allowed to cool. Then the chip is set onto the base, with the solder balls coinciding with bonding areas.



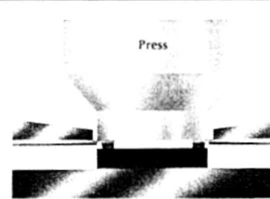
The chip and base are then heated to about 275 degrees Celsius, a temperature high enough to melt the solder and cement the chip to the bonding areas, but low enough not to damage the chip.

Tape-Automated Bonding

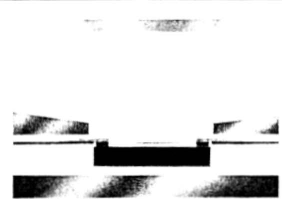




join a chip to gold conductors *(left)*, is placed on a heated platform called anvil *(above)*. The conductors are sitioned above the chip by means of rocket holes in a tape support.



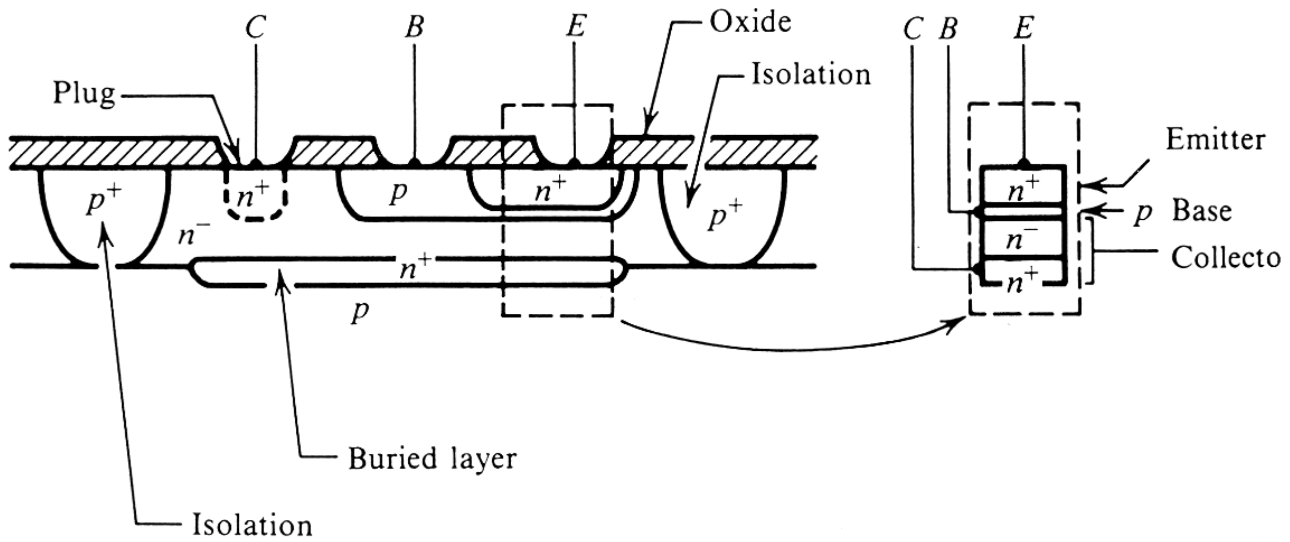
As a ceramic press descends toward the tape, the anvil rises, pressing the conductors and the chip together. Heat and pressure stick the chip to the conductors.



After the bond is made, the press and anvil retract. The tape lifts the bonded chip away from the anvil and then advances, moving the next set of conductors into position.

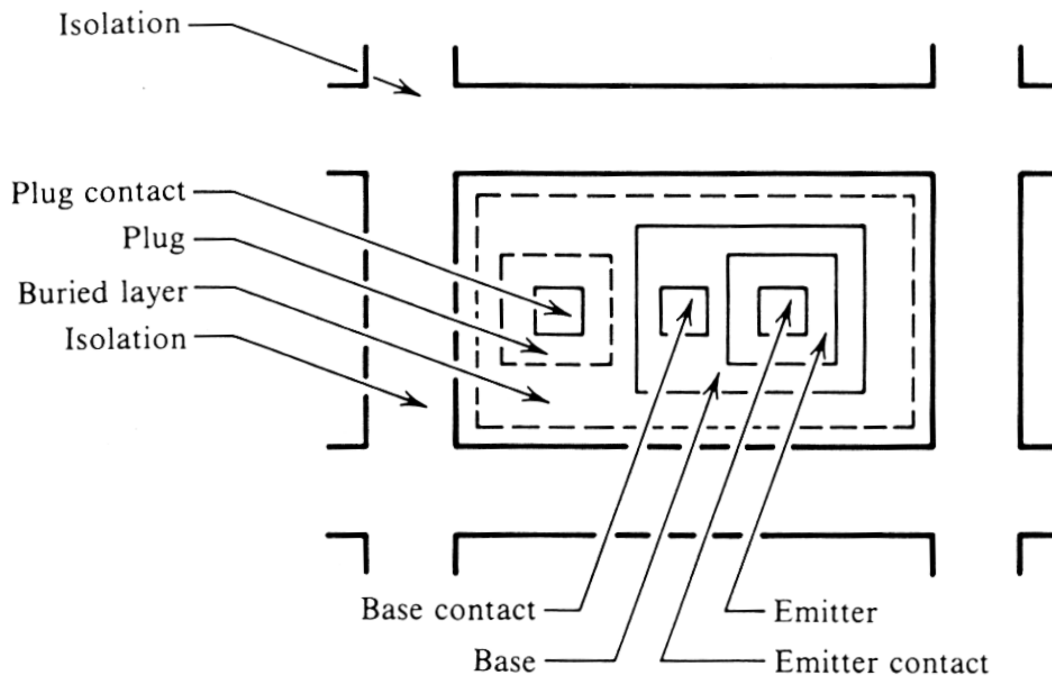
Vertical Buried Collector Bipolar Process

- Put buried collector to reduce collector resistance



(*a*)

Figure 10-5 A realistic bipolar transistor fabricated in a semiconducting substrate. (*a*) Cross-section of a typical transistor; the inset shows the relationship to the idealized transistor. (*b*) More detailed view showing how the minimum dimensions achievable by the masking process (*D*), alignment tolerance (*A*), layer thicknesses (*t*), and junction depths (x_j) define the dimensions of the transistor.



(*c*)

Figure 10-5(c) Overhead view

Standard Buried Collector (SBC) Bipolar Process

- Start with P substrate, high resistance
- Grow oxide, mask for buried collector
- n+ buried layer implant
- Grow n type epi layer
- Mask for P type isolation diffusion to P substrate

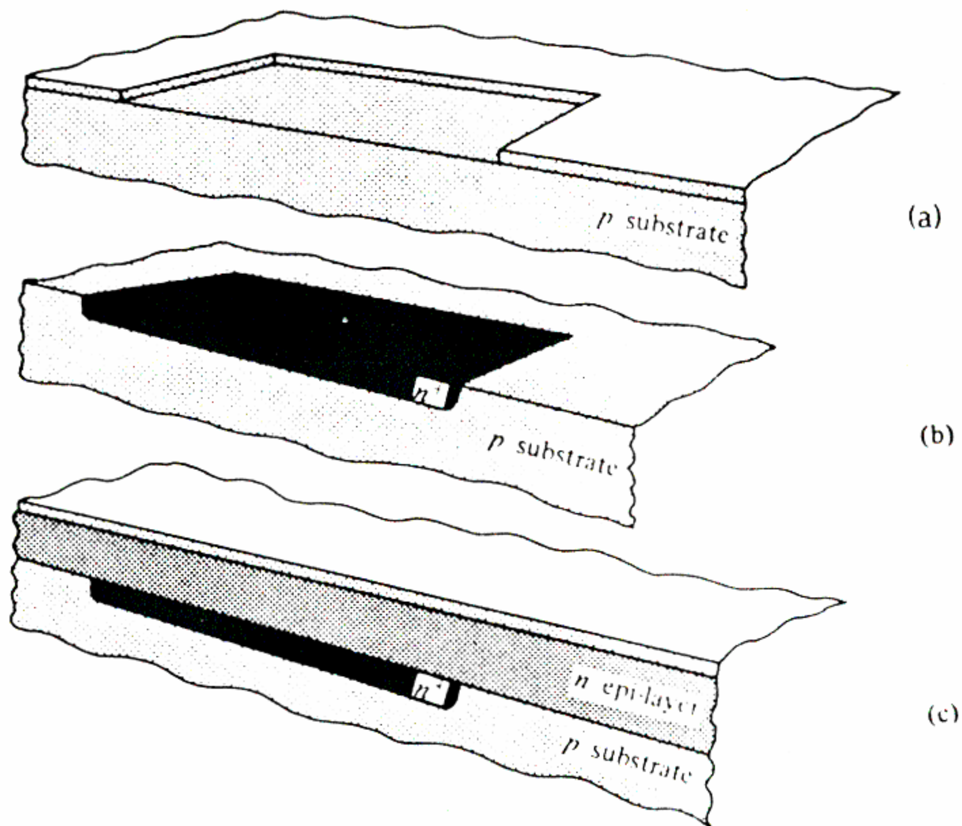
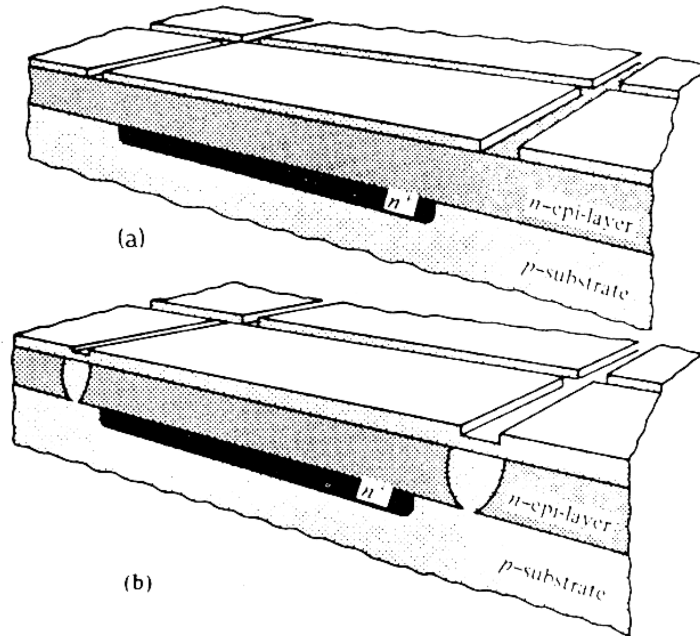


Fig. 7-21 (a) Oxide windows are opened for n^+ buried layer deposition. (b) Oxide layer is removed in preparation for epitaxial growth. (c) n-type epitaxial layer and oxide layer are grown. Copyright, 1982, Prentice-Hall. Reprinted with permission from reference [127].

Buried Collector Bipolar Isolation & Base

- Grow oxide, and mask for p base
- Grow oxide, mask for n+ emitter & collector contact
- Deposit and pattern metal



-22 (a) Oxide windows are opened for *p*-type isolation diffusion. (b) Oxide layer is vn over *p*-type isolation regions. Copyright, 1982, Prentice-Hall. Reprinted with

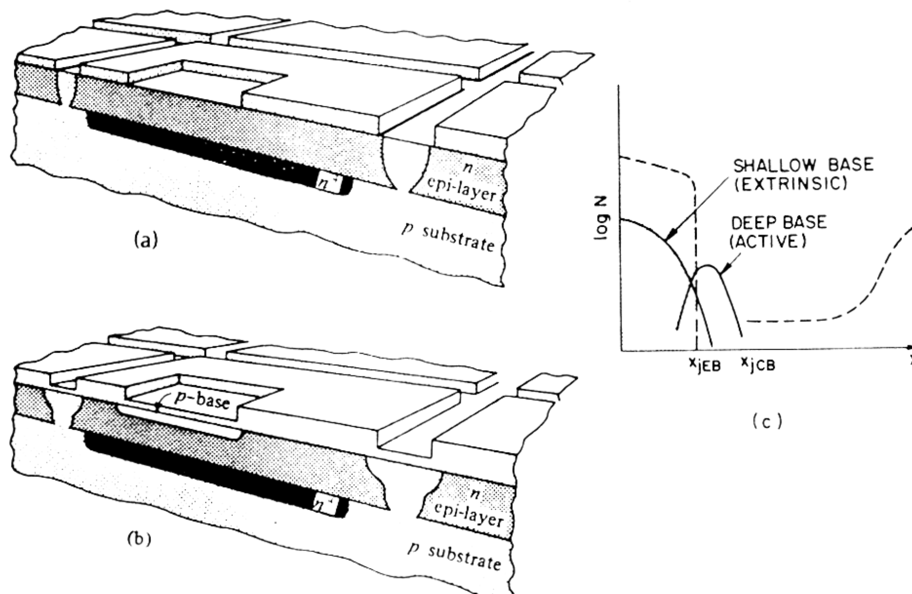


Fig. 7-24 (a) Oxide windows are opened for *p*-type base formation. (b) Base diffusion is completed and oxide is regrown. Copyright, 1982, Prentice-Hall. Reprinted with permission from ref. [127]. (c) Doping profile showing results of double-base implant.

Buried Collector (SBC) Bipolar Emitter/Collector

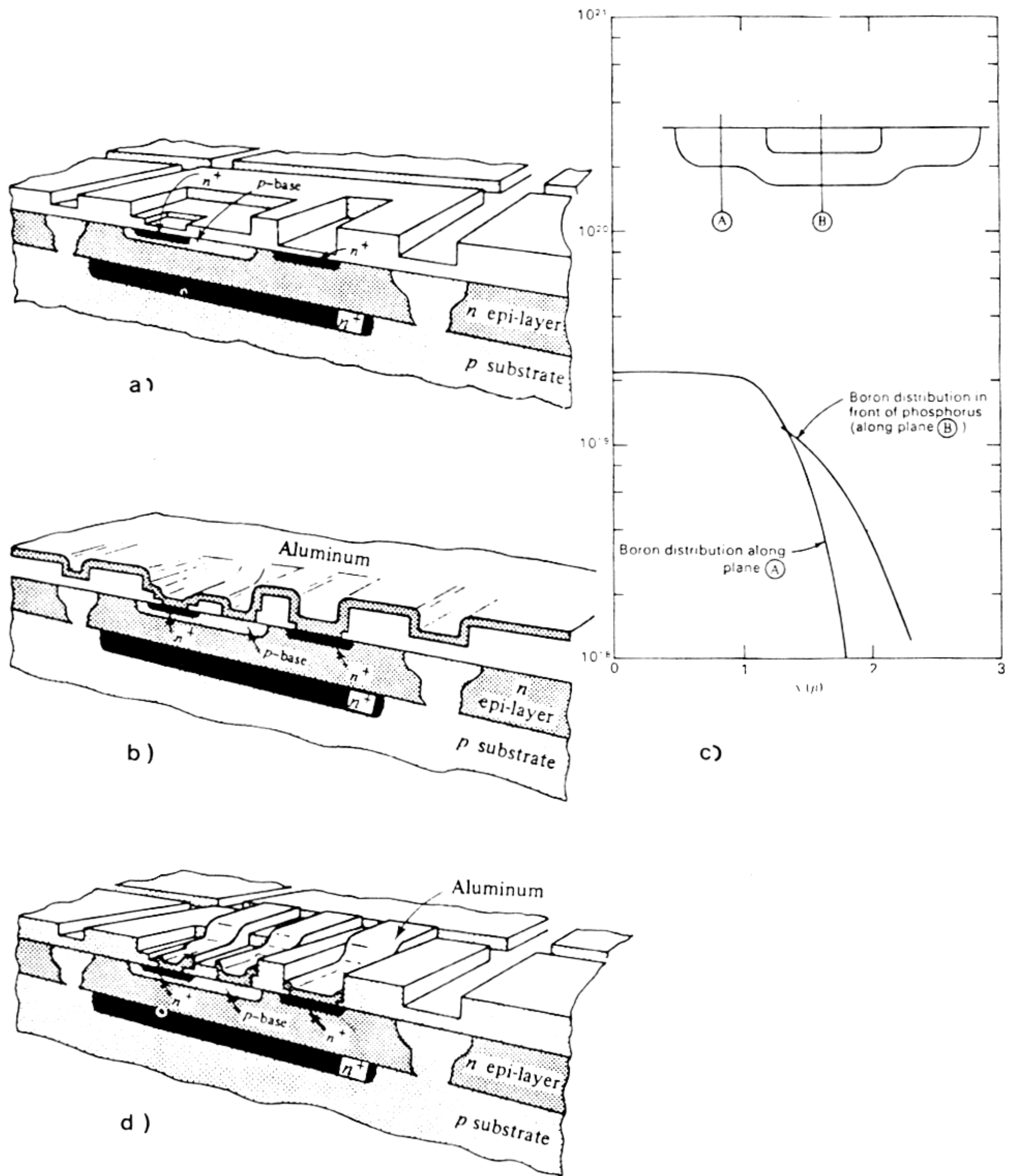


Fig. 7-25 (a) Oxide windows are opened for n^+ emitter formation. (b) n^+ emitter diffusion is completed and oxide layer is regrown. (c) The *emitter push effect*; anomalous diffusion due to a second high concentration phosphorus diffusion.[128] (d) Completed *npn* transistor; aluminum is removed as needed to complete the circuit. Copyright, 1982, Prentice-Hall. Reprinted with permission from ref. [127].

Simple MosFet Transistor

- Need to create a isolated gate between source & drain
- Originally metal gate, now all polygate

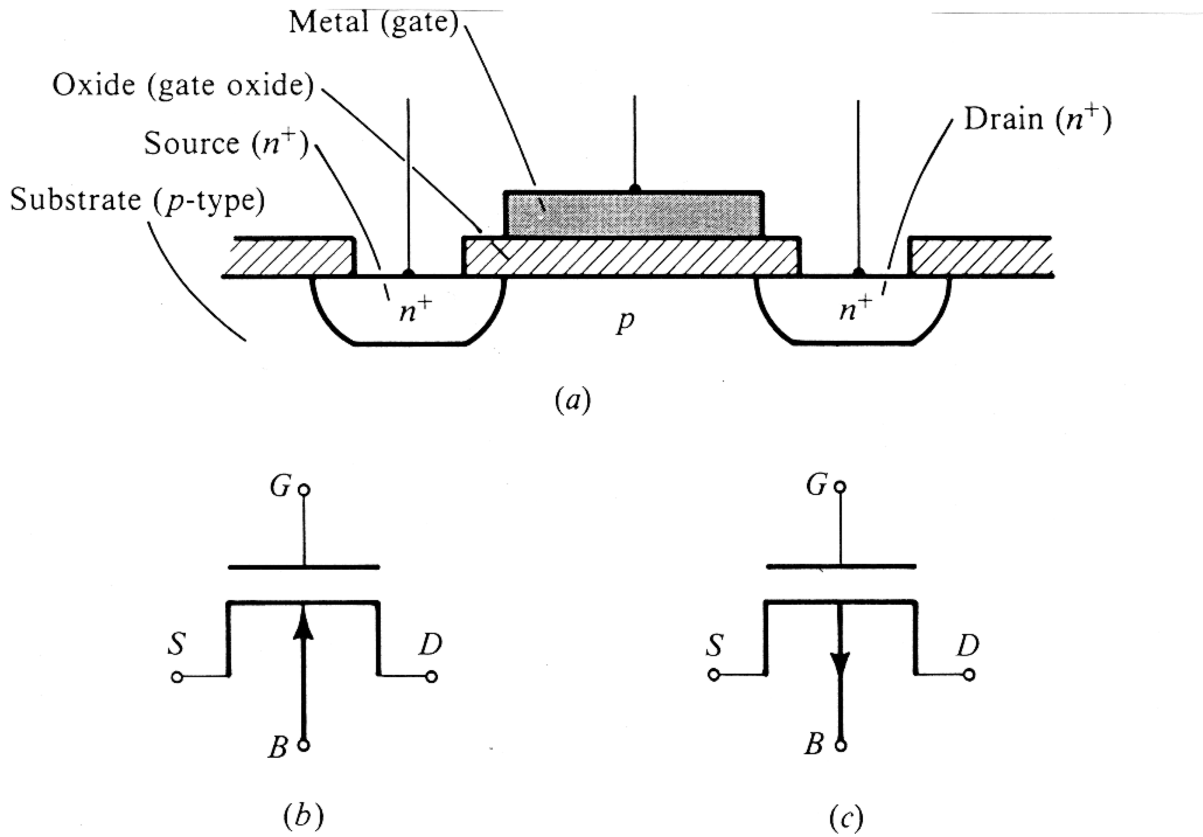


Figure 11-1 The MOS transistor. (*a*) Diagram of an MOS transistor, showing gate, gate oxide, source, and drain. (*b*) Symbol for an *n*-channel MOS transistor. (*c*) Symbol for a *p*-channel MOS transistor.

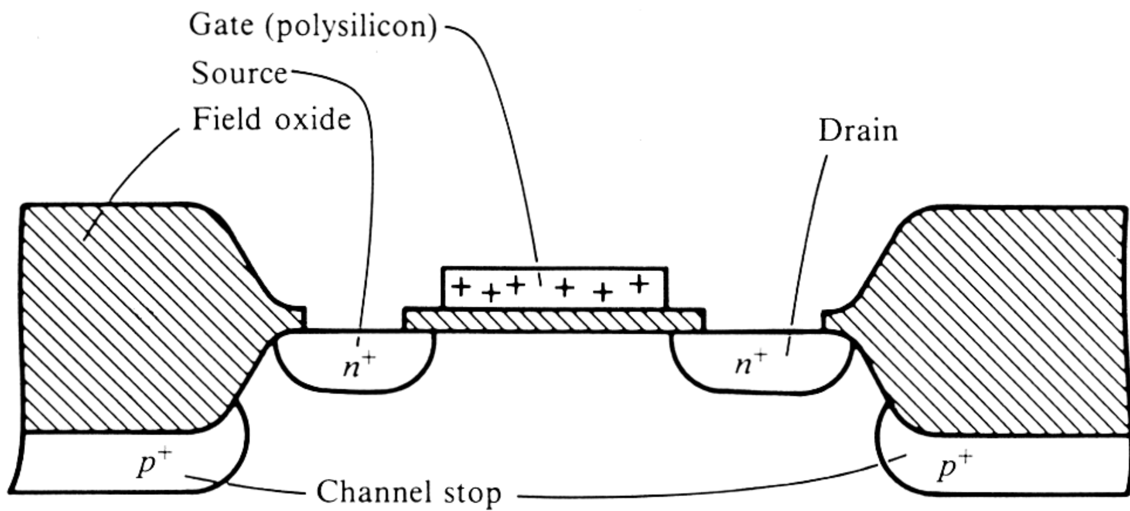
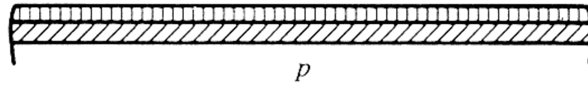


Figure 11-4 Cross-section of a practical NMOS transistor.

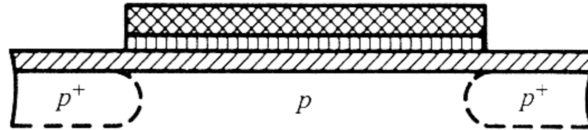
Simple One Metal/poly MosFet

- Simple One metal/poly MosFet

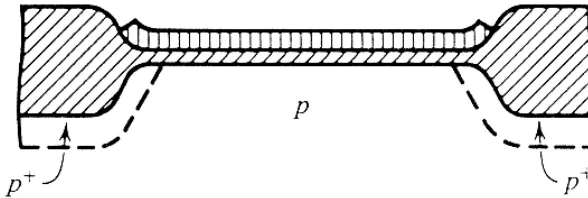
Initial oxidation
Silicon nitride deposition



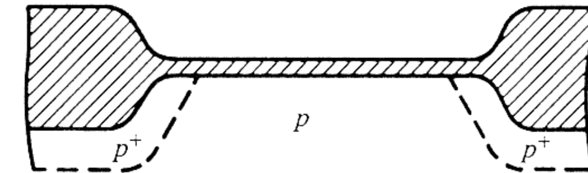
Channel stop implant (p^+)



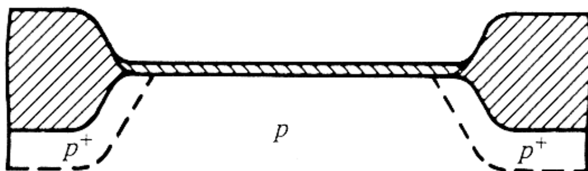
Selective field oxidation



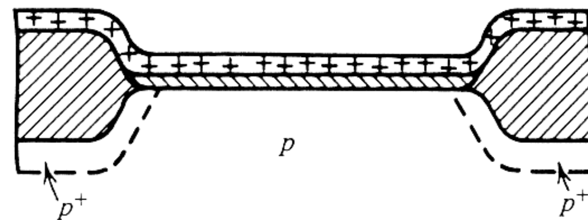
Silicon nitride removal



Gate oxidation



Polysilicon deposition
Polysilicon doping/oxidation



Gate mask

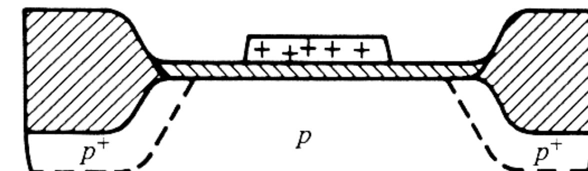
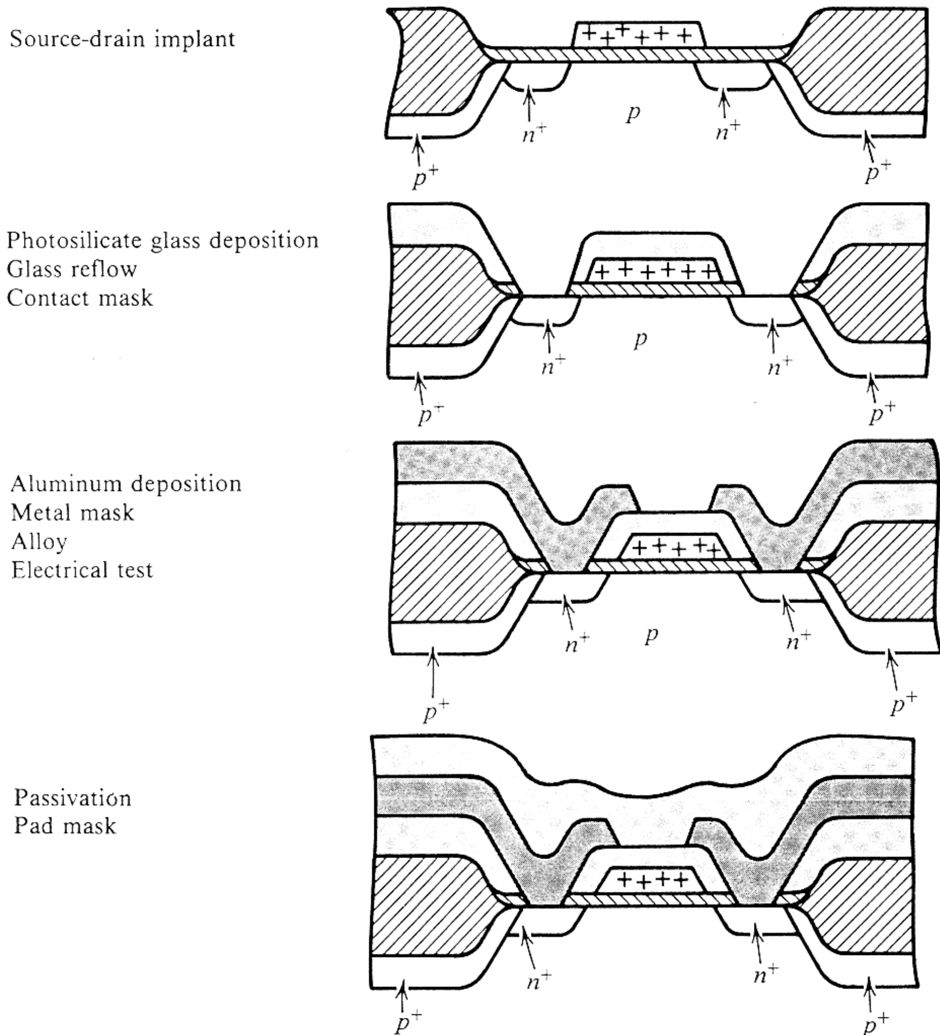
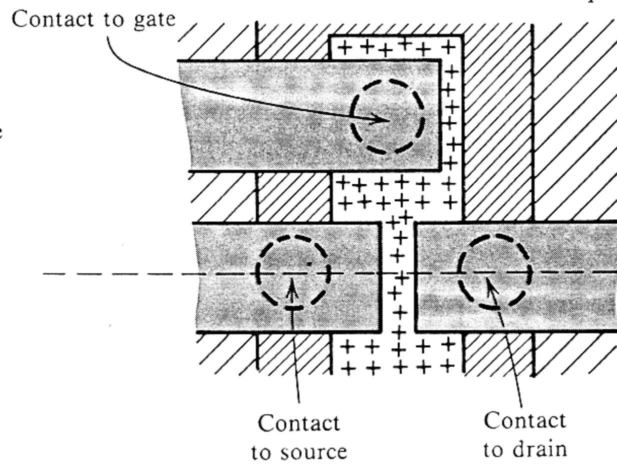


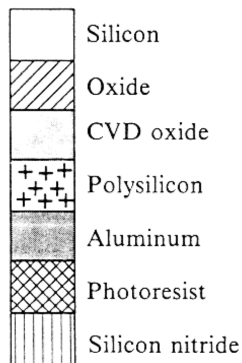
Figure 11-5 Steps in the fabrication on a NMOS transistor. Each panel depicts a cross-section, except for the final view which is a top view. In the top view, glass and passivation are omitted, although the shape of the contact opening through the glass is shown.

Simple One Metal/poly MosFet

- Simple One metal/poly MosFet Con'd







CMC Double metal, single poly CMOS

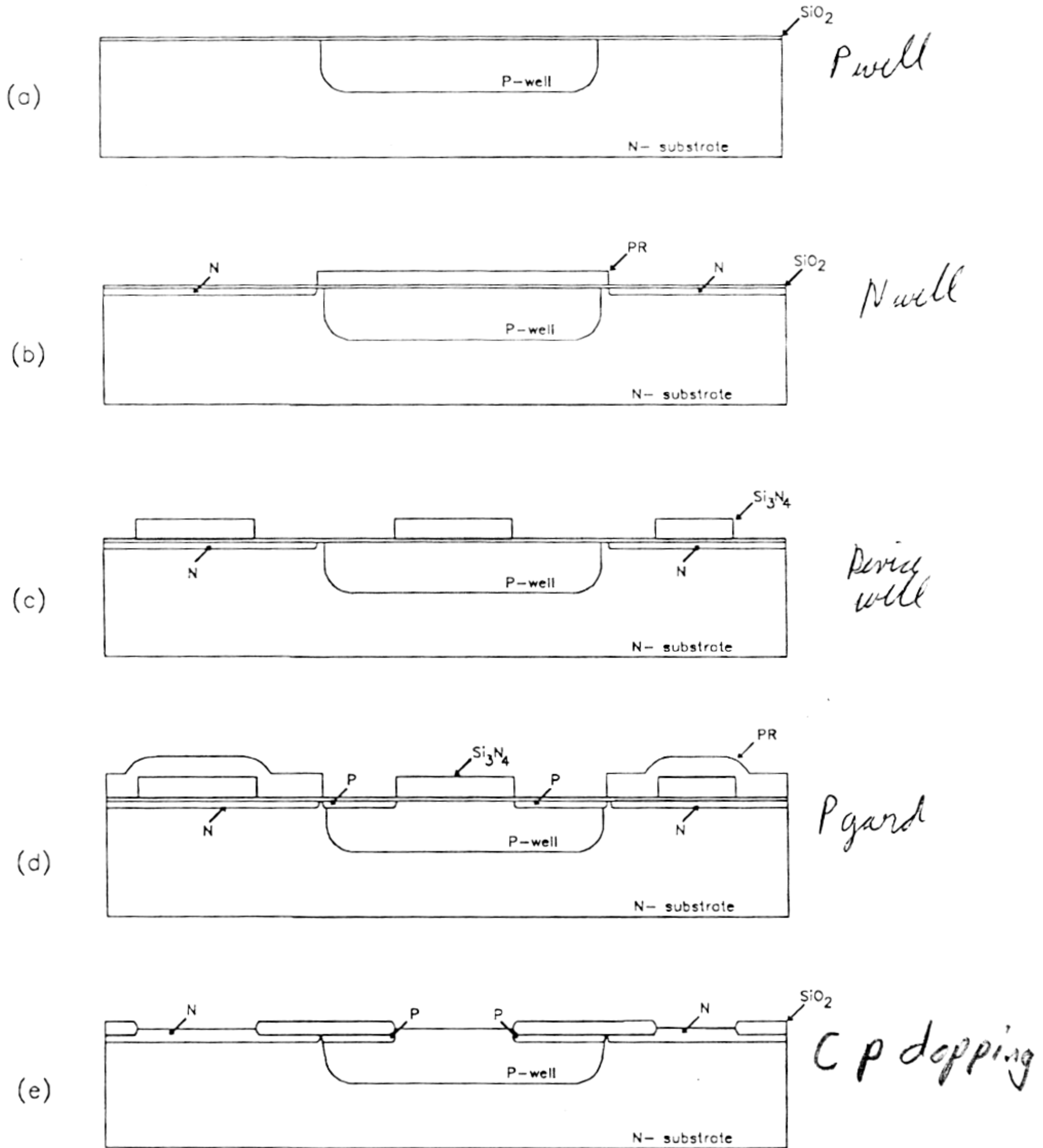


Figure C.1: CMOS3 DLM Process for a Simple Inverter and Capacitor

CMC CMOS: Poly through Metal

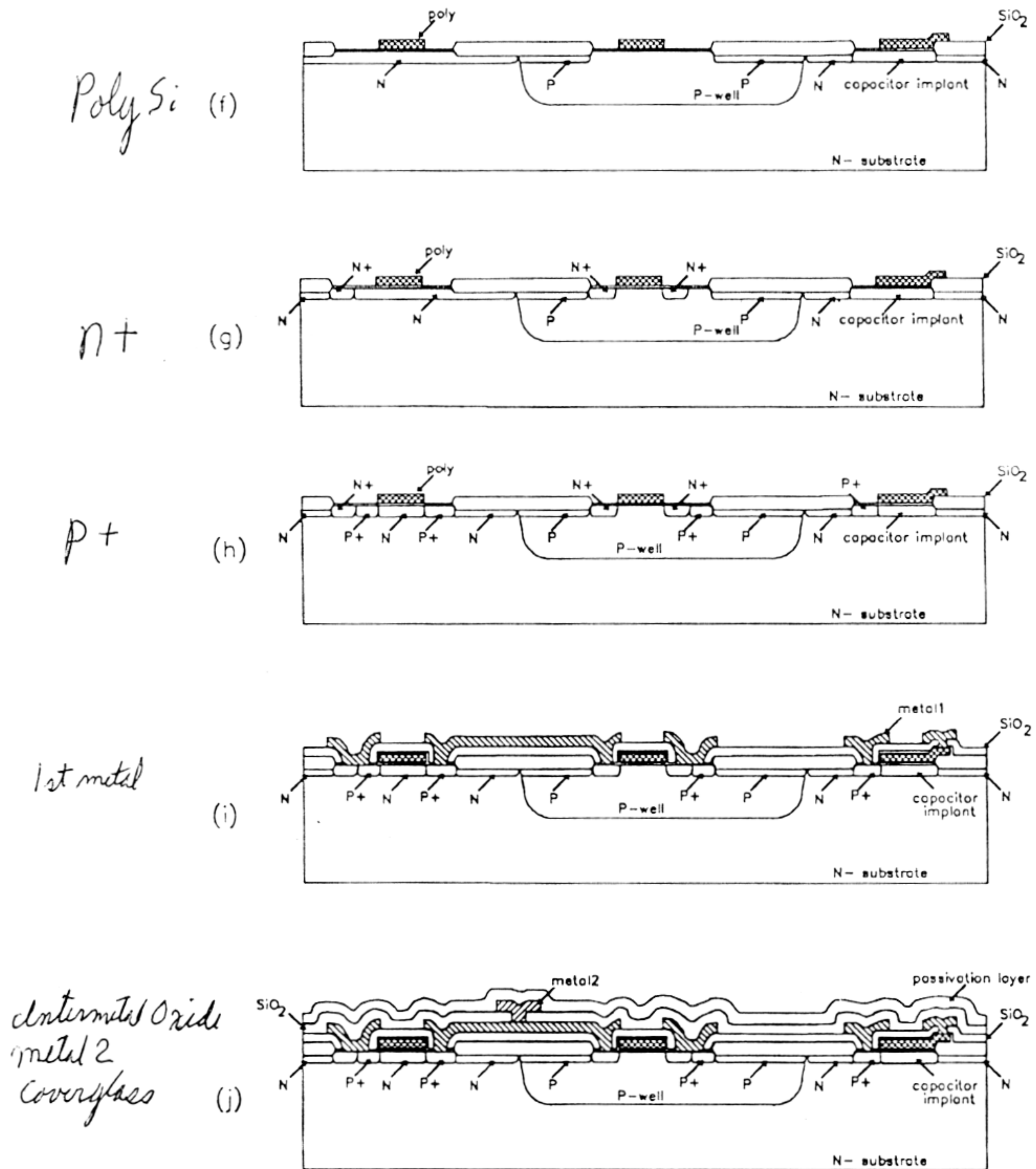


Figure C.1: CMOS3 DLM Process for a Simple Inverter and Capacitor Continued

CMOS Design Rules

- Sets size limits on structures
- Depends on the Design

MOSIS CMOS SCALABLE RULES (REV6)

WELL (P WELL, N WELL)

SAME POT. DIFF. POT.

ACTIVE

P- REGION

N- REGION

POLY

SELECT (PSELECT,NSELECT)

SUBS CONT

SELECT FOR WELL CONT

SELECT FOR XTOR

WELL

CONTACT to POLY

SIMPLER

CONTACT to ACTIVE

SIMPLER

CONTACTS EXACTLY 2x2

DENSER

MANY CONTACTS

ONE CONTACT

METAL1

VIA

POLY OR ACTIVE

EXACTLY 2x2

OVERGLASS

METAL2

PROBE PAD 75x75 MIC

BONDING PAD 100x100 MIC

MET2 REQD UNDR OVERGLASS

LAYER	CIF	CALMA *	COLOR
WELL	CWG	53	
PWELL	CWP	41	
NWELL	CWN	42	
ACTIVE	CAA	43	
SELECT	CSG	54	
PSELECT	CSP	44	
NSELECT	CSN	45	
POLY	CPG	46	
CONT to POLY	CCP	47	
CONT to ACT	CCA	48	
METAL1	CMF	49	
VIA	CVA	50	
METAL2	CMS	51	
CONT to ELEC	CCE	55	
ELECTRODE	CEL	56	
OVERGLASS	COG	52	

ALL LAYERS MUST BE ON LAMBDA GRID EXCEPT METALS WHICH CAN BE ON HALF LAMBDA GRID

CMOS Design Rules – Between Layers

- Sets spacing limits between layers

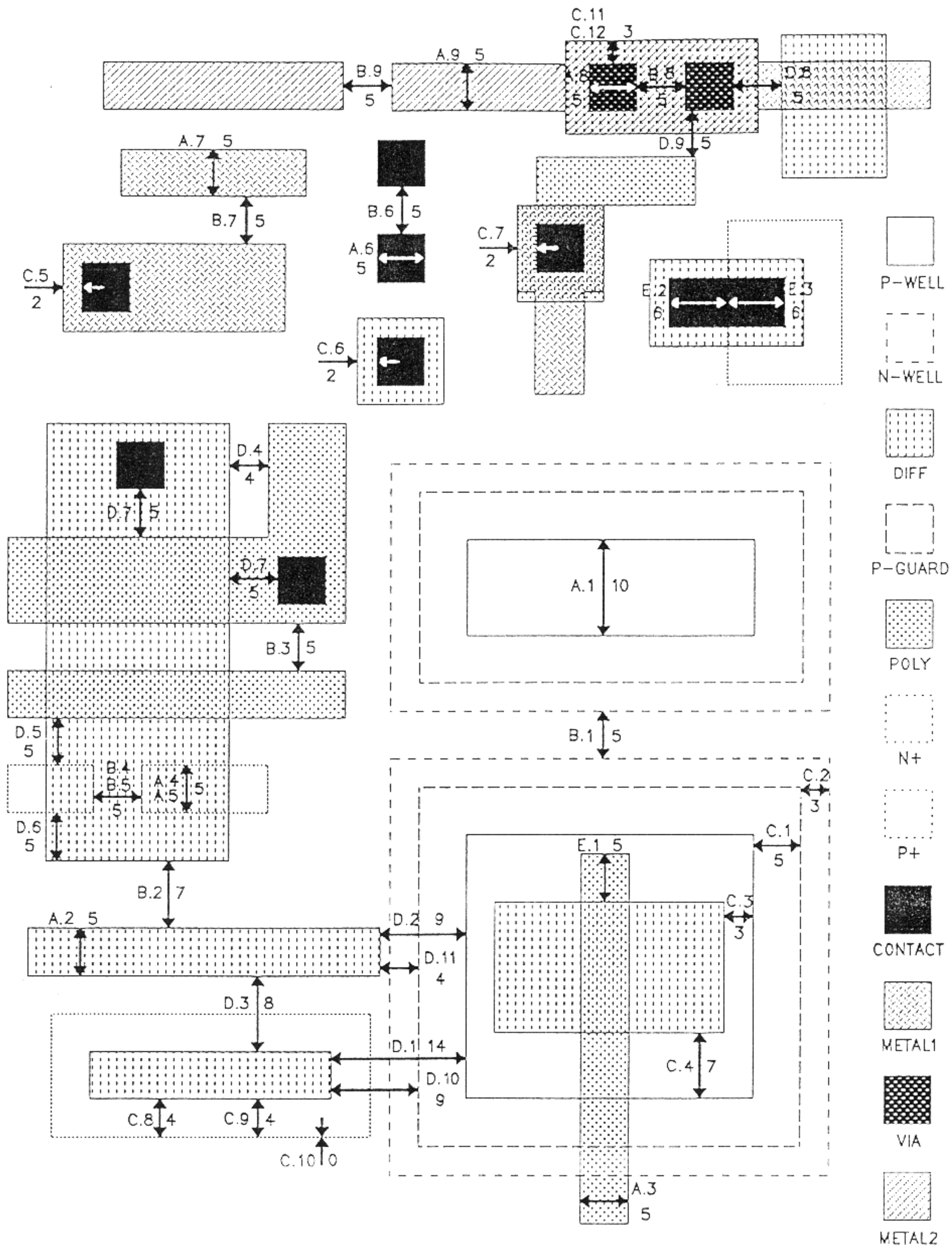


Figure C.2: CMOS3 DLM Design Rules

CMOS Design Rules – Bonding Pads

- Bonding pads also have rules

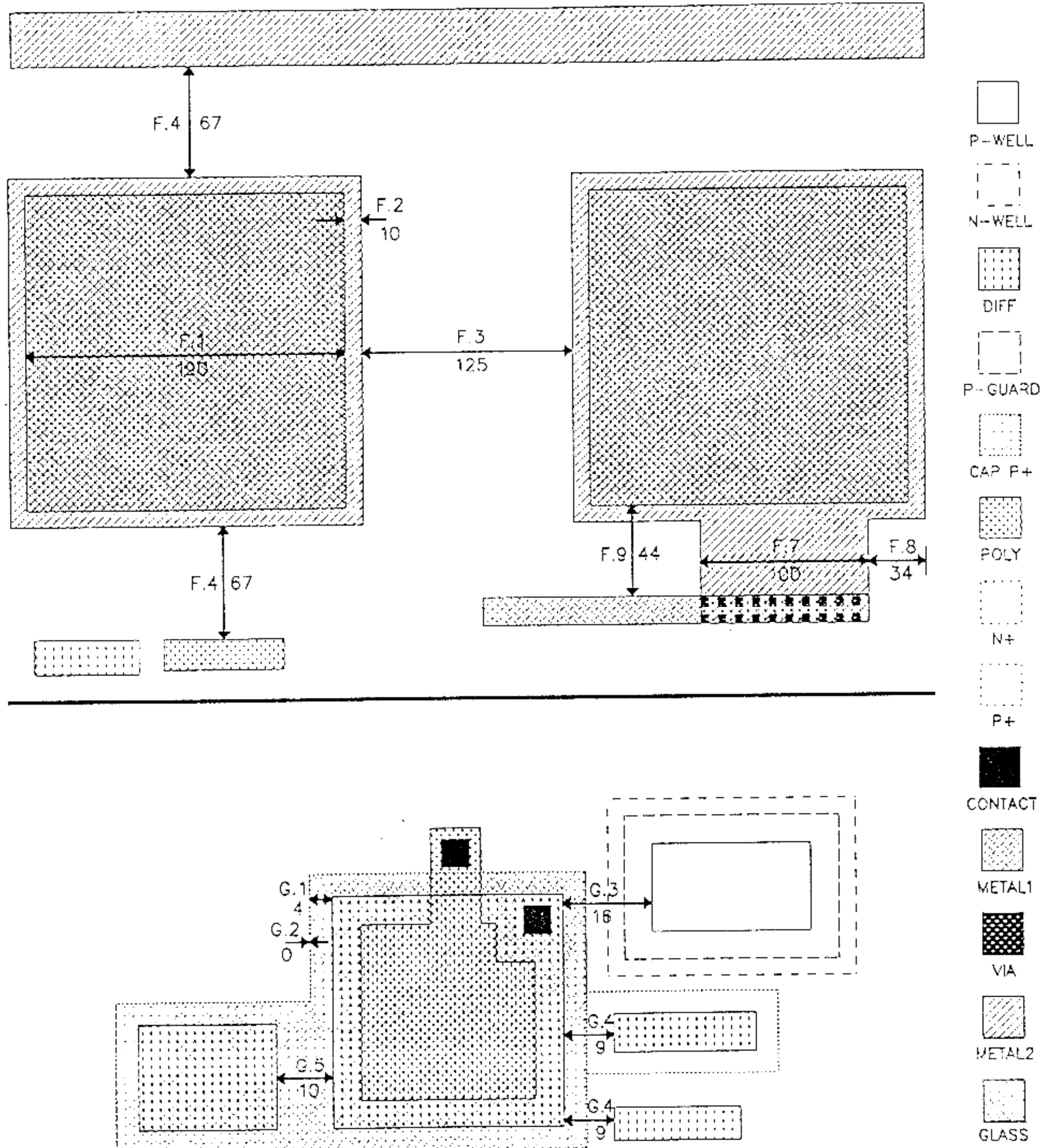


Figure C.3: CMOS3 DLM Pad and Capacitor Design Rules

Process Simulation

- CAD tools to verify processes
- Most common Supreme

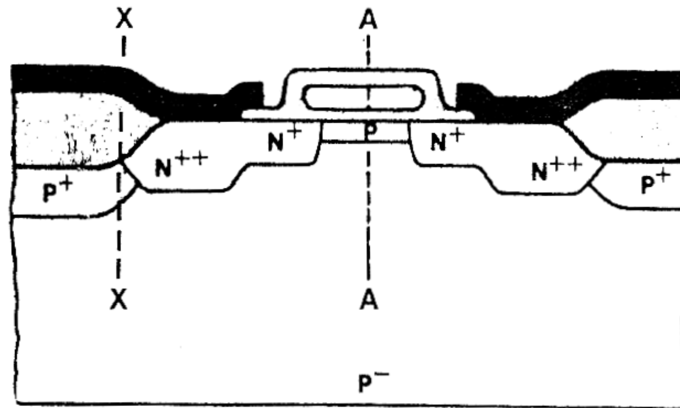


Fig. 9-6 1-D Process simulator can give accurate doping profiles in such regions of the device where the profile only changes in the vertical direction, as along cut line A - A. However, where the doping profile changes in the lateral direction such as in the region penetrated by the cut line X - X, a 1-D simulator will not provide an accurate result.

SUPREM

- Stanford University PRocess Engineering Model
- Now available from several commercial sources, Synopsys
- Added graphic interface

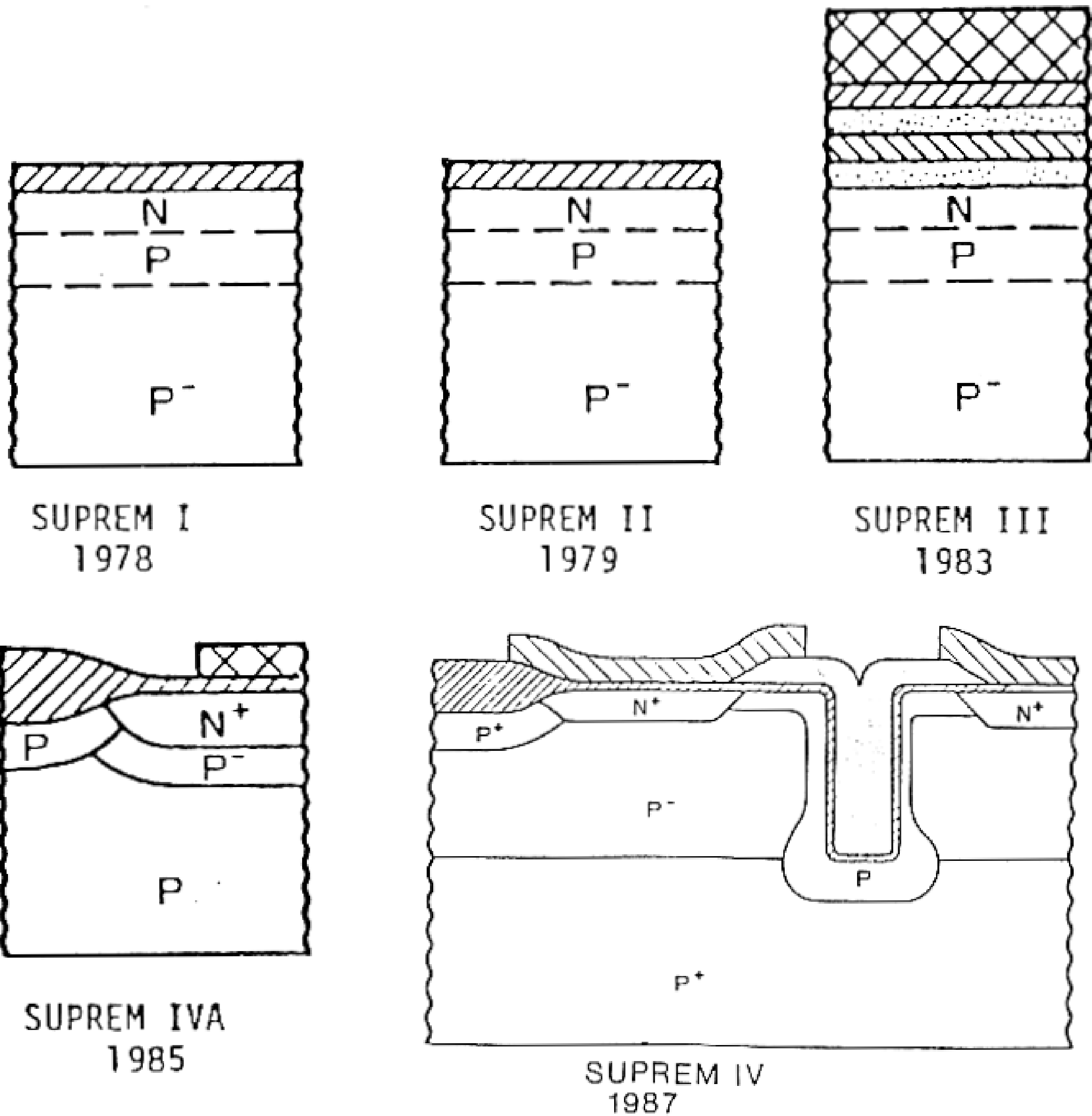


Fig. 9-7 History of the release of SUPREM codes.

Supreme Block Diagram

- Simple form: write text file description
- Still retains "cards": actually lines
- Useful when doing unique process
- When using specified process – design structure with Cadence
- Use fabrication technology that specifies steps
- eg CMOS18 (180 nm process)
- Chip design programs (eg cadence) export layout design
- Becomes an import to Supreme for device modeling
- Uses specific process parameters
- Output of Supreme input to device simulation files also
-

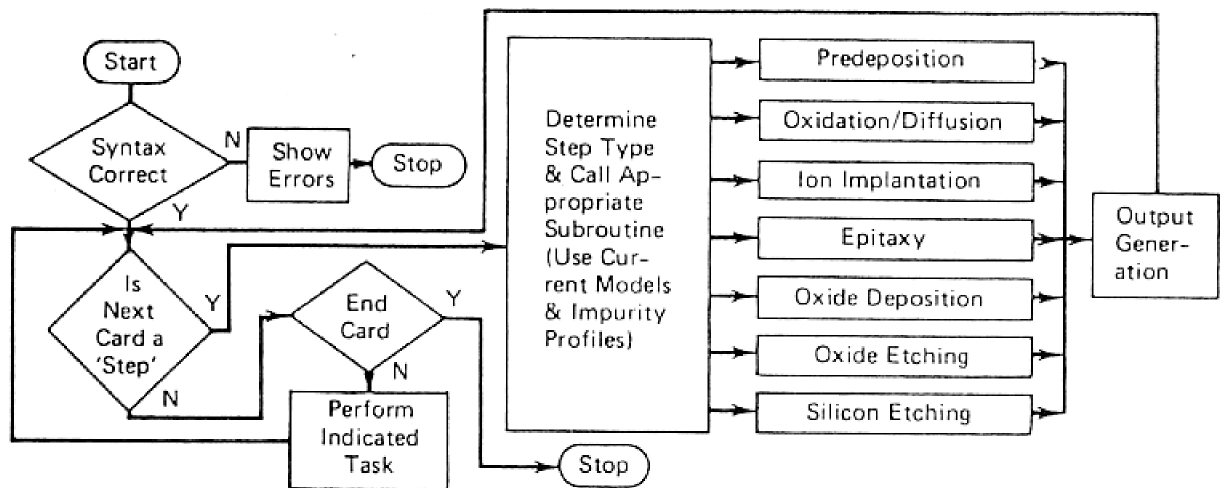


Fig. 9-8 Block flow diagram for the SUPREM II process-modelling computer program.

1 Dimensional Supreme Input

ONE-DIMENSIONAL SIMULATION EXAMPLE
Initial Active Region Simulation

```
$ TMA TSUPREM-4 -- Example 1 -- Part A
$ Bipolar active device region:
$       Buried layer and epitaxial deposition

$ Define the grid and initialize

line  x   loc=-0.5
line  x   loc= 0.5

line  y   loc=0     spac=0.25
line  y   loc=0.55  spac=0.02
line  y   loc=1.0   spac=0.15
line  y   loc=8     spac=1.0

initialize boron=1e15 line.dat

$ Select oxidation model
method erfc grid.oxi=4.0

$ Grow buried layer masking oxide
diffusion temp=1150 time=120 weto2

$ Etch the buried layer masking oxide
etch      oxide all

$ Implant and drive in the antimony buried layer
implant   antimony dose=1e15 energy=75
diffusion temp=1150 time=30 dryo2
diffusion temp=1150 time=360

$ Etch the oxide.
etch      oxide all

$ Grow 1.8 micron of arsenic doped epi.
deposition silicon thicknes=1.8 spaces=30  arsenic=5e15
diffusion temp=1050 time=6 arsenic=5e15

$ Grow pad oxide and deposit nitride
diffusion temp=1050 time=30 dryo2
deposition nitride thicknes=0.12

$ Save initial active region results
structure outfile=s4ex1as

$ Plot results
option device=ps
select    z=log10(antimony)  title="Active, Epitaxy" +
    label=log(Concentration)
plot.1d   x.v=0  y.min=13 y.max=21 x.max=5  line.typ=2
select    z=log10(arsenic)
plot.1d   x.v=0  ^axis  ^clear  line.typ=3
select    z=log10(boron)
plot.1d   x.v=0  ^axis  ^clear  line.typ=1

$ Label plot
label     x=2.1 y=18.2  label=antimony
label     x=4.2 y=15.1  label=boron
label     x=-.8 y=15.8  label=arsenic
```

Figure 4.1 - Listing of input file S4EX1A, for simulating the buried layer and epitaxial deposition for a bipolar transistor structure.

1 Dimensional Supreme Output

- These are similar to the 1D formulas for formulas
- However allows multi processes effects to be simulated

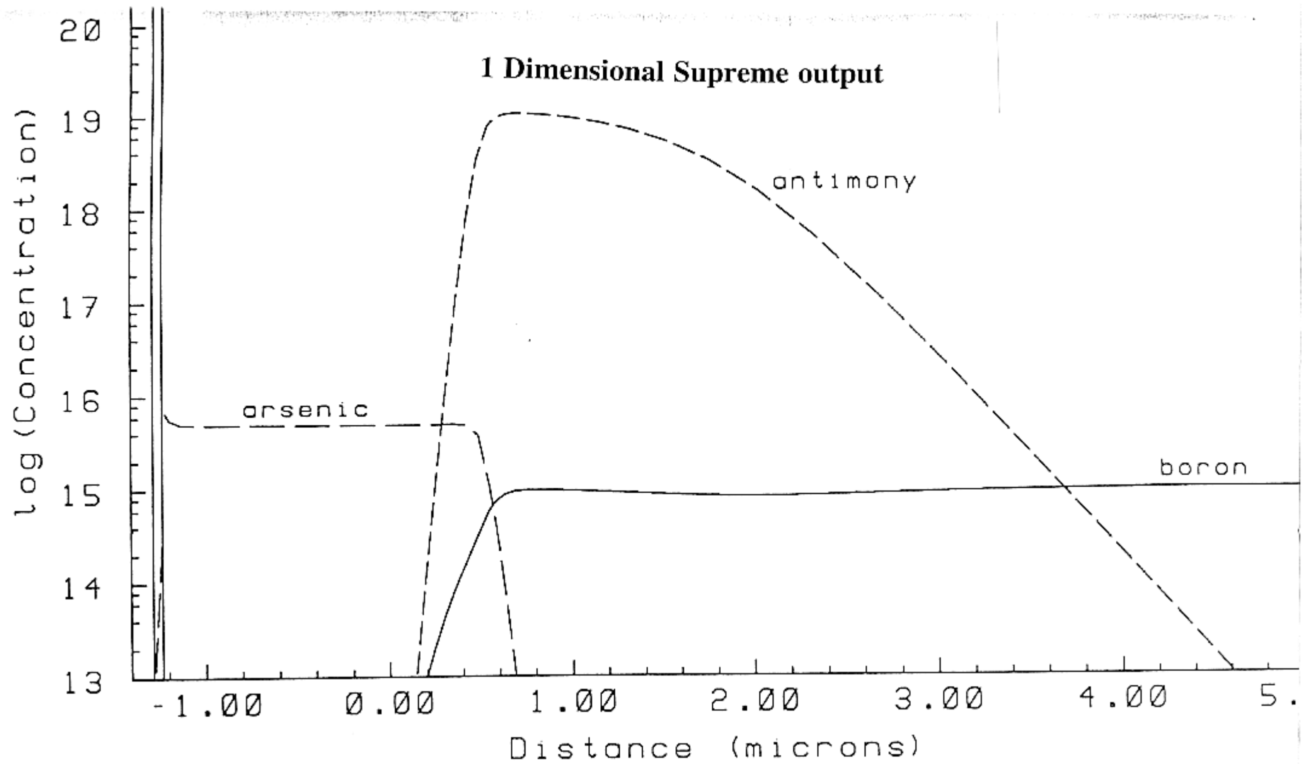
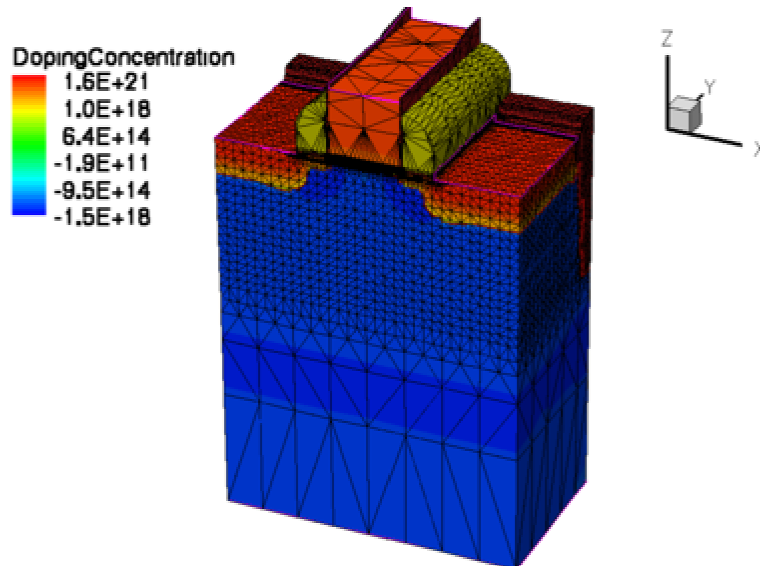


Figure 4.2 - Plot generated by TSUPREM-4 from statements in input file S4EX1A.

2D Supreme

- Must create Grid sufficient small for simulation
- High density grid in important areas, eg edges of structures
- Small grid spacing near edge of source/drain, active layers
- Often have small spaces at top, large in lower layers

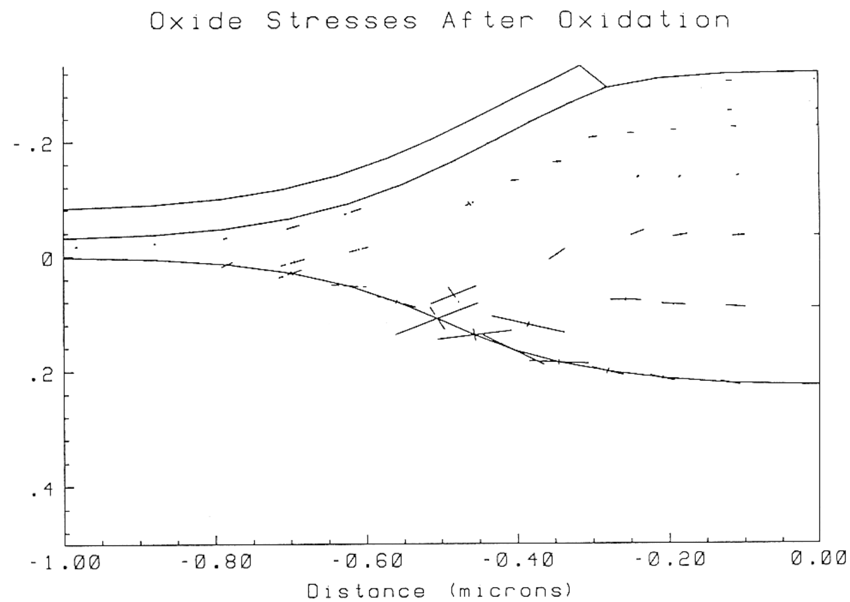



```
$ TMA TSUPREM-4 narrow window example
$   Part 1:  Oxide shape

$ Set up the grid
line   x    loc=-1.5   spac=.15
line   x    loc=-0.25  spac=.05
line   x    loc=0      spac=.1

line   y    loc=0      spac=.03
line   y    loc=0.5    spac=.1

$ No impurities, for faster oxidation simulation
initialize

$ Deposit pad oxide and define nitride mask
deposition oxide   thicknes=0.03 spaces=2
deposition nitride thicknes=0.05
etch       nitride right p1.x=-.25

$ Plot the grid
option     device=ps
select     title="Grid for Oxidation"
plot.2d    grid  scale

$ Do the oxidation
method     viscous  grid.oxi=4  init=.15
diffusion temp=1000 time=100   weto2
structure outf=s4ex2as

$ Plot the final structure, showing stress
select     title="Oxide Stresses After Oxidation"
plot.2d    stress vleng=.12 line.ten=2  x.min=-1
```

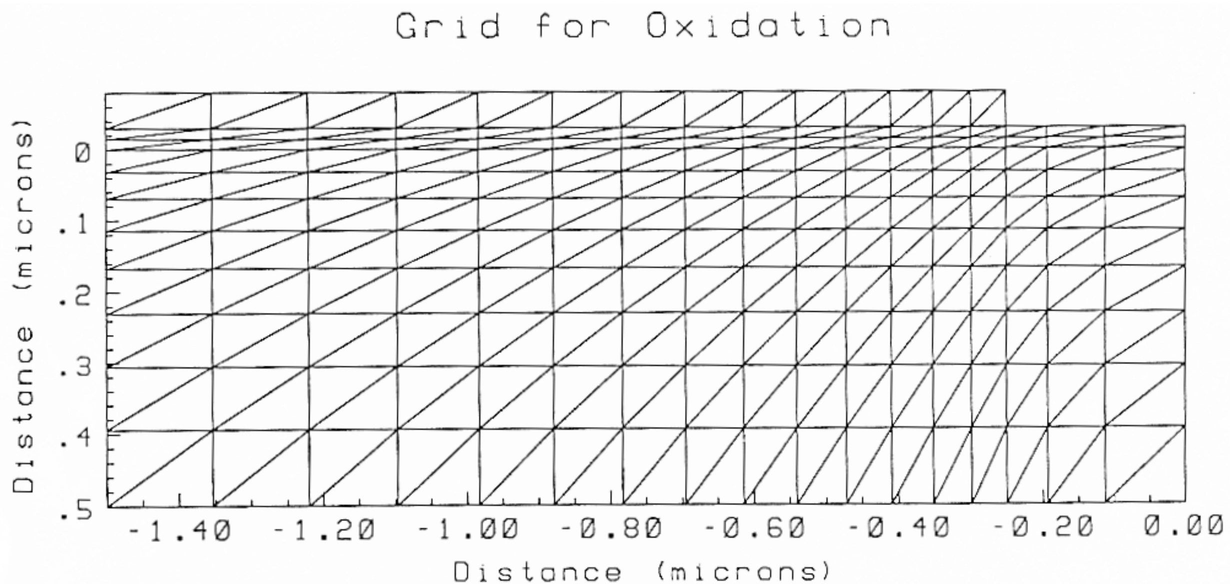
Figure 5.1 - Listing of statement input file S4EX2A, for determining LOCOS shape.

2D Supreme Output: Locos process

- Can simulate Local Oxidation process (SiN patterning of oxide)
- Diffusion of oxygen & stress in SiN show shape of oxide
- Important test: cut grid space by 1/2 and see if generates same
- Keep reducing until next smaller produces the same
- Issue: calculation time goes up by 4 when do this



ıre 5.3 - Result of oxidation simulation, showing oxide shape and stresses.



igure 5.2 - Mesh used for oxidation simulation. Produced by PLOT.2D GRID statement in input file S4EX2A.

Trench Capacitors in Supreme IV

- Simulate full etch and deposition processes
- Must use complex grid for non-rectangular structures
- Eg sloped sidewalls of trench
- Full 3D Supreme even more complex grid
- Requires high computation power/time

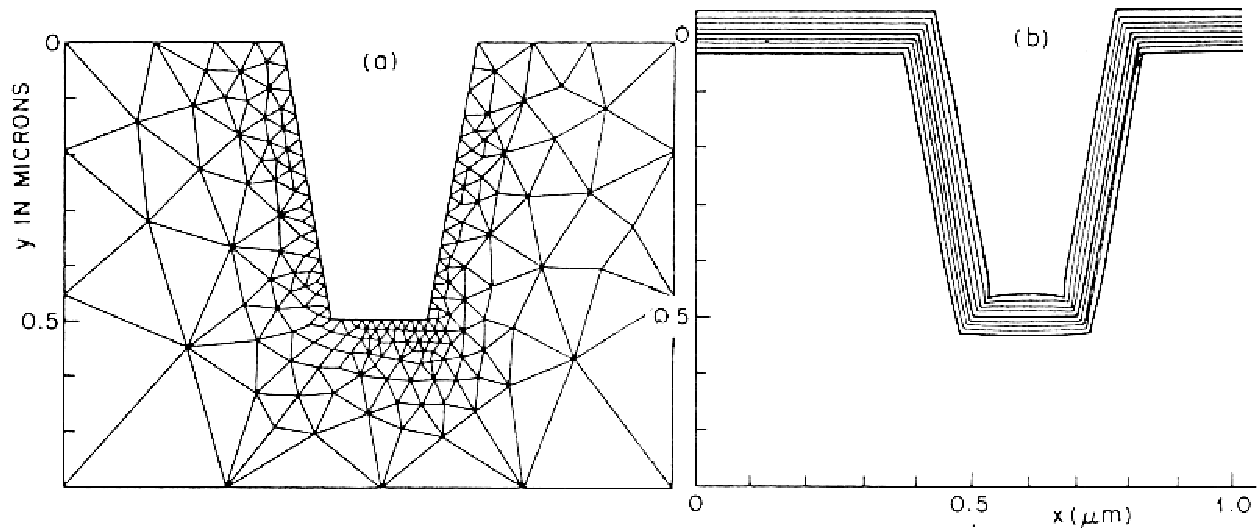


Fig. 9-33 Oxidation of a trench structure using SUPREM IV. (a) Initial grid. (b) Final oxide profile.