Course Outline 2016-1
ENSC495/851: Introduction to Microelectronic Fabrication
(ENSC 495, 4 credits, 2-0-4: ENSC 851, 3 credits, 2-0-1)

Professor:

Glenn Chapman, Rm ASB 8831, Phone: 778-782-3814,
email: glennc@cs.sfu.ca

Description

- Hands-on introduction to Integrated Circuit Fabrication.
- lectures: theoretical background & application of IC fabrication processes
- laboratory gives practical experience of each process
- Students build an IC from the bare silicon to final working device.

Primary text:

- "Introduction to Microelectronic Fabrication, 2nd ed", Richard C. Jaeger, Prentice Hall 2002
- Notes downloadable from

web:www.ensc.sfu/~glennc/e495out.html

Other references:

- "Microelectronic Processing", W.S. Ruska, McGraw-Hill
- "The Science and Engineering of Microelectronic Fabrication", Stephen Campbell, 2nd ed, Oxford Univ. Press.

Laboratory Engineer & TA's

- Lab Engineer: Andras Szigeti, aszigeti@sfu.ca Rm ASB 8832
- TA: Amin Rasouli, mrasouli@sfu.ca

Class notes and website
http://www2.ensc.sfu.ca/~glennc/e495out.html

Prerequisite:

- Students need understanding of basic transistor & diode operation.
  ENSC 220/ENSC 225 (Electronic Design I) or equivalent and application to the class

Lecture Schedule

- Lecture: Tuesday 17:30 - 19:20 SCEB1012

Week 1: Clean Room Technology & Silicon Wafer Production

- Basic outline of fabrication process: with to real structures.
- Theory behind clean room operations:
- History of semiconductor devices: diodes, transistors, Germanium/Silicon transition, monolithic integrated circuits
- Basic operation of Transistors, diodes
- Projected trends in Fabrication
- Theory and operations for contamination elimination, and safety issues.
- Silicon wafers; Crystallography, Production and Defects:
- Basic silicon wafer parameters, solid solubility of dopants in silicon, defects, and basic economics of operations.

Week 2: Thermal Oxidation

- Basic theory of the silicon oxidation, practical operations and measurement of films (thickness and quality).
- Tsupreme 4 simulation package introduction

Week 3: Lithography

- Basic operation of photolithography, chemical basis of photoresist, exposure equipment, exposure/development theory, and problems.

Week 4: Advanced Lithography
- Dealing with defects and exposure effects
- Advanced Lithography, Deep UV, Extreme UV, X-ray

Week 5: Etching
- Theory and operations of etching in general;
- Wet (chemical) etching of oxides

Week 6: Etching II
- Wet etching of silicon and metals

Week 7: Diffusion Processes & Ion Implantation
- Diffusion theory (constant, limited source, multisource).
- Theory and operation of Ion implantation doping techniques.

Week 8: Thin Film Deposition: Evaporation and Sputtering
- Theoretical and experimental operation of vacuum systems.
- Theory and operation of evaporation and sputtering systems

Week 9: Thin Film Deposition: Chemical Vapor Deposition
- Theory and operation of Chemical Vapor Deposition (CVD), Plasma Enhanced CVD
- Film thickness measurement and film problems

Week 10: Expitaxy CVD and Dry Etching Processes
- Expitaxy (deposition with same crystal structure) & laser CVD
- Dry etching processes (Plasma, Sputtering and Reactive Ion)

Week 11: Packaging, Yields, Processing Silicon Foundries
- Testing, dicing of wafers, packaging, bonding, yield theory and measurements.
- Measurement techniques: Optical microscope, Scanning Electron Microscope, energy dispersive analysis of X-rays, Augue analysis, Secondary Ion Mass Spectroscopy (SIMS), Laser Ion Mass Spectroscopy (LIMS), Rutherford Backscatter Spectroscopy (RBS), X-ray diffraction.
- Silicon Foundries

Week 12: CMOS and Bipolar Process Integration in practice
- Layer by layer process of sample CMOS and Bipolar
- Yield Analysis
- Using mask design tools

Week 13: Future of the processing
- Problems in submicron technology and Micromachining/sensors as a new fabrication area.
- Summary of main course points.

Laboratory Section

Labs: LA01 Wed. 17:30-21:20, ASB 8823
LA02 Thur. 14:30-18:20, ASB 8823 (if class is large enough)

Projects in Microfacation Lab

Students will work in 3-4 people teams which start with a bare silicon wafer and create finished IC's which include diodes, solar cells, transistors and some characterization test devices. All the process steps will be done by the students, who will also characterize the parameters for each step. Electrical characterization of the devices (diodes etc) will also be accomplished. Students get to keep samples of their own IC's. Two Laboratory reports must be submitted.

Week 1: Tour of Microfabrication facilities

- Tour of the microfabrication facilities, inspection of chips under microscopes. Learn to don clean room suits, gloves, handling wafers, use of tweezers

Week 2: Demonstration of laboratory processes

- Demonstration of oxide growth: learning how to preoxidation clean wafers, run oxidation furnaces, control of flow values, insertion/withdrawal of wafers, and measure the oxides.

Week 3-5: Growth/patterning of oxide film & P diffusion

- Set up furnace and grow oxide to stated thickness.
  measurement oxide thickness
- Characterize grown film: measure thickness.
- Pattern the first oxide layer
- P diffusion (source/drain and bipolar base)
- First Lab report done on this work

Week 6-13: Build simple 4 level structures:

- Build simple diffused diode, solar cells and test structures.
- Clean wafers, grow oxide, define oxide layers with photolithography.
- N+ diffusion (source/drain & bipolar collector) measure results.
- Oxide regrowth, measure thicknesses.
- Define contact cuts, etch oxide, inspect and measure contact size.
- Learn operation of simple sputter coater (thin film deposition).
- Deposit metal and measure thickness via profilometry.
- Deposit metal (contacts and gate), define/etch, measure thickness and line widths.
- Measure simple diode and transistor characteristics.
- Measure test devices: metal and diffusion sheet resistance, contact chains

Assignments

Assignments will be given every 2-3 weeks after the second week of class. Assignments will be emailed to the students. Each student gets a separate assignment with the same questions but different parameters and solutions. You will be emailed a solution set to your specific questions. If you used someone else's numbers you get zero on the question. If you do that twice within one assignment you get zero on the assignment. Happens on a second assignment an academic dishonesty report is filed.

Mid Term and Final Exam

- One mid term test (about week 6) and final examination

Tutorial/Problem Workshops

Tutorials will be held on an as announced basis (not every week but about every 2nd week). These will involve workshops where a problem is assigned, worked through in groups, and then solutions given. Typically 2 problems per session. Mostly these will be done during the lab portion, but there may be some extra sessions.

Graduate Students

Graduate students in the MASc or PhD program have two options.

- They can take the lab up to end of Week 5 and do the first report, and then do a Major processing project in the laboratory during the rest of the course. Major projects are only available for graduates doing microfab involved research in their thesis program.
- Alternatively they may do the entire laboratory like the undergraduate, with two Lab reports and extended tests on lab 2.

Mark Distribution

Student will receive the highest of the following distributions:

ENSC 495

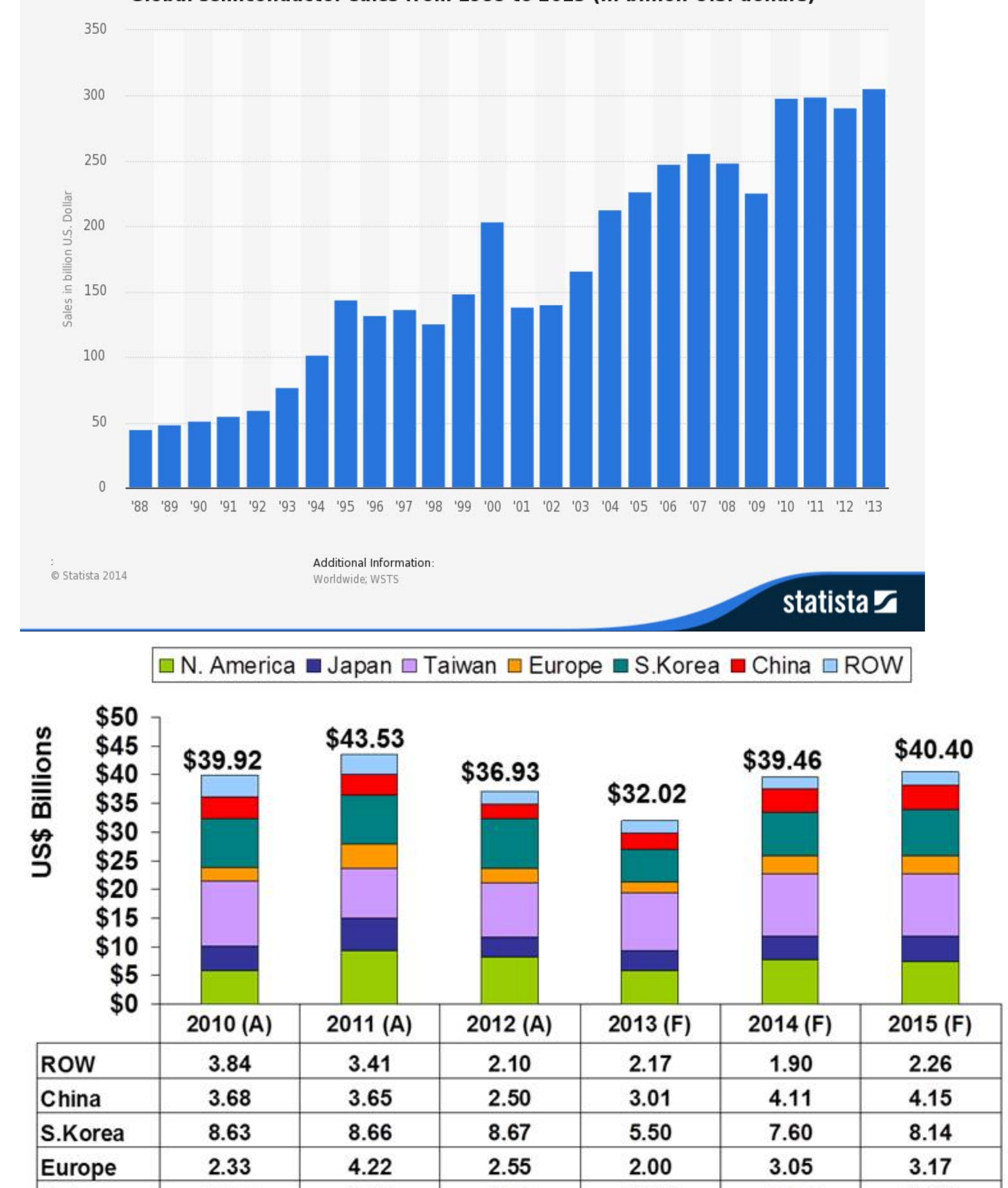
- 30% laboratory reports, 20% problem assignments, 10% mid term, 40% final exam.
- 25% laboratory reports, 25% problem assignments, 50% final exam.

ENSC 851

- 30% lab reports, 20% problem assignments, 10% mid term, 35% final exam.
- 25% lab reports, 40% Major Project, 20% problem assignments, 15% mid term.

Electronics Industry
World's Largest Manufacture

- Global Market: ~ $US336 Billion/year (2015)
- Current Growth 0.2%
- Largest manufacturing industry in the world
- Semiconductor fab equipment ~ $US45 Billion/year



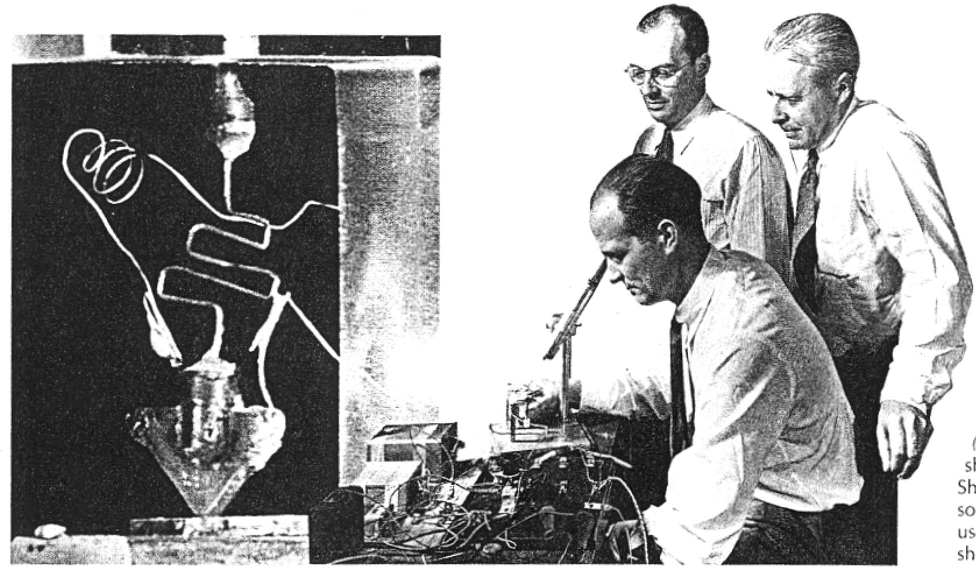
	2010 (A)	2011 (A)	2012 (A)	2013 (F)	2014 (F)	2015 (F)
ROW	3.84	3.41	2.10	2.17	1.90	2.26
China	3.68	3.65	2.50	3.01	4.11	4.15
S.Korea	8.63	8.66	8.67	5.50	7.60	8.14
Europe	2.33	4.22	2.55	2.00	3.05	3.17
Taiwan	11.25	8.52	9.53	10.19	10.99	10.98
Japan	4.44	5.81	3.42	3.41	4.08	4.24
N. America	5.75	9.26	8.15	5.74	7.73	7.46

Totals may not add due to rounding

Source: SEMI, December 2013

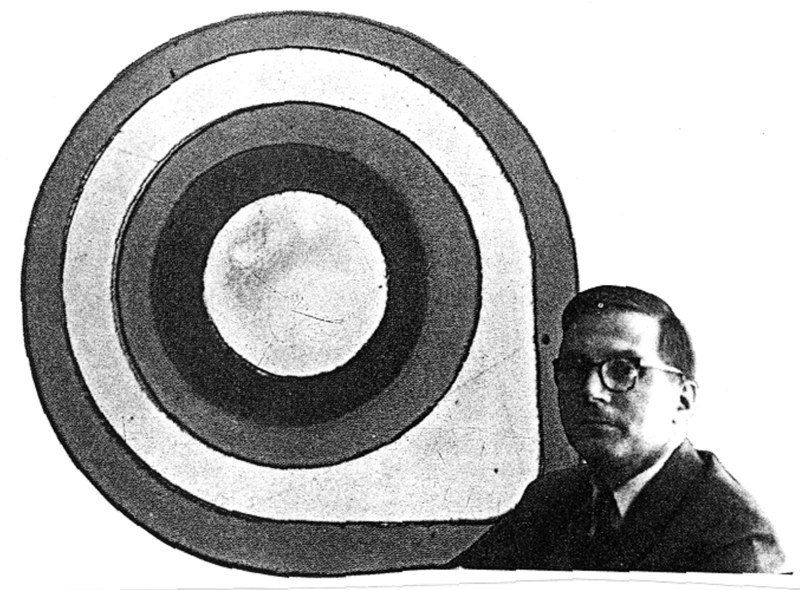
Transistor Inventors

- Bardeen, Brattain and Schockley at Bell Labs 1947
  First Transistor (bipolar point contact)



Bell Laboratories scientists John Bardeen and Walter Brattain *(standing, left to right)* look over the shoulder of colleague William Shockley, seated at a microscope and some of the other apparatus that was used to invent the first transistor, shown at far left about half life size.

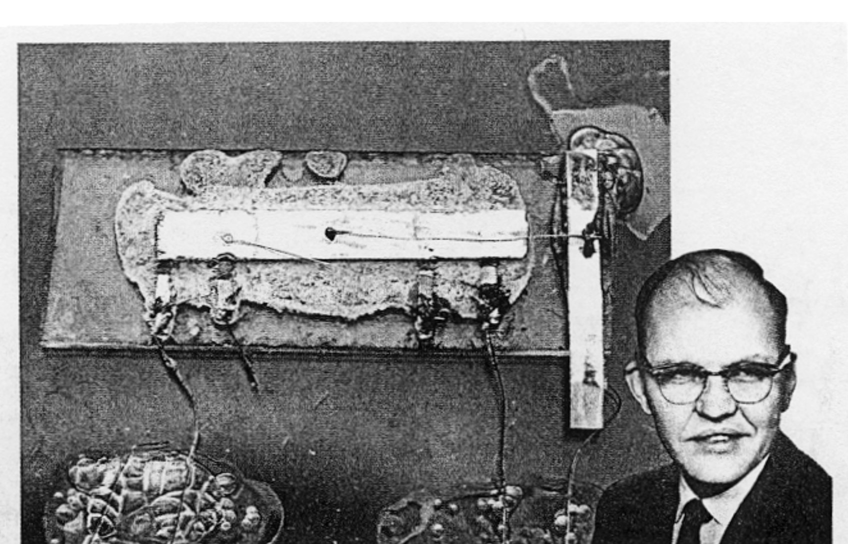
- First planer transistor
  Jean Hoerni at Fairchild 1959



The first planar (flat) transistor, shown with its inventor, Swiss physicist Jean Hoerni of Fairchild Semiconductor, was about 6/100 inch in diameter. Simpler to make than the devices that preceded it, the planar transistor became the basis for the first mass-produced chips *(opposite)*.

Integrated Circuits

- A monolithic (single substrate) collection of devices
- First proposed by G. W. Drummer, UK 1952
- First produced by Jack Kilby of Texas Instruments 1958
  Received Nobel Prize in 2000 for microchip development
- First Silicon IC Robert Noyce of Fairchild 1959



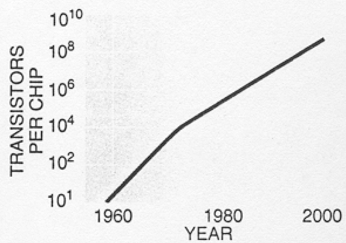
The first integrated circuit, invented in 1958 by Jack St. Clair Kilby of Texas Instruments, combined all the basic circuit elements in a single piece of germanium less than half an inch long *(horizontal bar)*. The device was held together by glue, with gold wires providing interconnections.

Early in 1959, Robert Noyce of Fairchild constructed an integrated circuit on a thin slice of silicon. Built-in metal conductors *(white)* linked to cone-shaped transistors and bar-shaped resistors *(blue)* eliminated the wires of Kilby's chip and made for easier mass production.

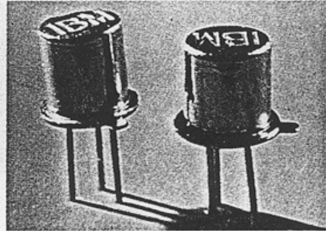
Shrinking Transistor

The Shrinking Transistor

Miniaturization is manifest in this comparison between an electromechanical switch, circa 1957, and a recent chip containing 16 million bits of memory (*right*). Progress appears in these snapshots (*counterclockwise*): Bell Laboratories' first transistor (1948); canned transistors (1958); salt-size transistors (1964); 2,000-bit chip (1973); boards with 185,000 circuits and 2.3 megabits of memory apiece (1985); and a 64-megabit memory chip (1992).

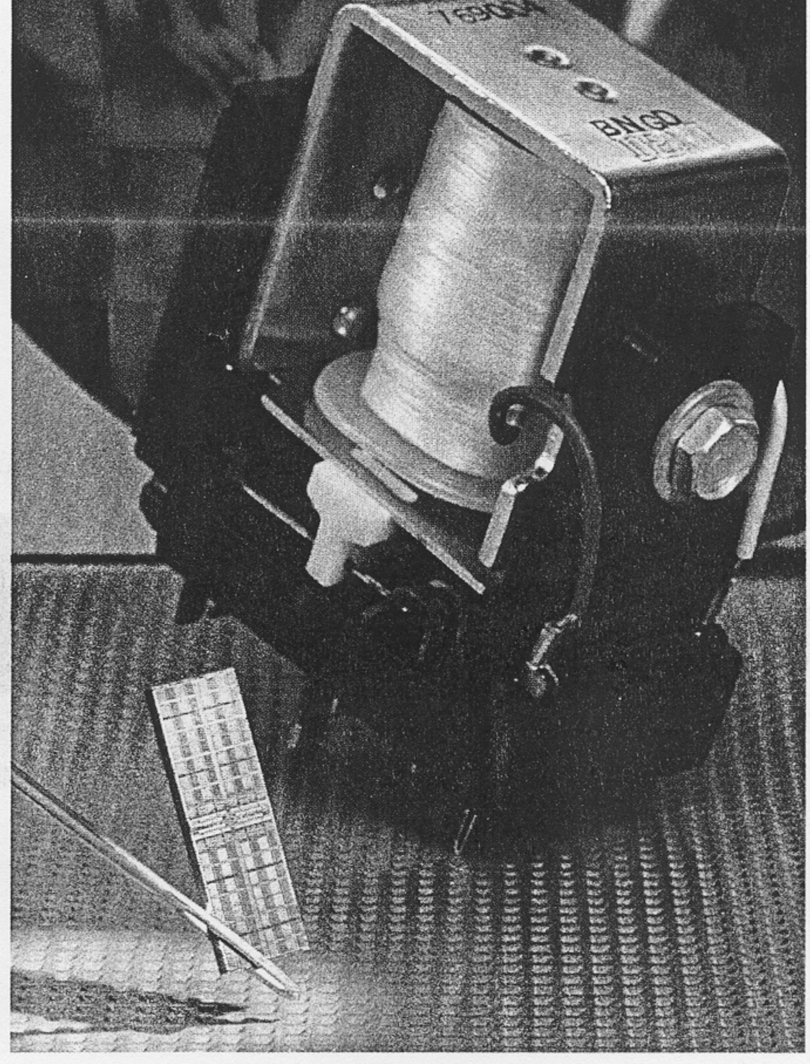


The first transistor

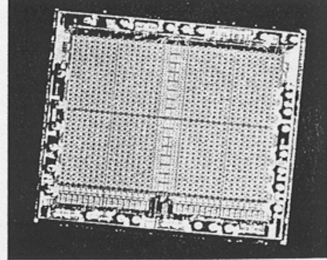


Early commercial transistors

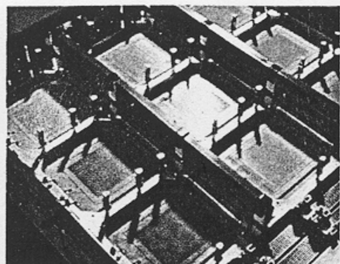
Salt-size transistors



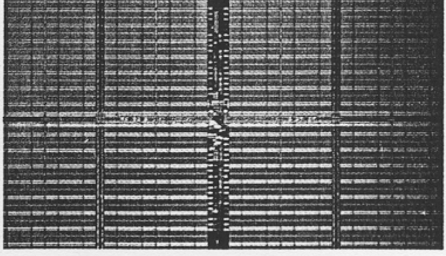
Switches, now and then



Early integrated circuit



Circuit assembly



Contemporary memory chip

Simple MosFet Transistor

- Need to create a isolated gate between source & drain
- Originally metal gate, now all polygate

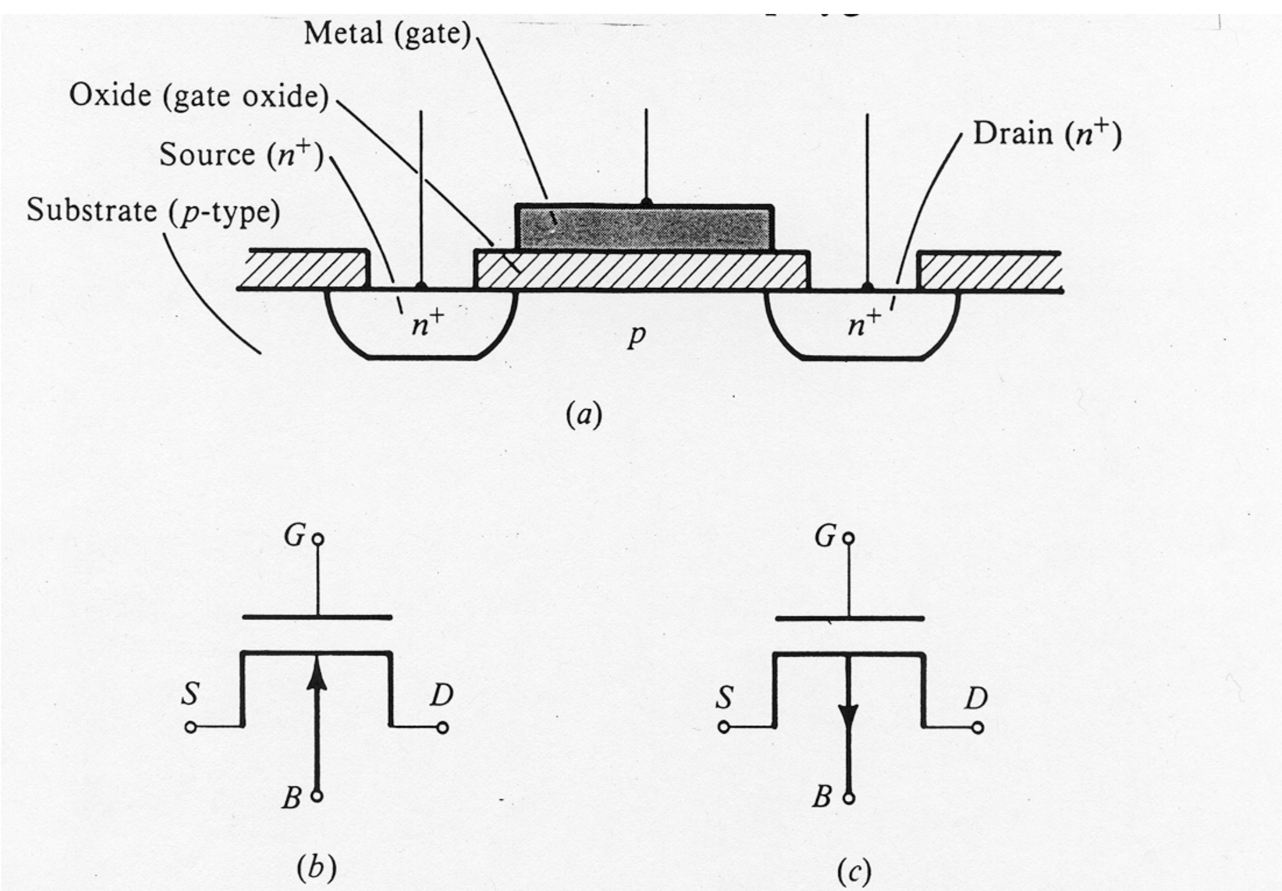


Figure 11-1 The MOS transistor. (*a*) Diagram of an MOS transistor, showing gate, gate oxide, source, and drain. (*b*) Symbol for an *n*-channel MOS transistor. (*c*) Symbol for a *p*-channel MOS transistor.

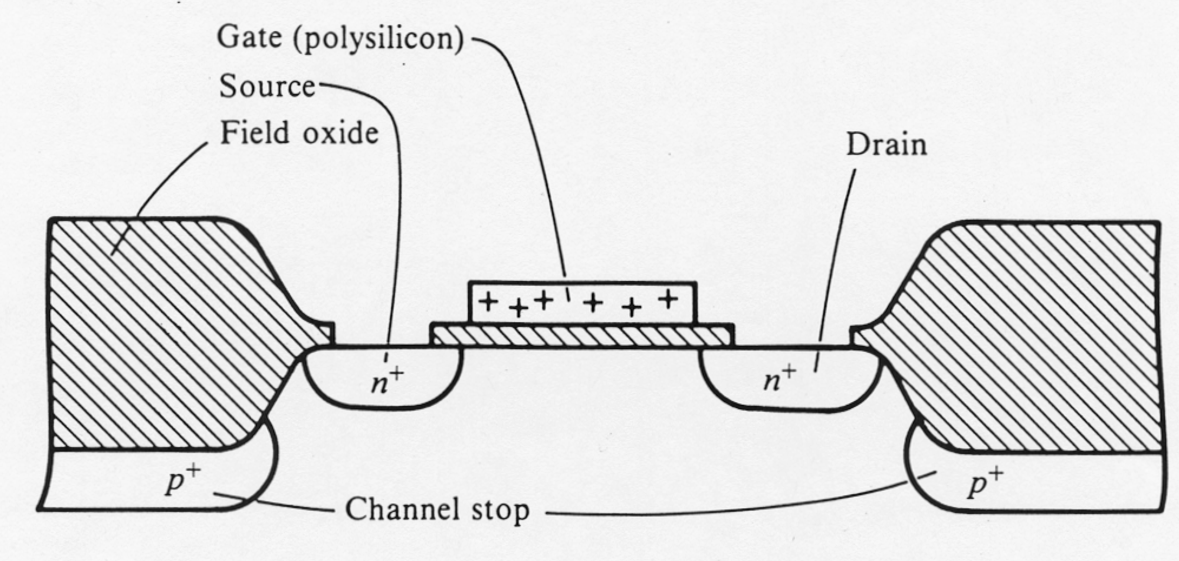


Figure 11-4 Cross-section of a practical NMOS transistor.

MOSFET Threshold and Low Drain voltage

- When gate exceed threshold ($V_G >> V_T$)
- Now channel filled with electrons: resistance reduced
- Note: this is called an **enhancement mode FET**
- Positive drain voltage causes carrier flow
- Get linear behavour: called Triode or Linear region
- Higher gate voltage, more inversion, more carriers
  lower resistance and higher current flow
- As Drain voltage increase current flow
  causes voltage drop in channel
- Larger drain depletion region (more reverse biased)
- But carriers near drain decrease until get pinchoff
- Pinchoff or saturation voltage V_{Dsat}

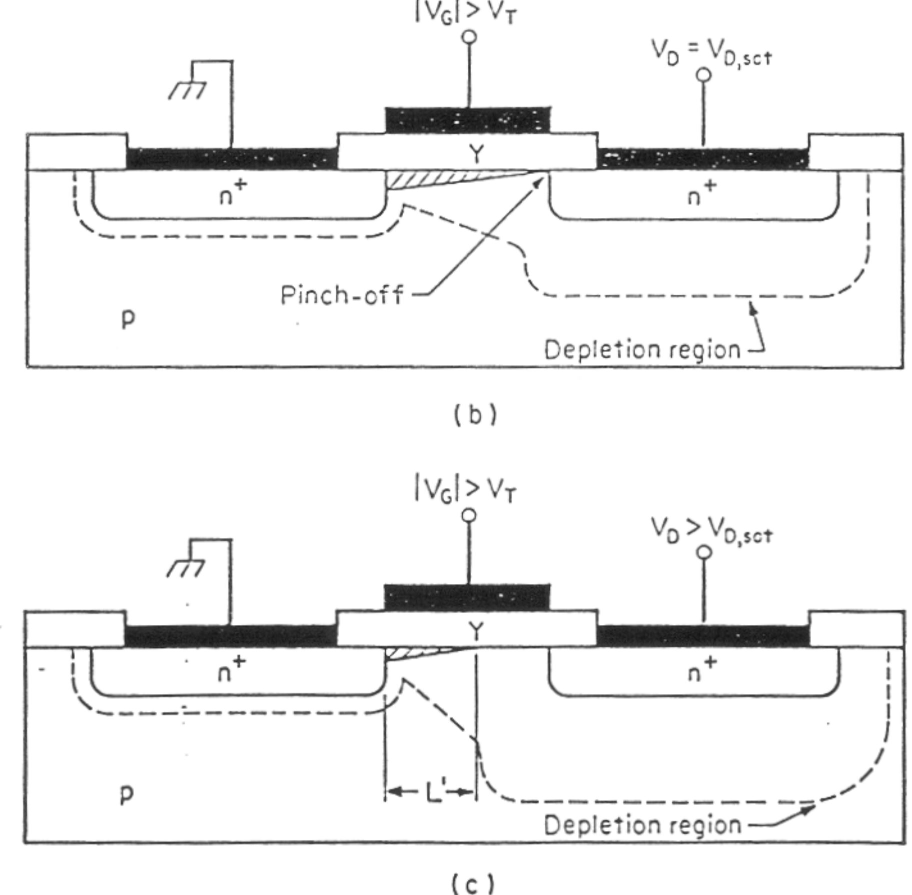
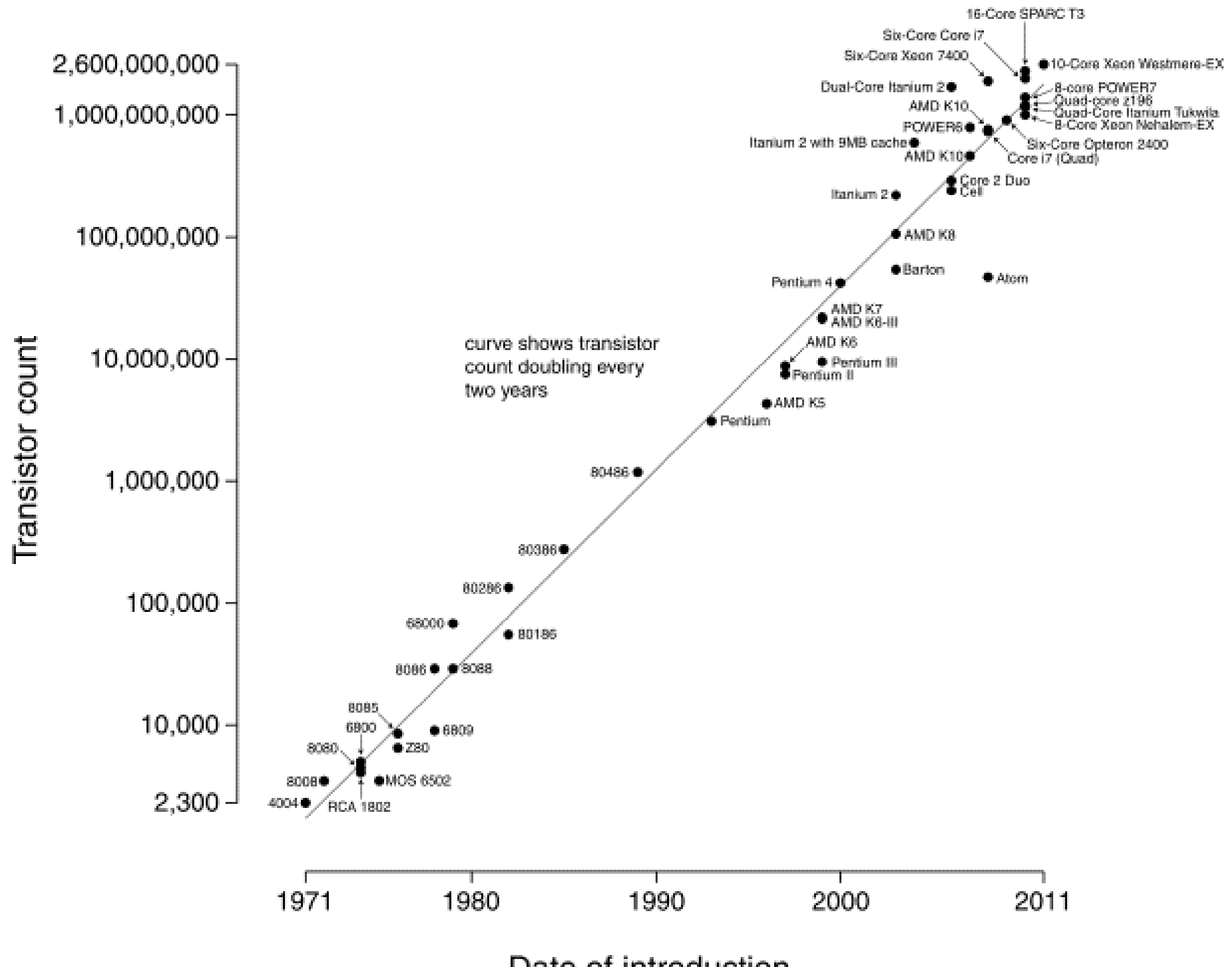


Figure 5-2 Device cross section in (*a*) triode region, (*b*) onset of saturation, and (*c*) beyond saturation. (*After Ref. 3-2.*)

Increasing Density of Devices

- Growth with time - Transistors numbers/Chip
- Increase by 5000x in 15 years!
- More value per chip

Microprocessor Transistor Counts 1971-2011 & Moore's Law



Moore's Laws

- Moore's laws show industrial trends with time
- Source: Semiconductor Research Corp.: ISIS '96 conf.

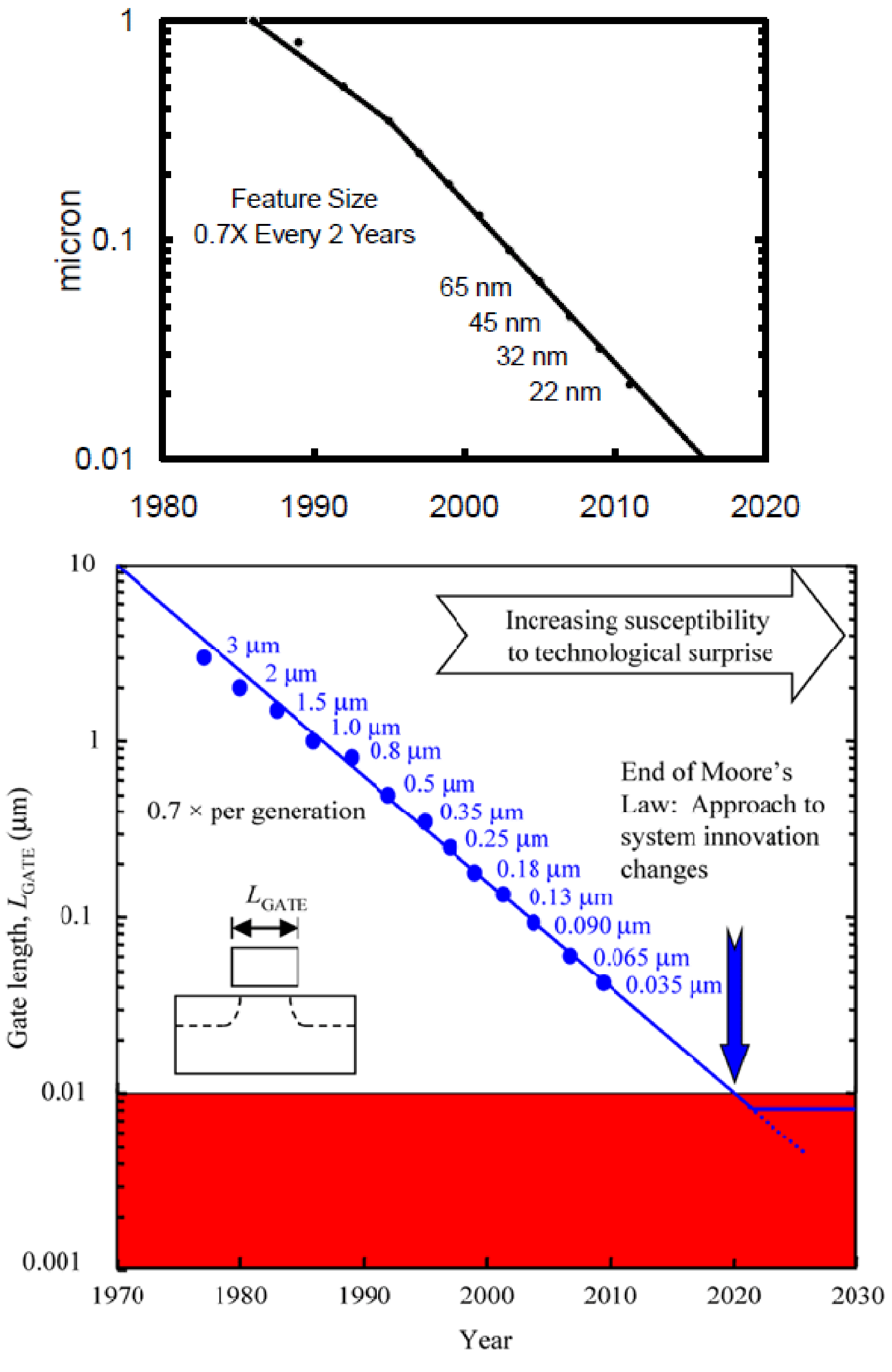
Moore's Law

- Trend Projections

		2004
Die Area	1.5x every 3 yrs.	6.5 cm^2
Min. Feature size	30% reduction every 3 yrs.	0.13 μm
Transistors/die	4x every 3 yrs.	4 Gb DRAM
Ckt. On-Chip Clock	1.5x every 3 yrs.	1 GHz μP
Cost/Transistor	.50% reduction every 3 yrs.	$0.0001 (Logic)
Fab Cost	2.3x every 3 yrs.	$8B !!

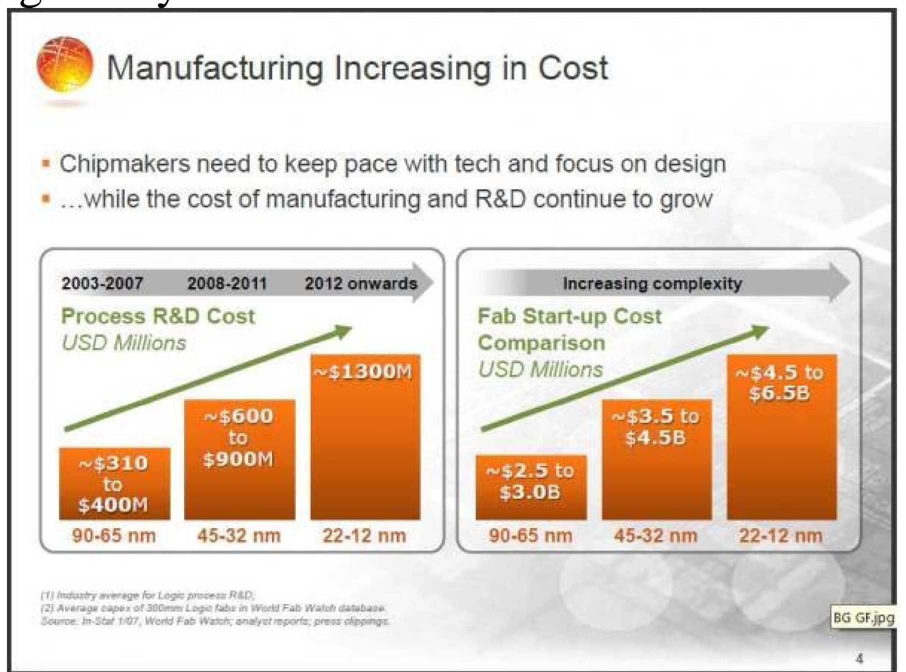
Transistor (MOSFET) Dimensions

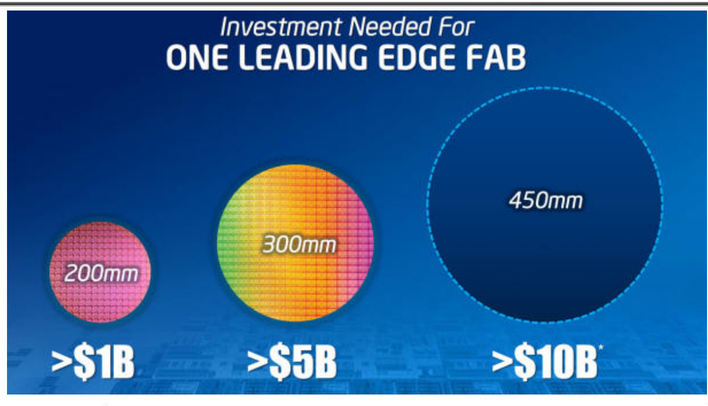
- Transistor scale shrinkages
- Width of device
- Depth of device in Silicon
- Thickness of critical films

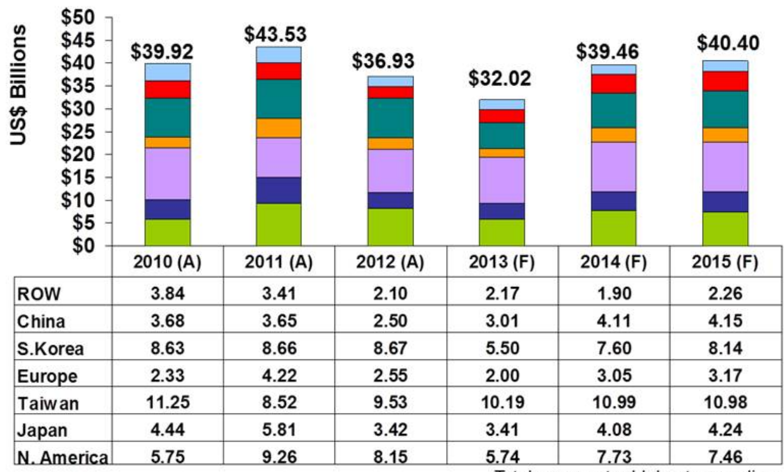


Fab Capacity vs Cost

- Fab capacity grows slowly
- Costs rising 32%/year: source Semiconductor Research Corp.







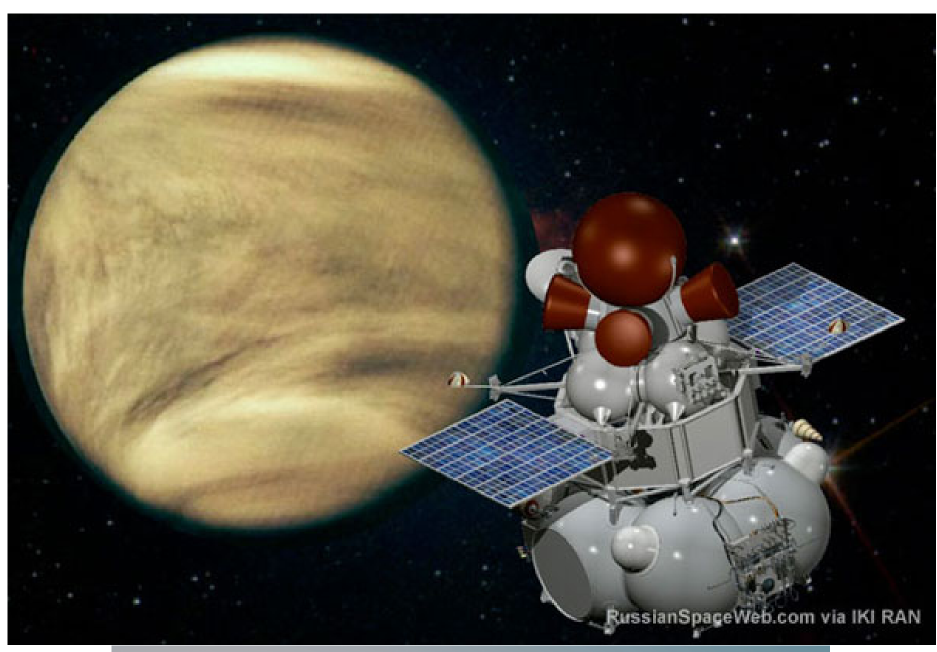
	2010 (A)	2011 (A)	2012 (A)	2013 (F)	2014 (F)	2015 (F)
ROW	3.84	3.41	2.10	2.17	1.90	2.26
China	3.68	3.65	2.50	3.01	4.11	4.15
S.Korea	8.63	8.66	8.67	5.50	7.60	8.14
Europe	2.33	4.22	2.55	2.00	3.05	3.17
Taiwan	11.25	8.52	9.53	10.19	10.99	10.98
Japan	4.44	5.81	3.42	3.41	4.08	4.24
N. America	5.75	9.26	8.15	5.74	7.73	7.46

Totals may not add due to rounding

Source: SEMI, December 2013

Counterfeit Semiconductors

- Big problem – high end chips so expensive
- Getting widespread counterfeiting of
- Chips for special applications, aircraft, space, military
- Process for higher temperature range. Resist radiation
- Eg cost of regular memory chip <$10, rad hard $30,000
- Repackage cheap chips in high end packages
- Fake manufacturing
- Russian Phobos-Grunt mission – to Moons of Mars
- Failed because memory chips turned repackage as rad hard
- Cost $500M mission failed.
- Us nuclear subs – supplied charge with fake chips



Semiconductors

- Conductor s (eg copper/aluminum) very low resistance
- Insulators very high resistance
- Semiconductors moderately resistances: modifiable to lower values
- Wire 1 mm sq by 1 m long 300,000 ohms: native silicon
- 0.1% impurity decrease the wire by $3x10^8$ X to 0.001 ohms
- Electrons are more tightly bound than metals
- But much looser than insulators.
- Crystal structure: diamond like tetrahedral
  (each atom bonded to 4 others)
- Semi shiny
- Mono semiconductors: Column 4 in the periodic table:
  eg Germanium, Silicon, Diamond and Grey Tin
- Covalent bonding: sharing of electrons between two atoms
- N type dopants, from column V:
  add extra electrons (negative charges)
- P type dopants, from column III:
  create holes (act as mobile positive charges)

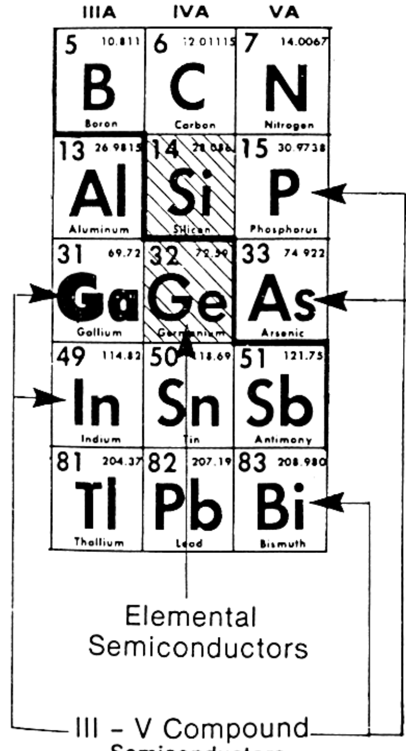


Figure 2.6 Semiconductor materials.

Binary and Ternary Semiconductor

- Mono semiconductors: Column 4 in the periodic table:
- If average 4 electrons/atom get similar materials
- Covalent bonding: sharing of electrons between two atoms
- Binary semiconductors:
  mixture of two elements that average 4 outer electrons.
  eg. III-V materials
  (GaAs: Gallium Arsenide, InP: Indium Phosphide),
  or II-VI materials
  (CdS: Cadmium Sulphide, HgTe: Mercury Telluride).
- NOTE: not all combinations are semiconductors

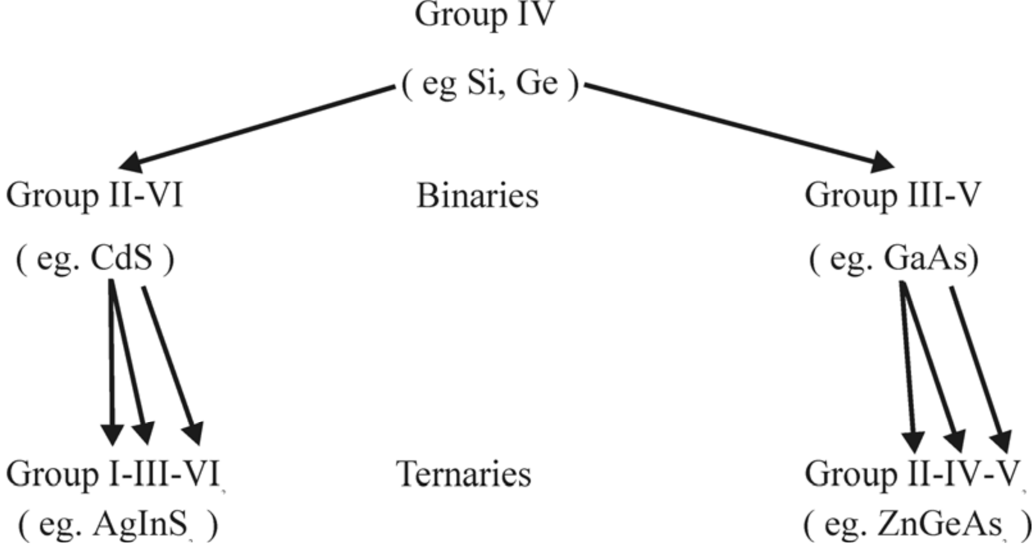


Table 2-1 Important properties of common semiconductors

	Ge	Si	GaAs
Atomic or molecular weight (amu)	72.6	28.09	144.63
Atoms or molecules ($cm^{-3} \times 10^{22}$)	4.4	5.00	2.21
Lattice constant (nm)	0.566	0.543	0.565
Density ($g\ cm^{-3}$)	5.32	2.33	5.32
N_c ($\times 10^{17}\ cm^{-3}$)	104	28	4.7
N_v ($\times 10^{17}\ cm^{-3}$)	60	104	7.0
E_G (eV)	0.67	1.11	1.40
n_i (cm^{-3})	2.4×10^{13}	1.45×10^{10}	9×10^{6}
Intrinsic lattice mobilities ($cm^2\ V^{-1}\ sec^{-1}$)			
Electrons	3900	1350	8600
Holes	1900	480	250
Dielectric constant	16.3	11.7	12
Melting point (°C)	937	1415	1238
Vapor pressure (torr)	10^{-7} (@ 880°C)	10^{-7} (@ 1050°C)	1 (@ 1050°C)
Specific heat ($J\ g^{-1}\ °C^{-1}$)	0.31	0.7	0.35
Thermal conductivity ($W\ cm^{-1}\ °C^{-1}$)	0.6	1.5	0.81
Linear coefficient of thermal expansion (ppm)	5.8	2.5	5.9

Crystal Structure

- Most semiconductor crystal structure:
  diamond like tetrahedral
- Each atom bonded to 4 others
- With binary follows similar tetraheadral
  However each atom hooked to both types
- Binary crystal structure called Zink Blende (ZnS)
- Ternary Chalcopyrite
- Much more difficult to make
  binary/ternary compound crystals

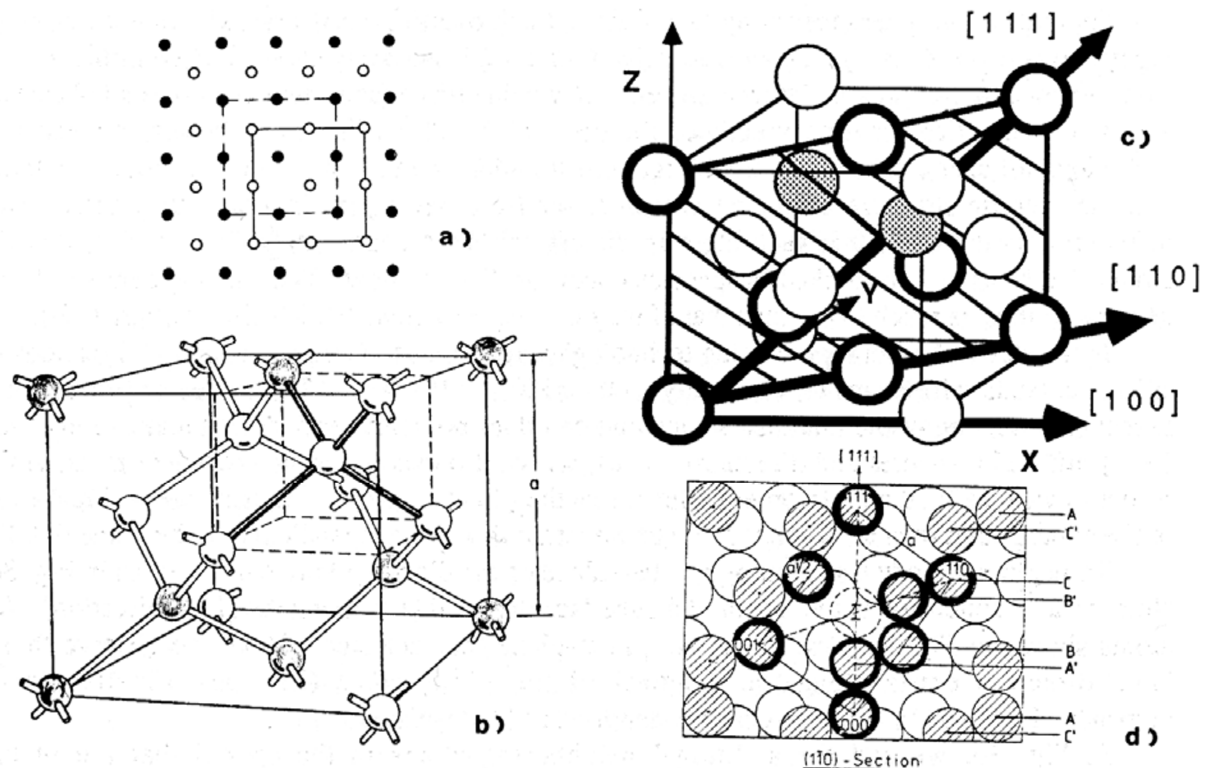


Fig. 3 (a) Top view (along any <100> direction) of an extended diamond lattice cell. The open circles indicate one fcc sublattice and the solid circles indicate the interpenetrating fcc. (b) Schematic representation of the diamond lattice unit cell. (c) A (110) section through the diamond lattice unit cell[8]. (d) (110) section showing atoms in the unit cell of (c) and neighboring atoms in the same $(1\bar{1}0)$ plane. Reprinted with permission of Springer-Verlag.

Miller Indexes and Crystal Planes

- Miller Indices are basic description of crystal plane
- Used to denote orientation of crystals

Miller Index

- Find intercept of plane on crystal axis
- Express intercepts as 3 integers
- Take r reciprocal of 3 integers
- Miller is smallest set of integers h, k, l
  having same ratio as reciprocals
- h for x axis, k for y, l for z
- eg if intercepts at 4, 3, 2
  then reciprocal are 1/4, 1/3, 1/2
  h = 3, k = 4, l = 6 (base of 12 in this case)
- For a plane show (h k l)
  if all similar planes in [h k l] then < h k l >
- Direction is [h k l]

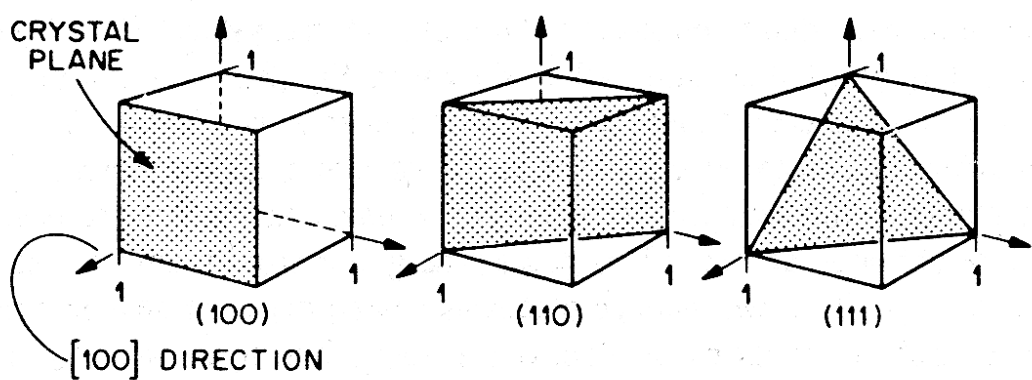
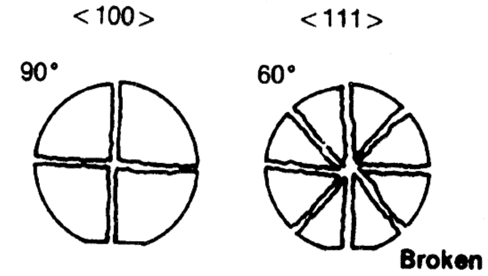


Fig. 2 Miller indices of some important planes in a cubic crystal.

Crystal Planes and Wafers

- Wafers (thin slices of silicon) has specific planes
- Planes are that of the wafer surface
- If taped at the centre then
- <100> breaks in 4 pieces with right angles
- <111> breaks in six 60° segments



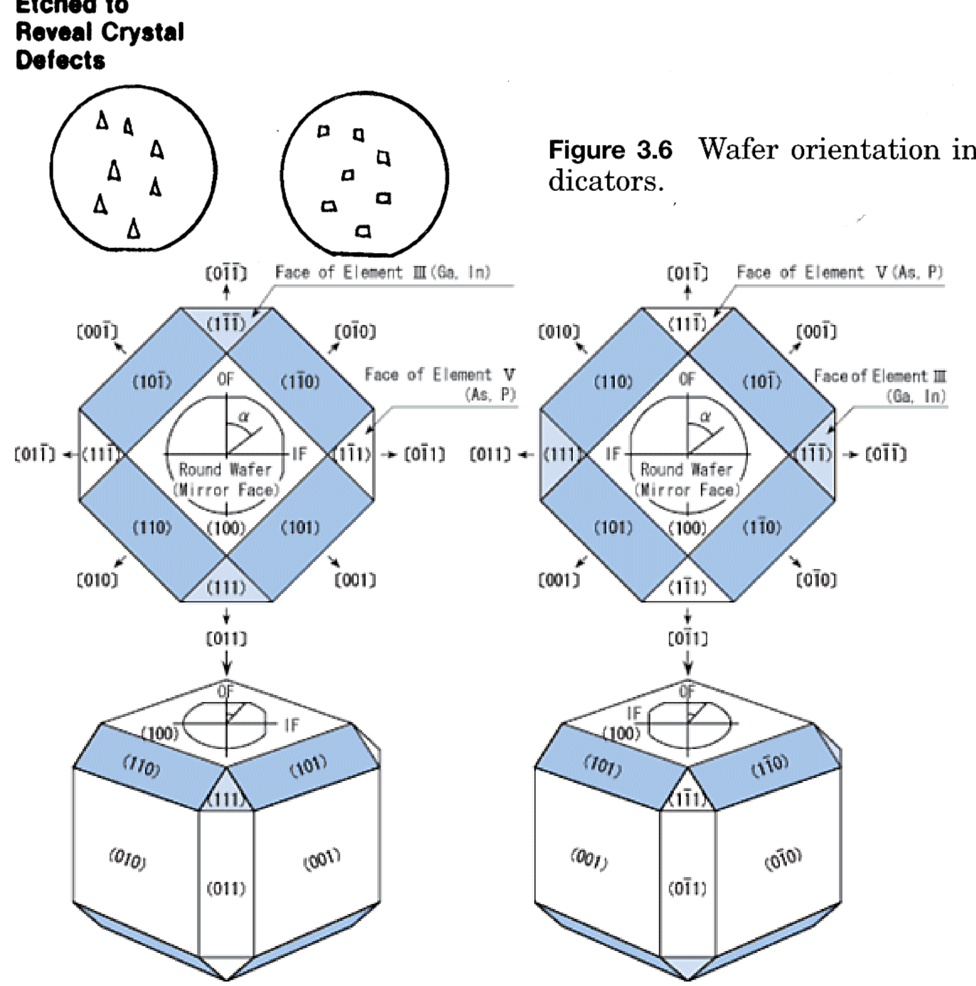
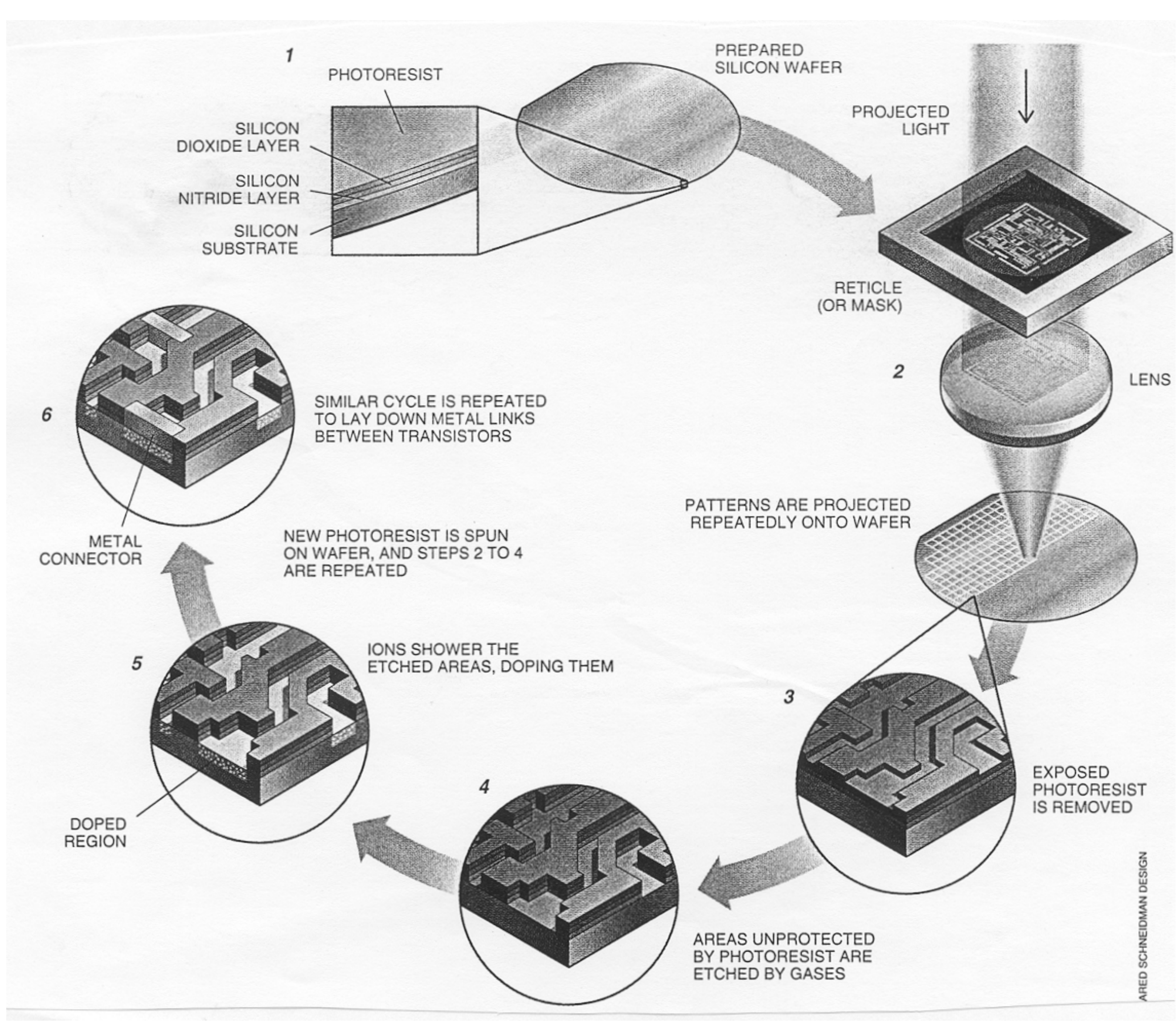


Figure 3.6 Wafer orientation indicators.

Basic Process Steps in Microfabrication

- Design of Circuit (by computers)
- Clean Wafer
- Deposit or grow layer of film
- "spin" on photosensitive material: photoresist
- Definition: Make pattern with Photolithography
- Develop photoimage (3D structure of resist).
- Etch away unwanted material
- Remove definition mask
- Sometimes other thermal or doping processes
- Repeat 7-20 times to defines layers as process requires



Single Layer Photolitographic Step

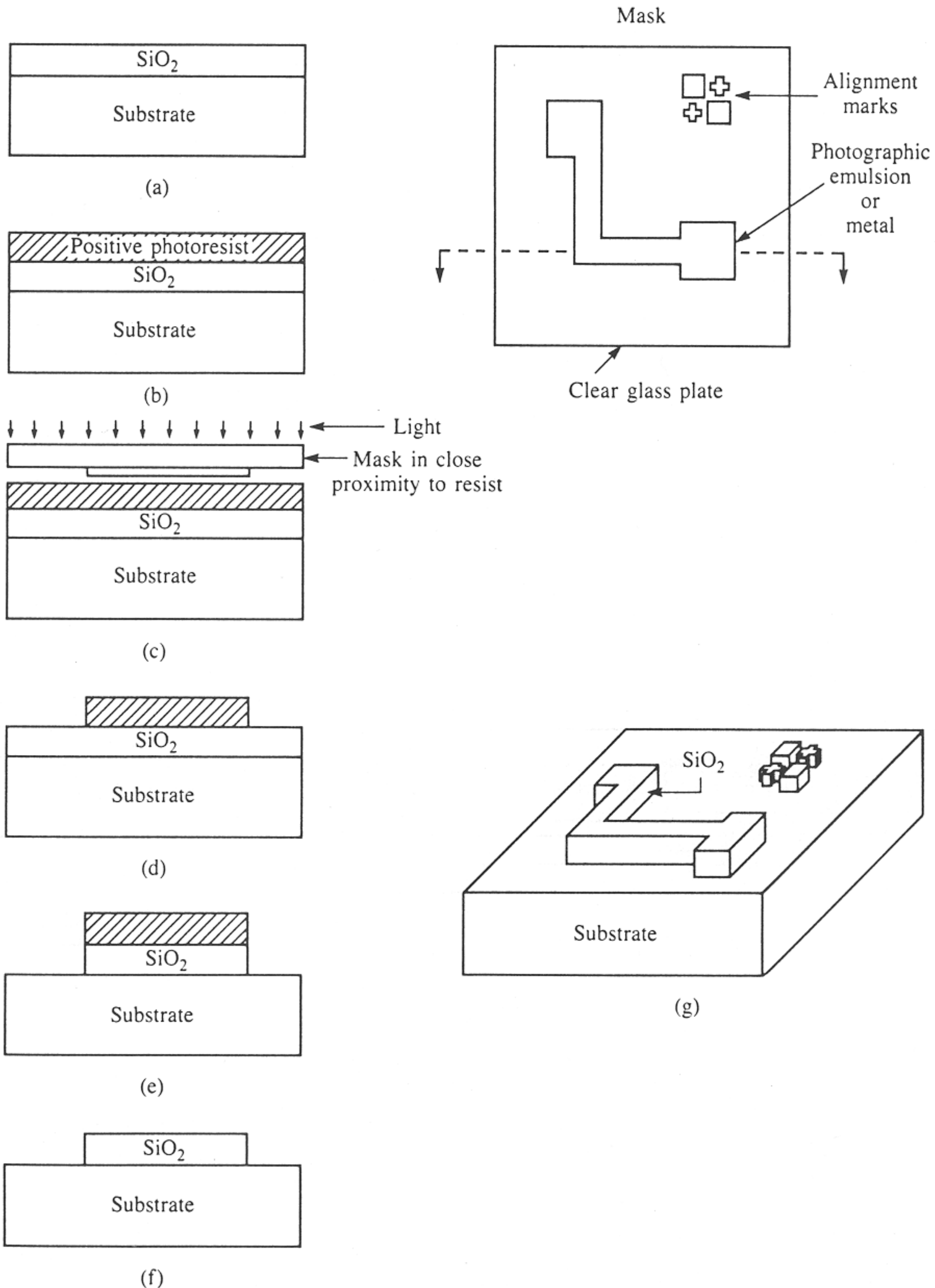


Fig. 2.2 Drawings of wafer through the various steps of the photolithographic process. (a) Substrate covered with silicon dioxide barrier layer; (b) positive photoresist applied to the surface of the wafer; (c) mask in close proximity to the surface of the resist-covered wafer; (d) substrate following resist exposure and development; (e) substrate following etching of the silicon dioxide layer; (f) oxide barrier on wafer surface after resist removal; (g) view of substrate with silicon dioxide pattern on the surface.

Simple MOS Process

Cross Section	Step	Operation	Name/Purpose
		Starting wafer	
	1	Layering	Field Oxide
	2	Patterning	Source/drain holes
	3	Doping Layering	N-type doping and reoxidation of source/drain
	4	Patterning	Gate region is formed
	5	Layering	Gate oxide is grown
	6	Patterning	Contact holes are patterned into source/drain regions
	7	Layering	Conducting metal layer is deposited
	8	Patterning	Metal layer is patterned
	9	Heat Treatment	Metal is alloyed to layer
	10	Layering	Protective passivation layer is deposited
	11	Patterning	Passivation layer is removed over metal pads

Figure 5.17 Formation of metal gate MOS transistor.

Step 8: Patterning. After deposition, the wafer goes back to the patterning area where portions of the metallization layer are removed from the chip area and the scribe lines. The remaining portions connect all the parts of the surface components to each other in the exact pattern required by the circuit design.

Contamination Control

- The most important aspect of microfabrication is control of dirt
- Processes killed by very small contaminants

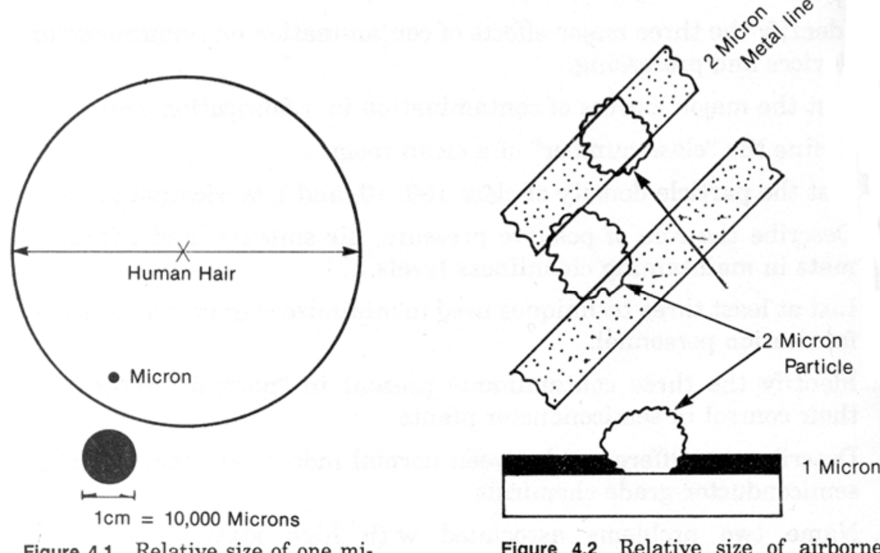


Figure 4.1 Relative size of one micron.

Figure 4.2 Relative size of airborne particulates to wafer dimensions.

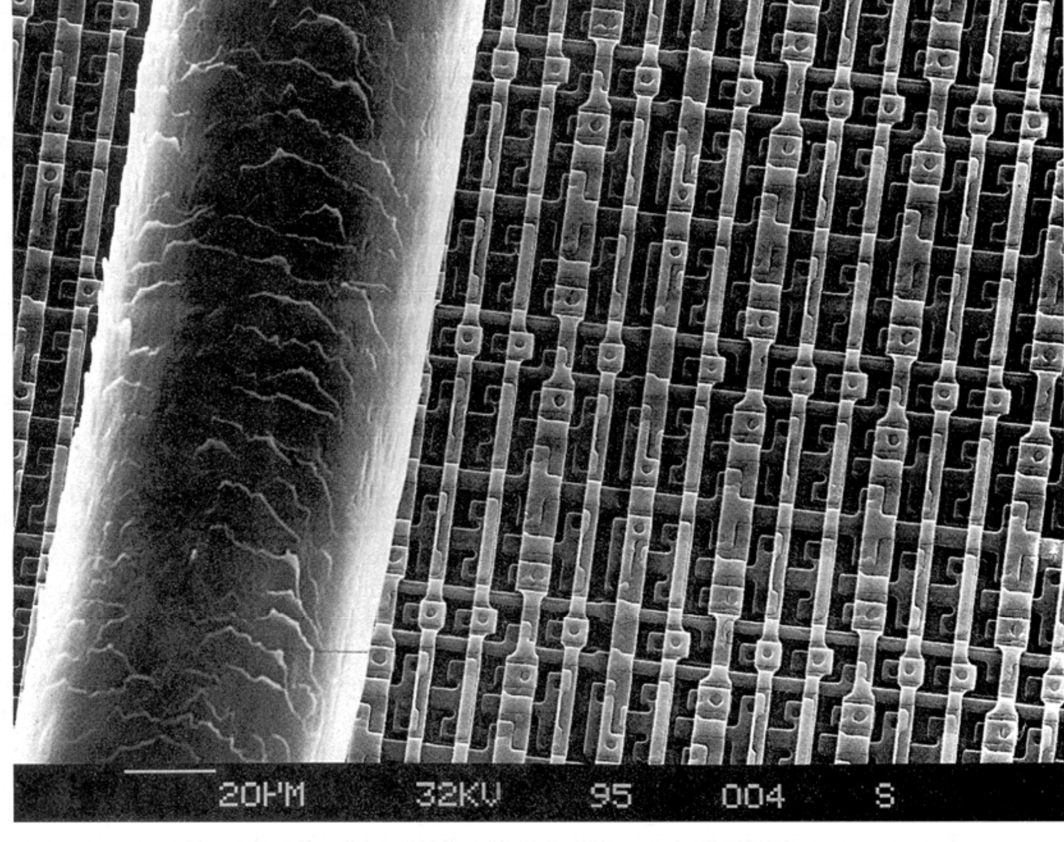


Figure 1.2 Scanning electron micrograph (SEM) of an IC circa mid-1980s. The visible lines correspond to metal wires connecting the transistors.

Particle Sizes in Air

FIGURE 2.1

PARTICLE SIZE DISTRIBUTION OF ATMOSPHERIC AIR

(at a concentration of 69 Micrograms per Cubic Meter
or .03 Grains per 1000 Cubic Feet)
For Typical Day

PARTICLE SIZE (MICRONS)	AVERAGE QUANTITY PER CUBIC FOOT	PERCENT BY COUNT	PERCENT BY WEIGHT
0.01 - 0.02	173,929,613	7.28%	-
0.02 - 0.05	338,577,845	14.17	0.02%
0.05 - 0.10	395,213,491	16.54	0.18
0.10 - 0.22	906,959,672	37.95	4.20
0.22 - 0.46	501,288,728	20.98	23.22
0.46 - 1.00	69,890,564	2.92	32.38
1.00 - 2.15	3,801,973	0.16	17.60
2.15 - 4.64	212,705	-	9.85
4.64 - 10.00	15,235	-	7.06
10.00 - 21.54	645	-	2.98
21.54 +	28	-	2.51
	2,389,890,499	100.00%	100.00%

Source: American Air Filter Research Laboratories

Human Activities and Contamination

PARTICLE EMISSION FROM HUMAN ACTIVITY
(without cleanroom gowning isolation)

Activity	Particles Emitted Per Minute Larger Than 0.3 Micron Diameter
Standing or Sitting - No Movement	100,000
Sitting - Light Head, Hand and Arm Movement	500,000
Sitting - Average Body and Arm Movement, Toe Tapping	1,000,000
Changing Position - Sitting to Standing	2,500,000
Slow Walking - 2.0 MPH	5,000,000
Average Walking - 3.57 MPH	7,500,000
Fast Walking - 5.0 MPH	10,000,000
Calisthenics	15,000,000 to 30,000,000

Chapter 7-127, OPERATING IN AND MAINTENANCE OF CLEANROOMS; 1990

Clean Room Class Numbers

- Class = number of 0.5 micron particles/cu. ft.
- Modest clean room Class 1000
- State of art Class 1

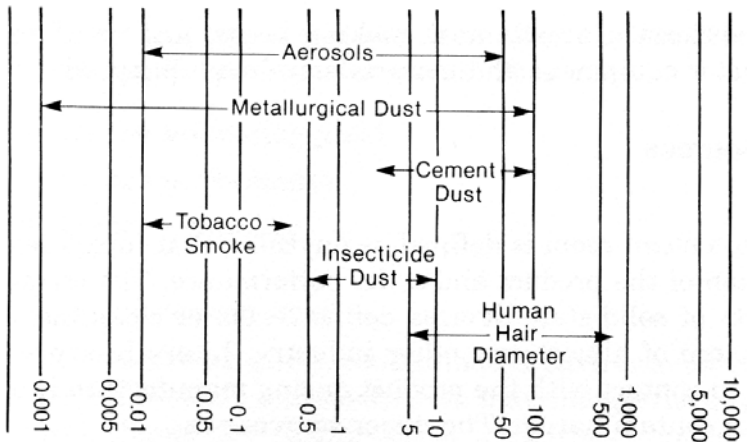


Figure 4.4 Relative size of airborne particulates (microns).

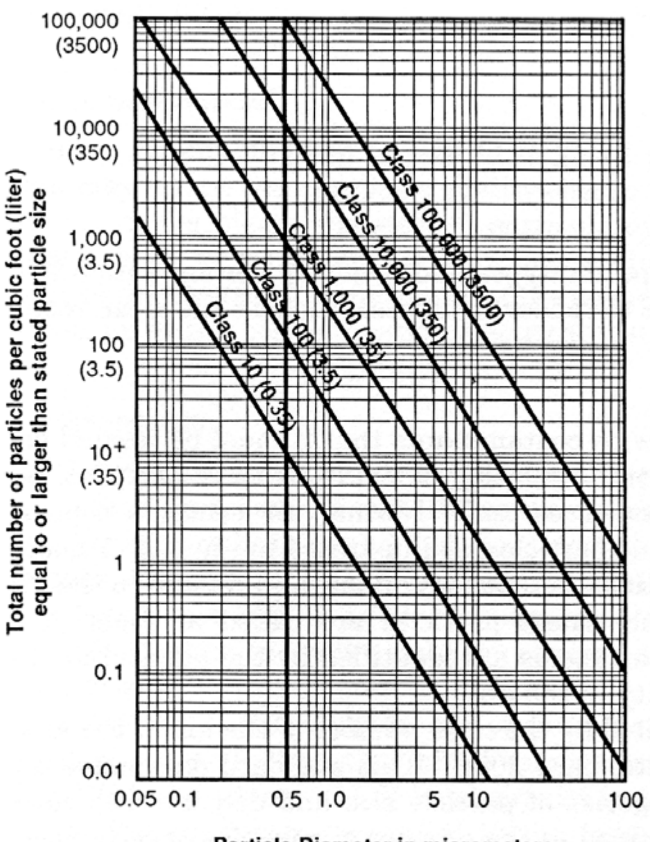
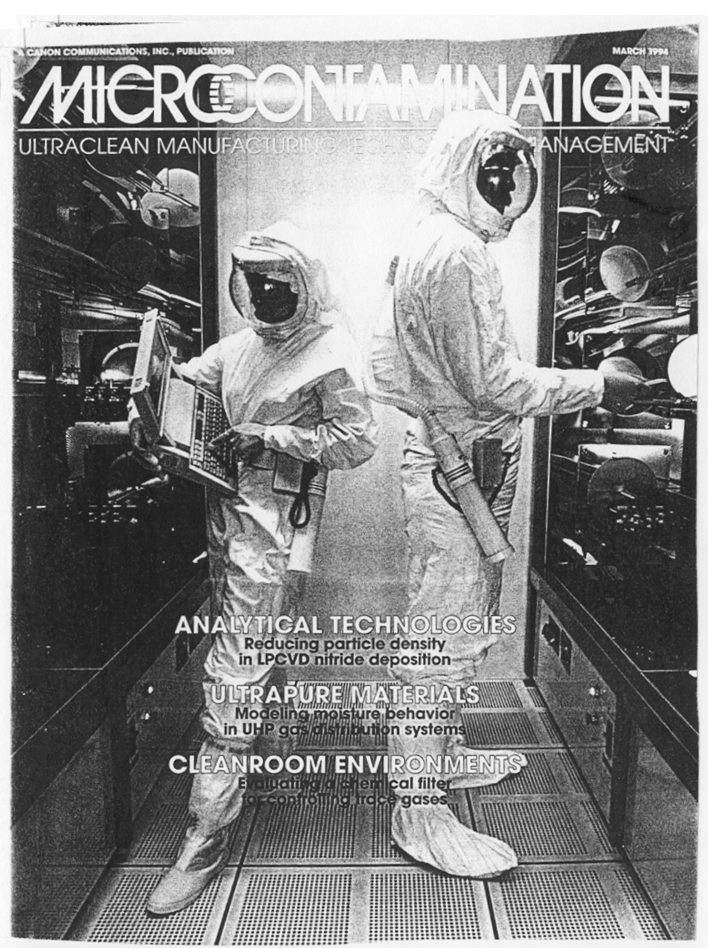


Figure 4.5 Particle size, density, and class number relationship.

Clean Room Garments

- For class 1000 cover most of body
- Class 100 - 10 must cover much of face
- Class 10 - 1 full face masks and breather filters

Figure 4.14 Worker in clean-room garments.



Basic Clean Room Layout

- Clean air from HEPA filters
- HEPA High Efficiency Particle Attenuators
- Call Laminar flow: means air does not have turbulence
- Air blows down from roof, and comes out bottom

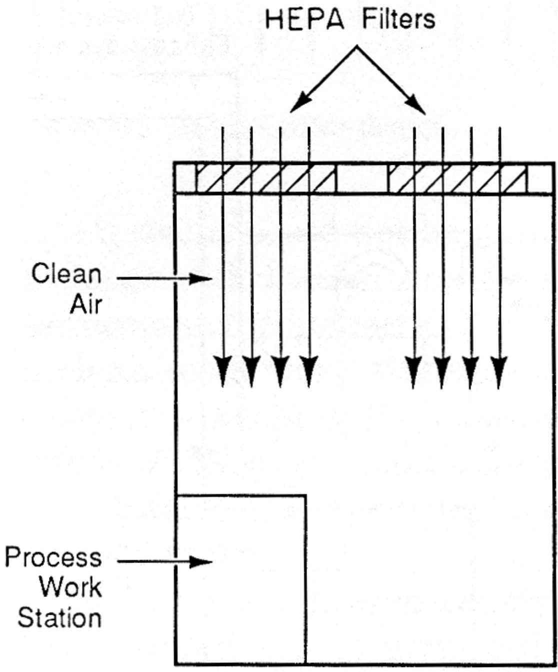


Figure 4.10 Cross section of clean-room tunnel.

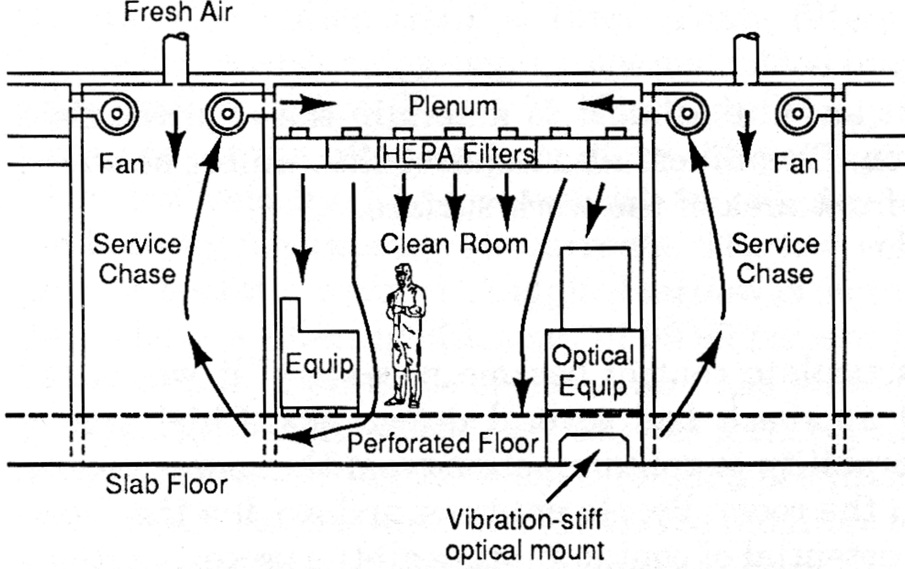
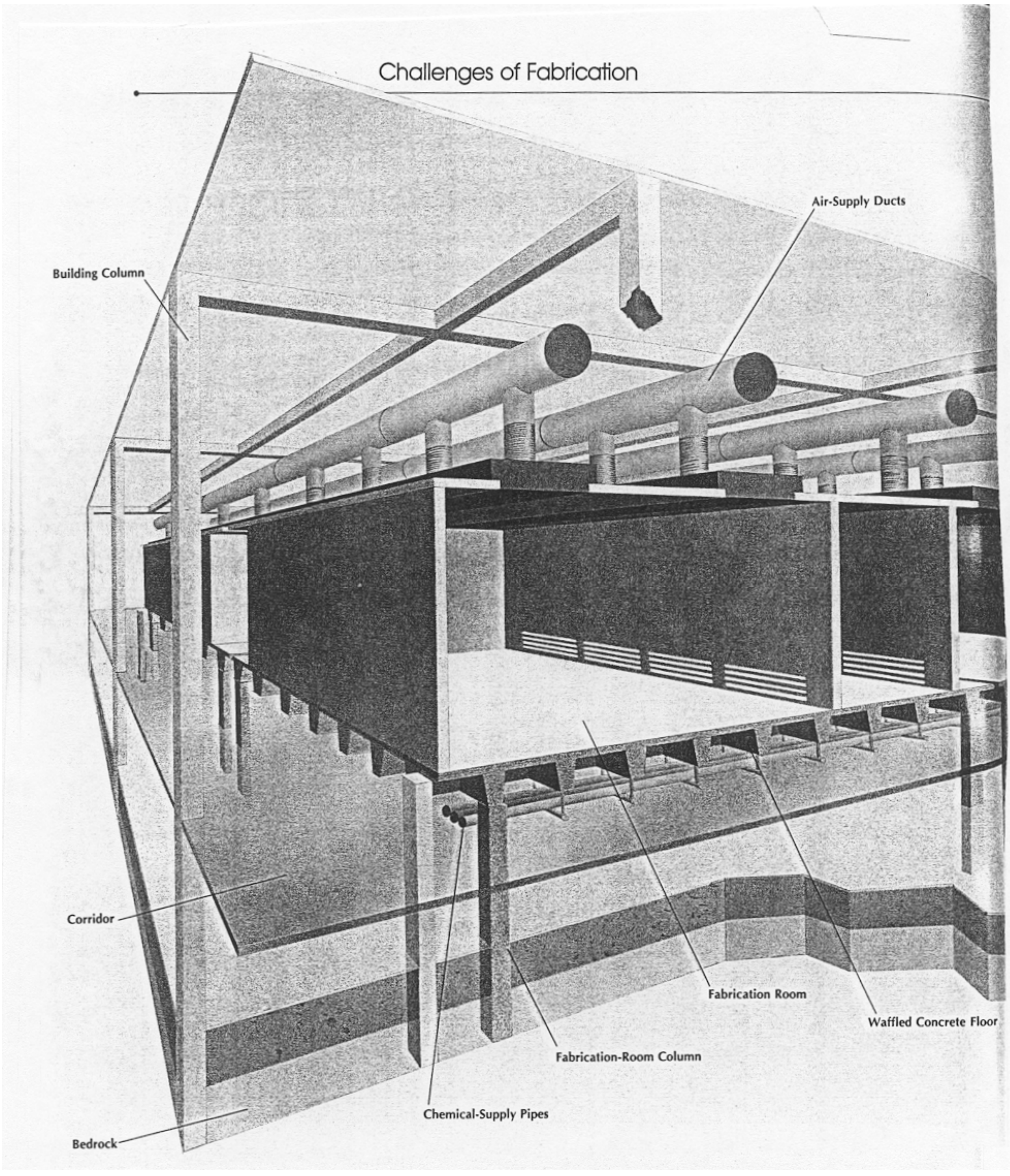


Figure 4.11 Cross section of laminar flow clean room. *(Courtesy of Semiconductor International.)*

Clean Room Building

- Clean room suspended within the building
- Vibration isolated from outside



HEPA Filters: High Efficiency Particle Attenuators

- HEPA filters very simple in concept:
  just folded aluminum foil and paper
- Air forced by foil to flow though many layers of filter
- As particles absorbed filter gets better but air pressure drop rises

Energy required to push the air through the HEPA filter area is

$$E = v_a P \qquad W/m^2$$

v_a = air velocity (m/s), P = pressure drop (Pa)

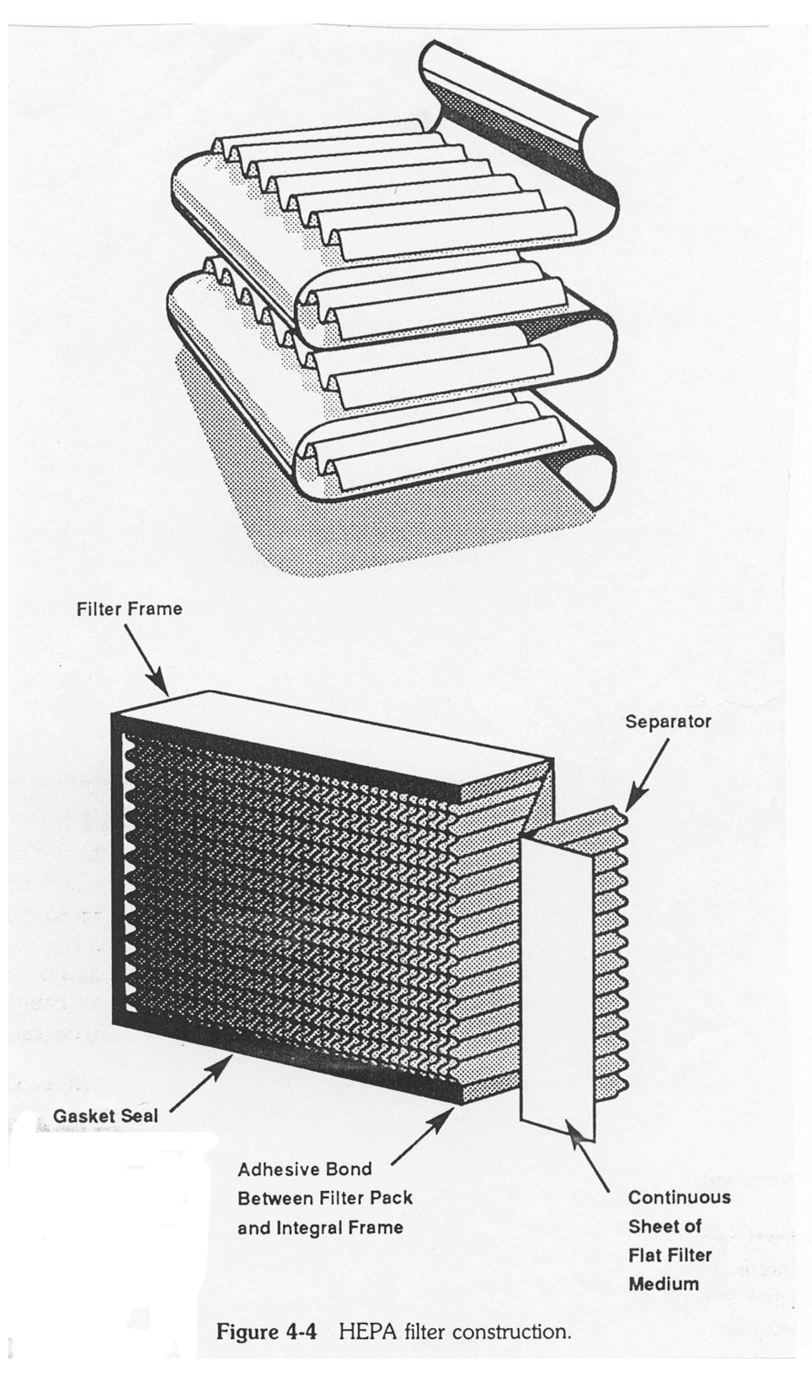


Figure 4-4 HEPA filter construction.

Deionized Water

- Water contamination as important as air
- Use Deionized (DI) water systems
- Removes heavy elements and biologicals

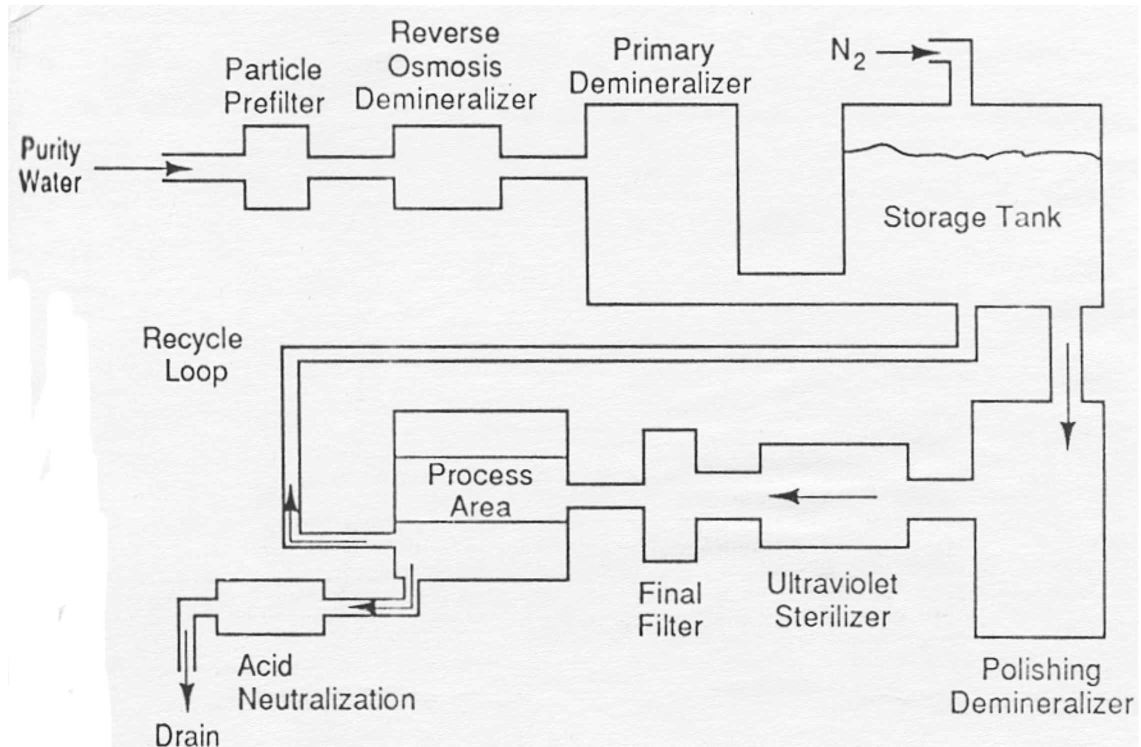


Figure 4.15 Typical deionized water system.

Resistivity Ohms-cm 25°C	Dissolved Solids (ppm)
18,000,000	0.0277
15,000,000	0.0333
10,000,000	0.0500
1,000,000	0.500
100,000	5.00
10,000	50.00

Figure 4.16 Resistivity of water versus concentration of dissolved solids.

Specifications for Clean Room Utilities

- Air, Water, Chemicals, Gases are common utilities
- All must meet specifications listed

SOURCE		SPECIFICATION
Air		
Particulates	LSI	Class 100 @ 0.5 micron
	VLSI	Class 10 @ 0.3 micron
Humidity		15-50%
Temperature		68-74°F
Photochemical Smog		2 pphm (parts per hundred million)
Deionized Water		
Resistivity		15-18 meg Ω cm
Particulate		Less than 100 particulates per centiliter after 0.5 micron filtration
Bacteria		Less than 100 colonies per ml sample after 0.5 micron filtration
Chemicals		
Metallic Impurities		Less than 1 ppm
Filtration		To 0.2 micron
Gases		
Purity		Greater than 99.9%
Water Vapor		Less than 5 ppm
Filtration		To 0.3 micron
Static Charge		Less than 50 volts

Figure 4.17 Summary of clean-room requirements.

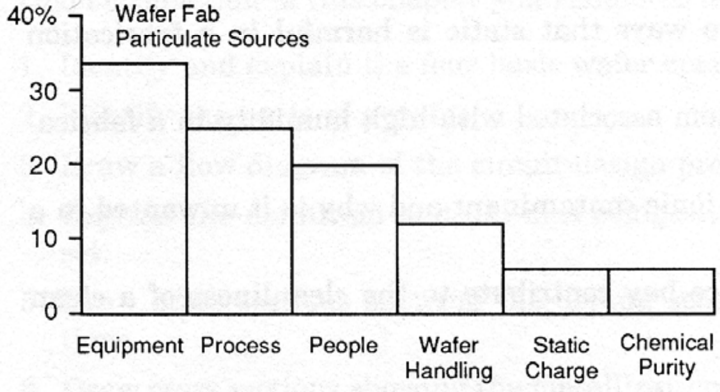


Figure 4.18 Sources of particulate contamination. This analysis, shown at SEMI Forecast by Dr. C. Rinn Cleavelin, Texas Instruments, revealed equipment-generated particles as the top enemy in 1985. *(Courtesy of Semiconductor Equipment and Materials Institute.)*