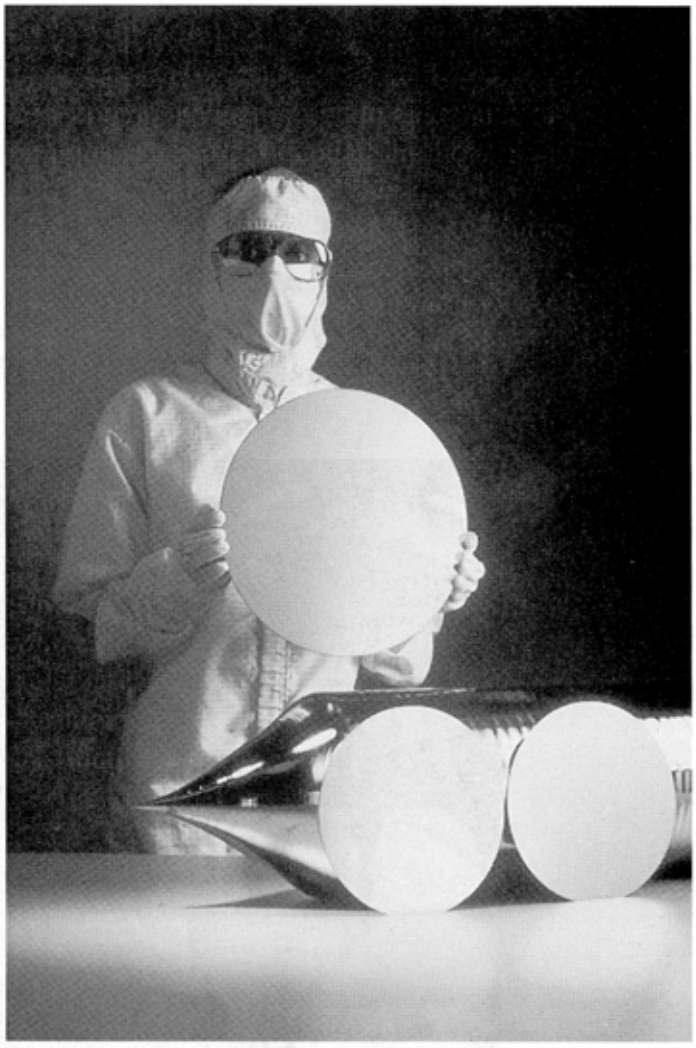
Silicon Wafers: Basic unit

- Silicon Wafers Basic processing unit
- 150, 200, 300 mm disk, 0.5 mm thick
- Newest ones 300 mm (12 inches)
- Typical process 25 - 1000 wafers/run
- Each wafer: 100 - 1000's of microchips (die)

- Wafer cost $10 - $100's
- 200 mm wafer weight 0.040 Kg
- Typical processing costs $1200/wafer (200 mm)
- Typical processed wafer value $11,000
  (all products, modest yield)
- Value/Mass of processed wafer $275,000/Kg



Production of Silicon Wafers

- Silicon starts as beach sand quartzite

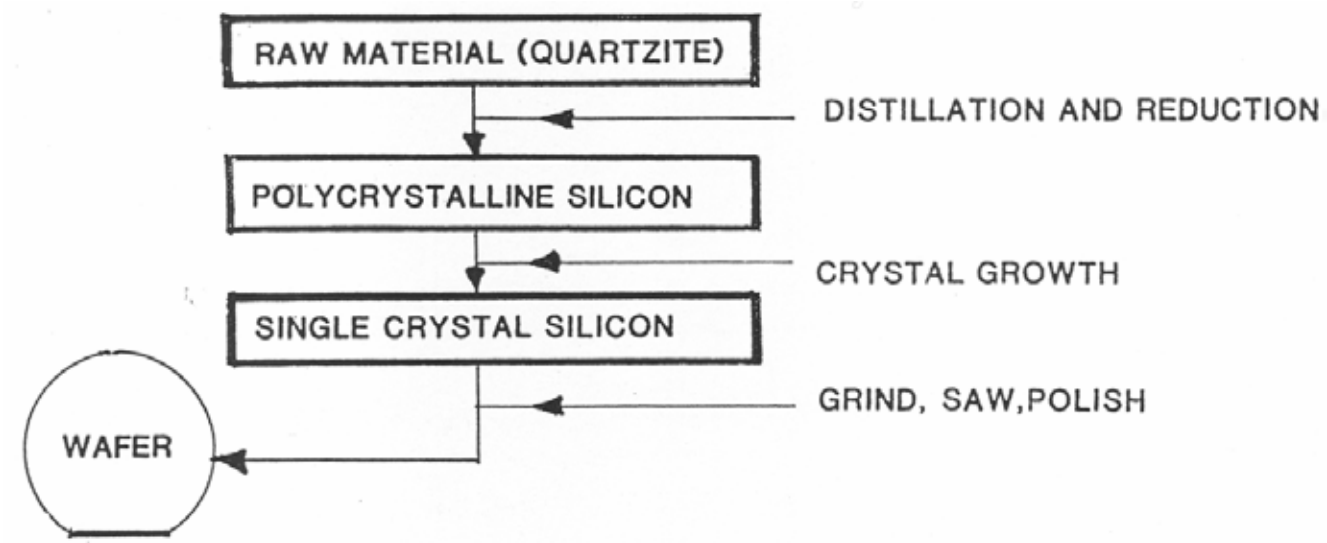


Fig. 4 Process sequence from starting material to polished wafer.

Conversion of Raw Sand into Metallurgical Grade Silicon

Step 1: Metallurgical Grade Silicon (MSG): 98% pure

- Start with white beach sand (quartzite or SiO_2)
- Use electric arc to melt in mixture of coal coke, wood at 2000°C
- Carbon removes impurities: molten Si drawn from bottom

$$SiO_2 + 2C \rightarrow Si + 2CO$$

- Takes considerable power: 12-14 KWh/Kg of Si

Step 2: Metallurgical Grade Silicon Chemical Purification

- Convert MSG powder to trichlorosilane ($SiHCl_3$) by reacting with anhydrous hydrogen chloride at 300°C
- Chlorine reacts with impurities to give $AlCl_3$,
- Trichlorosilane ($SiHCl_3$) boils at 31.8°C

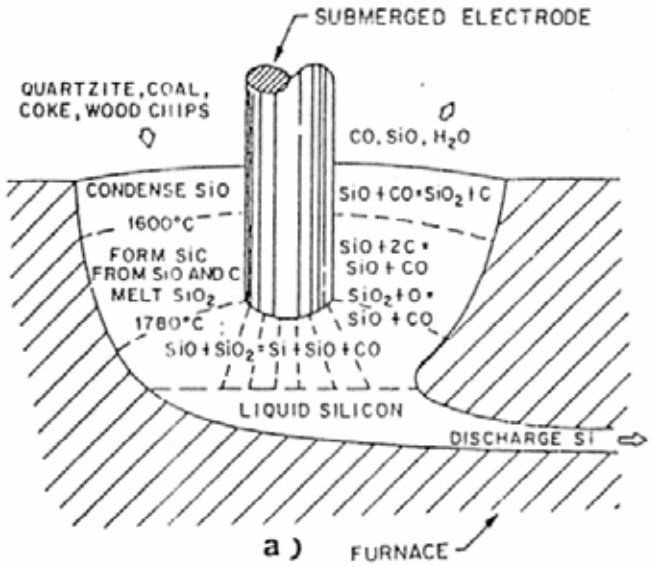


Fig. 5 (a) Schematic of submerged-electrode arc furnace for production of MGS[5].

Metallurgical Grade Silicon into Polycrystalline Silicon

Step 3: Distill Trichlorosilane

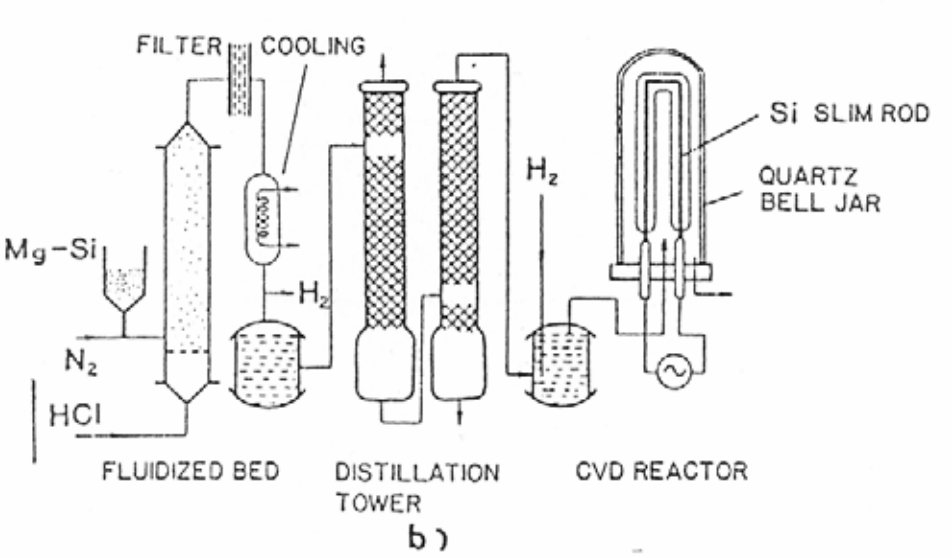
- Impurities reduce to parts per billion atoms (ppba) or $10^{13}/cm^3$
- Reduced by 10^8 from original values

Step 4: Silicon Chemical Vapour Deposition

- Gaseous trichlorosilane ($SiHCl_3$) reacted with Hydrogen

$$SiHCl_3 + 2H_2 \rightarrow 2Si + 6HCl$$

- Si deposits out on rods with large crystals: Polycyrstalline
- Result Electronic Grade Silicon (EGS)
- Called the Siemens process
- Total production 3 million Kg 1985



(b) Schematic of fluidized bed, distillation tower, and CVD reactor developed by Siemens[9]

Czochralski Crystal Growth methods

- Czochralski (CZ) basic Silicon crystal growth method
- Melt Poly Si EGS at 1430^{o}C in quartz crucible
- Rotate crucible
- Bring counter rotating seed crystal to melt
- Slowly draw seed from melt
- Atoms of melt freeze out aligned with crystal planes of seed

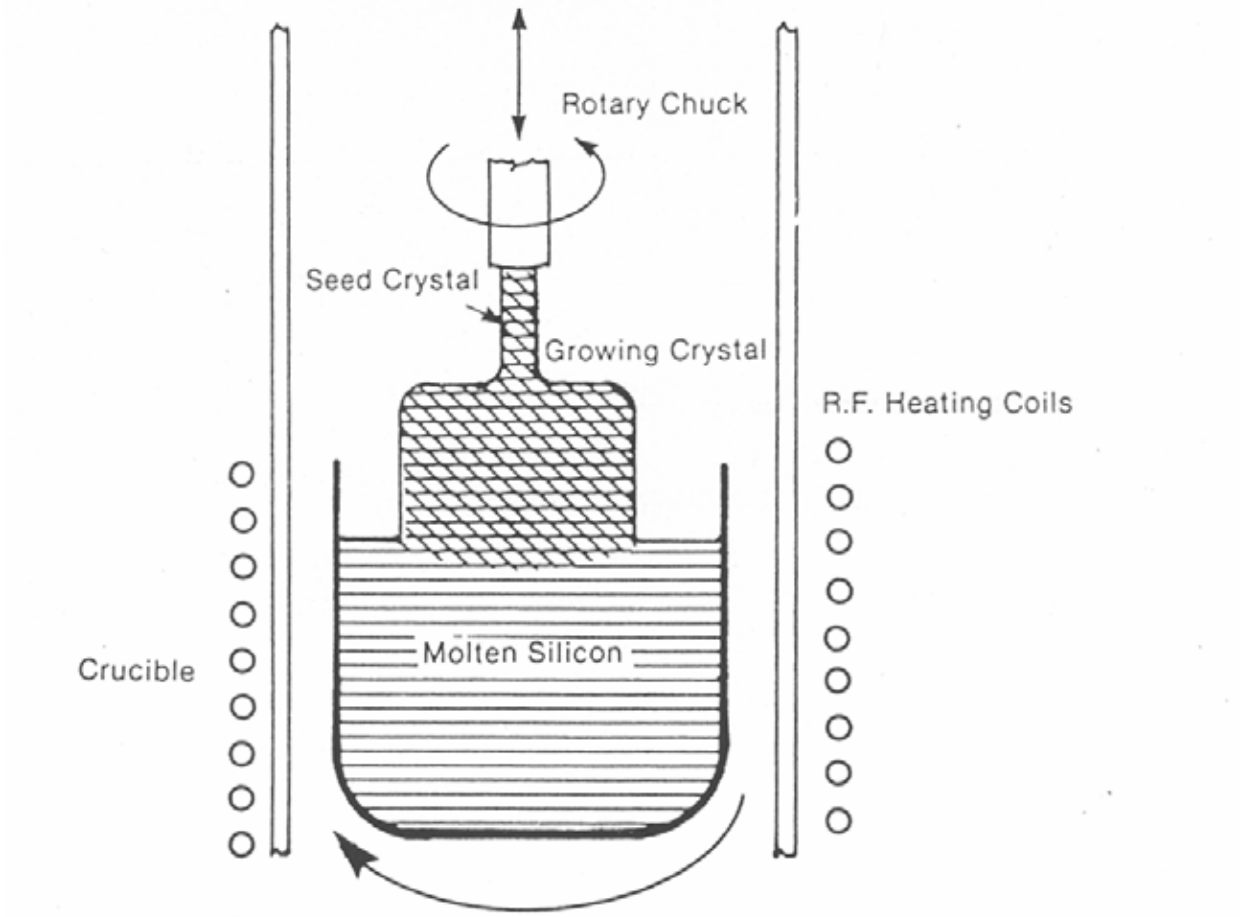


Figure 3.7 Czochralski crystal-growing system.

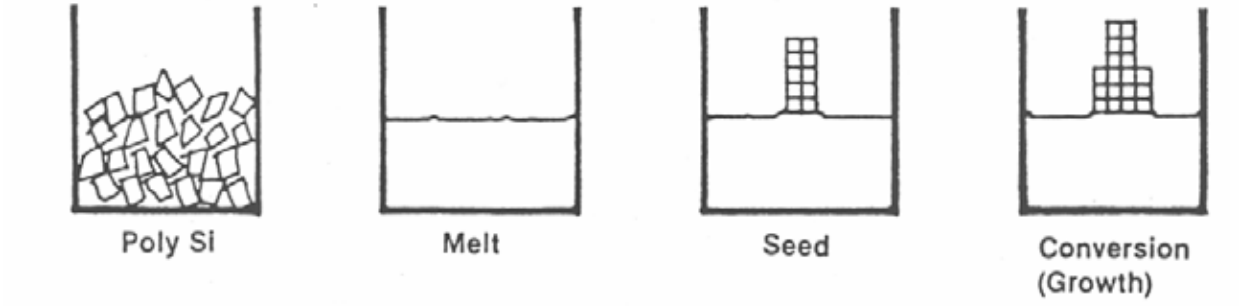


Figure 3.8 Crystal growth from a seed.

Czochralski Crystal Growth

- As seed drawn from melt initially grow narrow neck
- Dislocations (incorrect crystal alignment stopped at neck)
- As slow rate of pull (withdrawal) crystal diameter grows to max
- Maintain constant rotate/pull rate for uniformity eg 20 cm/hr

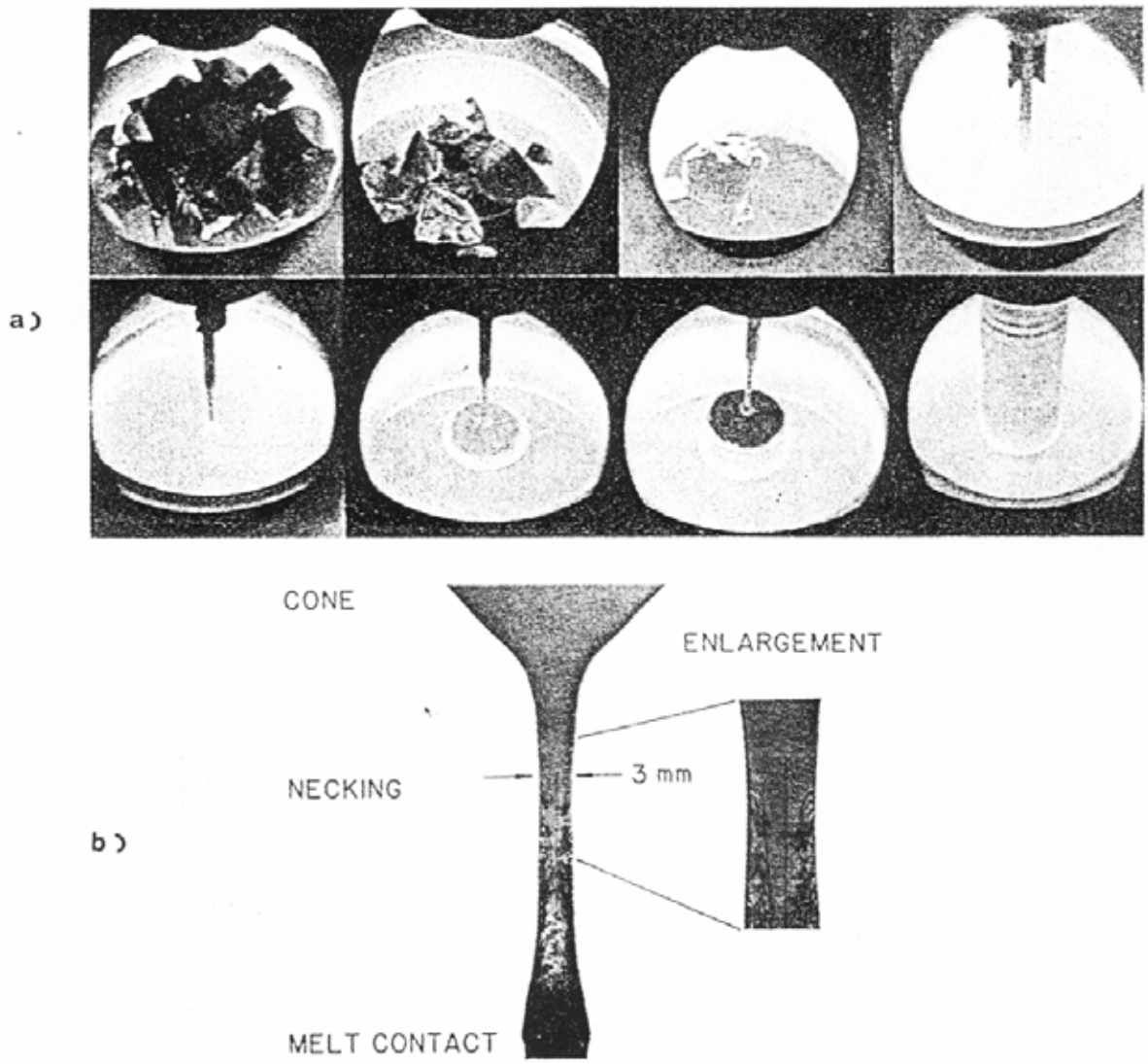


Fig. 8 (a) Illustration of several process steps during CZ crystal growth. Courtesy of Dynamit-Noble-Grace. (b) X-ray topograph of seed necking and conical part of crystal. Dislocations generated at the end of the seed crystal that contacted the molten zone grow out to the side surface of the neck and do not propagate into the main crystal[9]. Reprinted with permission of Academic Press.

Finished Czochralski Crystals

- Crystals up to 200, 300 and 400 mm now possible
- Most recent advance: Magnetic Convection suppression
- Magnetic field induces force to prevent moving Si conductor

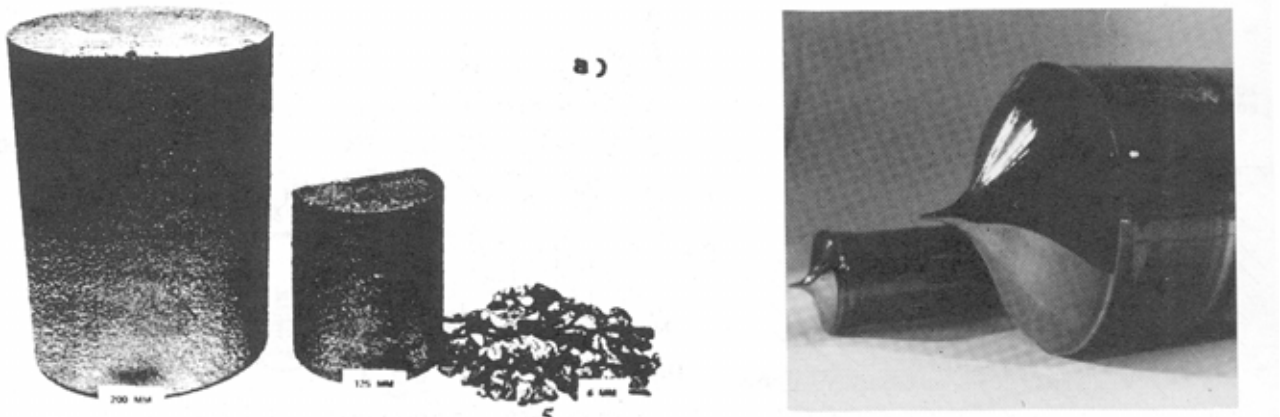


Fig. 6 (a) EGS in polysilicon form[5]. Reprinted with permission of the publisher, the Electrochemical Society. (b) 150 mm single-crystal CZ silicon ingot. Reprinted with permission of the Monsanto Eletronics Materials Company.

Movement of Impurities from Melt to Crystal

- To put dopants in wafer place impurity in melt
- Equilibrium concentration (solubility) different in solid, N_s than in liquid N_l (note solubilities often symbolized as C_s, C_l)
- Segregation ratio fraction of liquid dopant in solid

$$k = \frac{N_s}{N_l}$$

- Thus as crystal pulled melt dopant concentration changes with X, fraction of melt consumed (starting with 0)

$$N_s = kN_{l0}(1 - X)^{[k-1]}$$

- Thus dopant concentration changes along length of crystal
- Thus impurities & dopants differ in each wafer

Table 1-1 Segregation coefficients for common impurities in silicon

Impurity		Segregation coefficient k†
Aluminum	(Al)	0.002
Antimony	(Sb)	0.3
Arsenic	(As)	0.3
Boron	(B)	0.72–0.8
Carbon	(C)	0.07
Copper	(Cu)	4×10^{-4}
Gallium	(Ga)	0.007–0.008
Gold	(Au)	2.2×10^{-5}
Indium	(In)	4×10^{-4}
Iron	(Fe)	8×10^{-6}
Oxygen	(O)	1.25
Phosphorus	(P)	0.35

†Where multiple values are given, literature values vary.

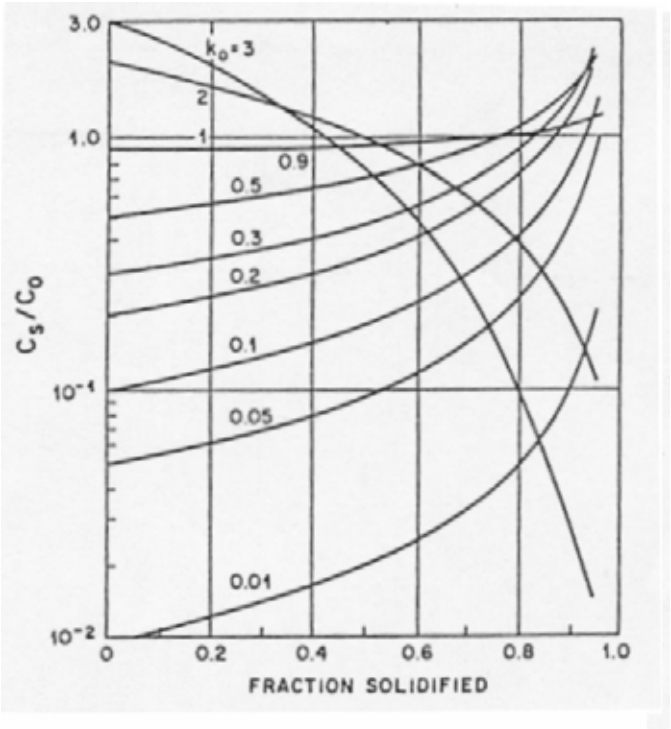


Fig. 10 Curves fron growth from the melt, showing the doping concentration in a solid as a function of ther fraction solidified. From W.G. Pfann, *Zone Melting*, 2nd Ed. 1966. Copyright © John Wiley and Sons. Reprinted with permission of John Wiley and Sons.

Float Zone Crystallization

- Float Zone (FZ) produces smaller wafers
- Start with polycrystalline Si rod
- Touch rod to seed crystal
- Heat with moving Radio Frequency (RF) coil
- Melts road near coil
- Move melt front from crystal to end and back
- Leaves single crystal rod behind

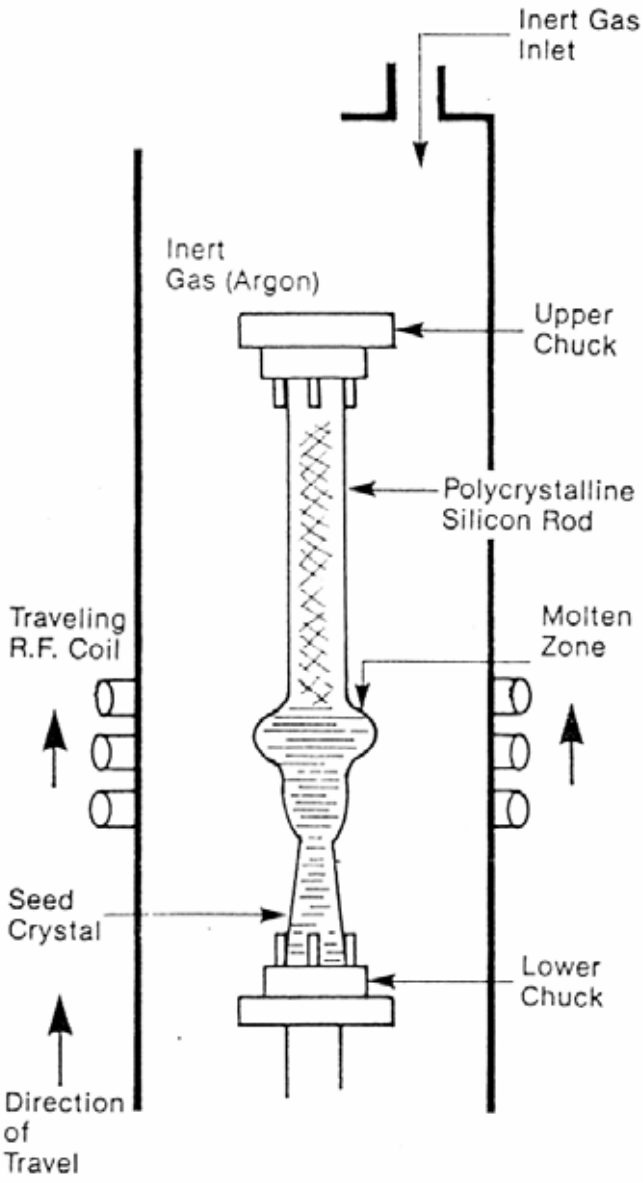


Figure 3.10 Float-zone crystal-growing system.

Comparison of CZ and FZ wafers

- FZ better impurity, but smaller size

PARAMETER	CZ	FLOAT ZONE
Large Crystal	Yes	Difficult
Cost	Lower	
Dislocations	0 - 10^4/cm^2	10^3 - 10^5/cm^2
Resistivity	Up to 100 ohm-cm	2000 ohm-cm Max.
Radial Resistivity	5 - 10%	5 - 10%
Oxygen Content	10^{16} - 10^{18} atoms/cm^3	0 - Very Low

Figure 3.11 Comparison of CZ and float crystal-growing methods.

TABLE 2.4 Comparison of Silicon Material Characteristics and Requirements for ULSI

Property	Characteristics		Requirements for ULSI
	Czochralski	Float Zone	
Resistivity (phosphorus) *n*-type (ohm-cm)	1–50	1–300 and up	5–50 and up
Resistivity (antimony) *n*-type (ohm-cm)	0.005–10	—	0.001–0.02
Resistivity (boron) *p*-type (ohm-cm)	0.005–50	1–300	5–50 and up
Resistivity gradient (four-point probe) (%)	5–10	20	< 1
Minority carrier lifetime (μs)	30–300	50–500	300–1000
Oxygen (ppma)	5–25	Not detected	Uniform and controlled
Carbon (ppma)	1–5	0.1–1	< 0.1
Dislocation (before processing) (per cm^2)	≤ 500	≤ 500	≤ 1
Diameter (mm)	Up to 200	Up to 100	Up to 300
Slice bow (μm)	≤ 25	≤ 25	< 5
Slice taper (μm)	≤ 15	≤ 15	< 5
Surface flatness (μm)	≤ 5	≤ 5	< 1
Heavy-metal impurities (ppba)	≤ 1	≤ 0.01	< 0.001

ppma, parts per million atoms; ppba, parts per billion atoms.

Current common Si Wafer Sizes

- 300 mm (12 inch) now in most state of art fabs (2001)
- 200 mm (8 inch) common fabrication (started 1995)
- 150 mm (6 inch) most 2nd level to front line fabs
- 125 mm (5 inch) Bastard size (only a few facilities)
- 100 mm (4 inch) Smallest production wafers: research
- 75 mm (3 inch) Obsolete size: still used in research
  (special order: more expensive than 4 inch)
- 400 mm (16 inch) experimental production
- Basically need to rebuild entire fab to change wafer size

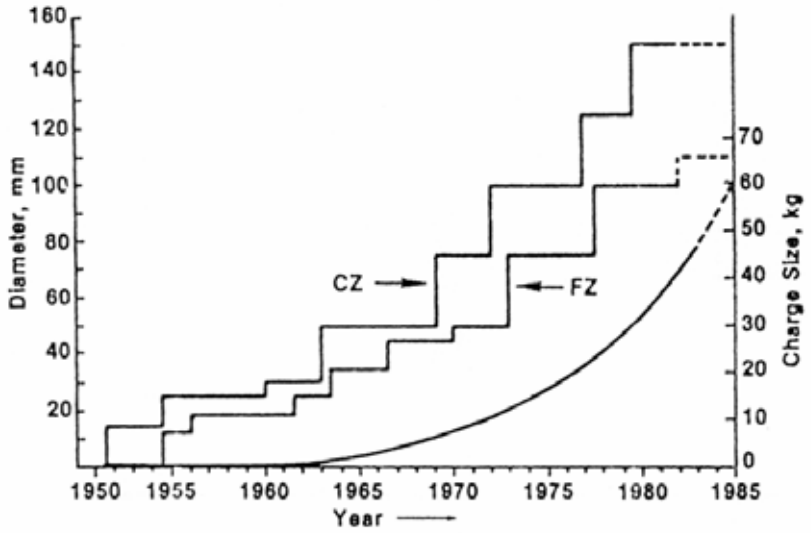


Fig. 7 The increase with time of CZ silicon crystal diameter and charge sizes[47]. Reprinted with permission of Semiconductor International.

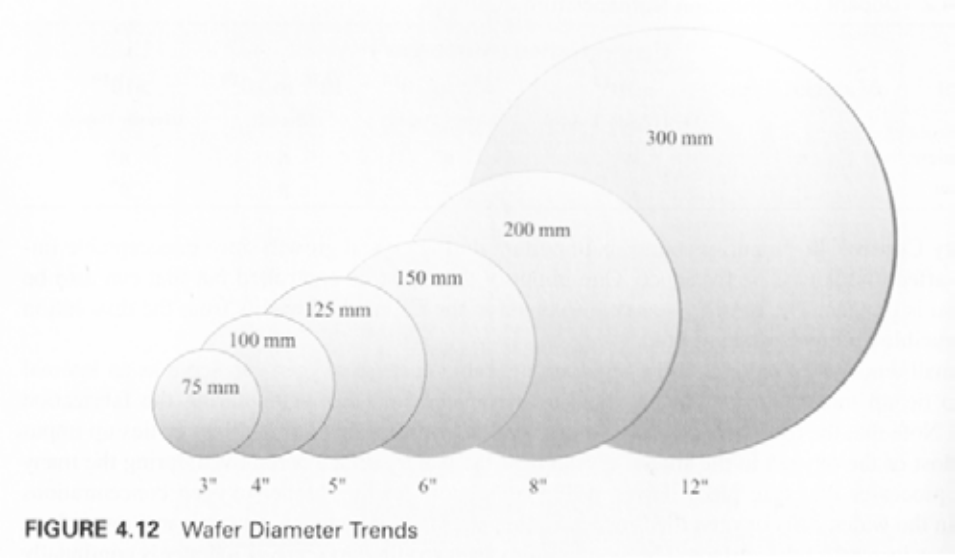


FIGURE 4.12 Wafer Diameter Trends

Rod (Bole) Sawing

- Use diamond saws to cut Crystal rods
- Very thin blades
- Resulting slices called wafers
- Typical wafer about 0.5-0.6 mm thick
- Lose nearly half material in cutting

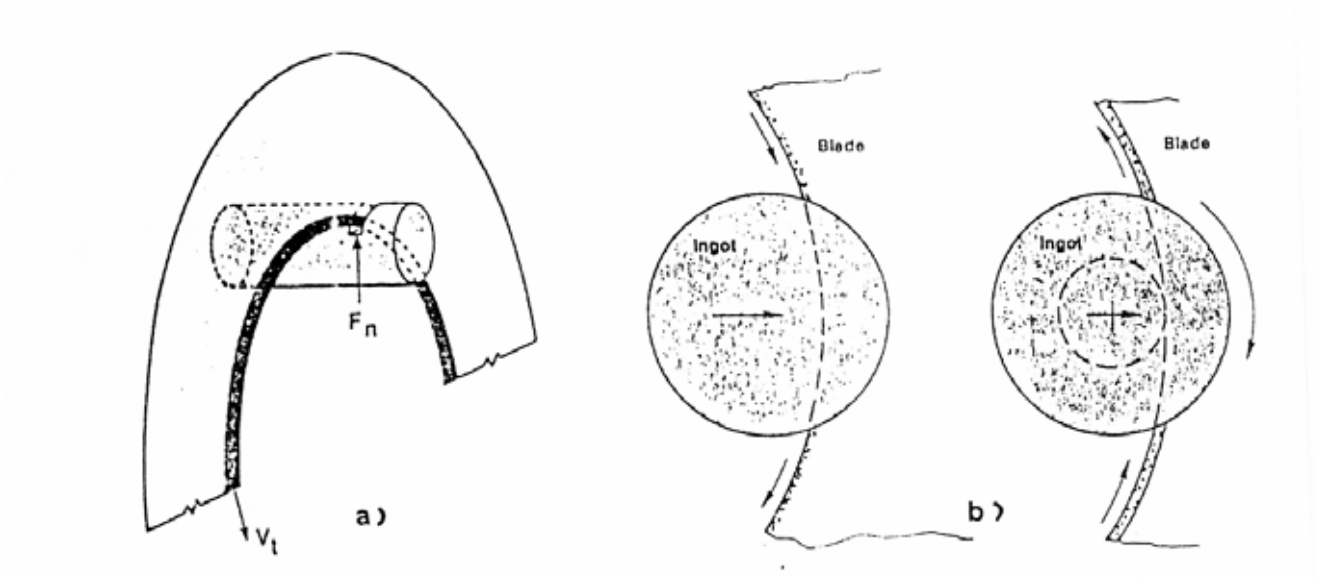


Fig. 19 (a) ID saw geometry[27]. (b) ID slicing[28]. Reprinted with permission of Solid Sta Technology, published by Technical Publishing, a company of Dun & Bradstreet.

Table 4.2 Wafer thickness for different wafer sizes

Wafer Size (mm)	Thickness (μm)	Area (cm^2)	Weight (grams)
50.8 (2")	279	20.26	1.32
76.2 (3")	381	45.61	4.05
100	525	78.65	9.67
125	625	112.72	17.87
150	675	176.72	27.82
200	725	314.16	52.98
300	775	706.21	127.62

Wafers Polishing

- Wafers mechanically abrasive polished to reduce roughness
- Then chemical/mechanical polished
- Film thickness are 0.1 microns or smaller for devices
- Thus wafers polished to < 10 nm defects

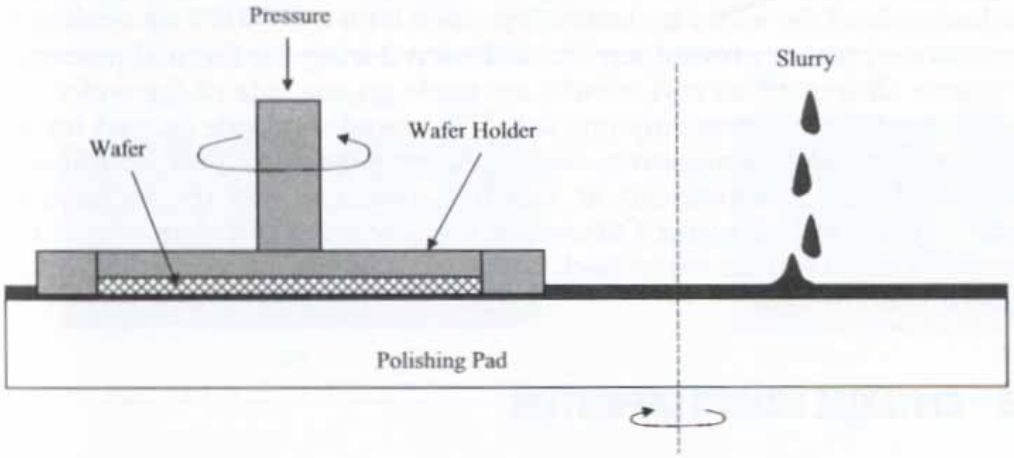


Figure 4.17
Schematic of CMP process.

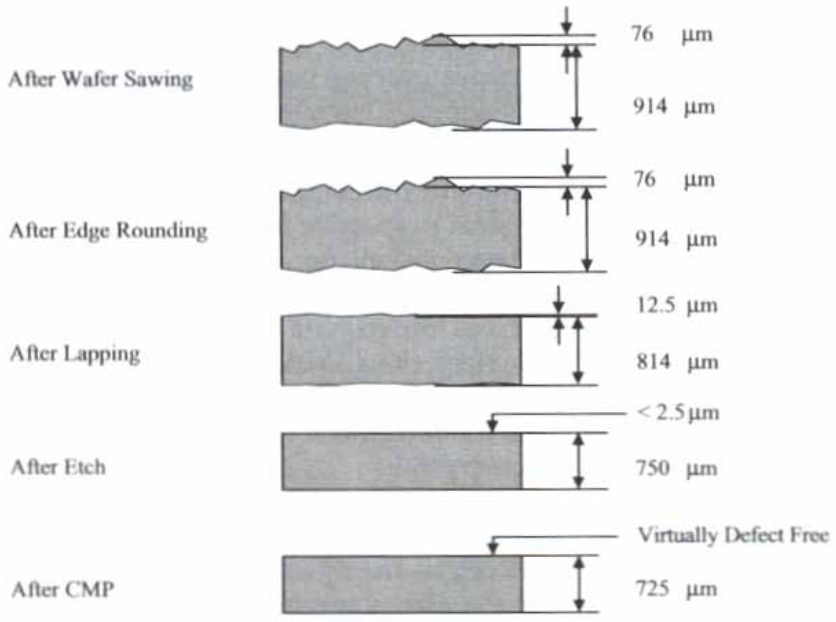


Figure 4.18
Wafer thickness and surface roughness changes.

Wafer Flatness

- Very important for holding wafers down
- Also for focusing of photolithography

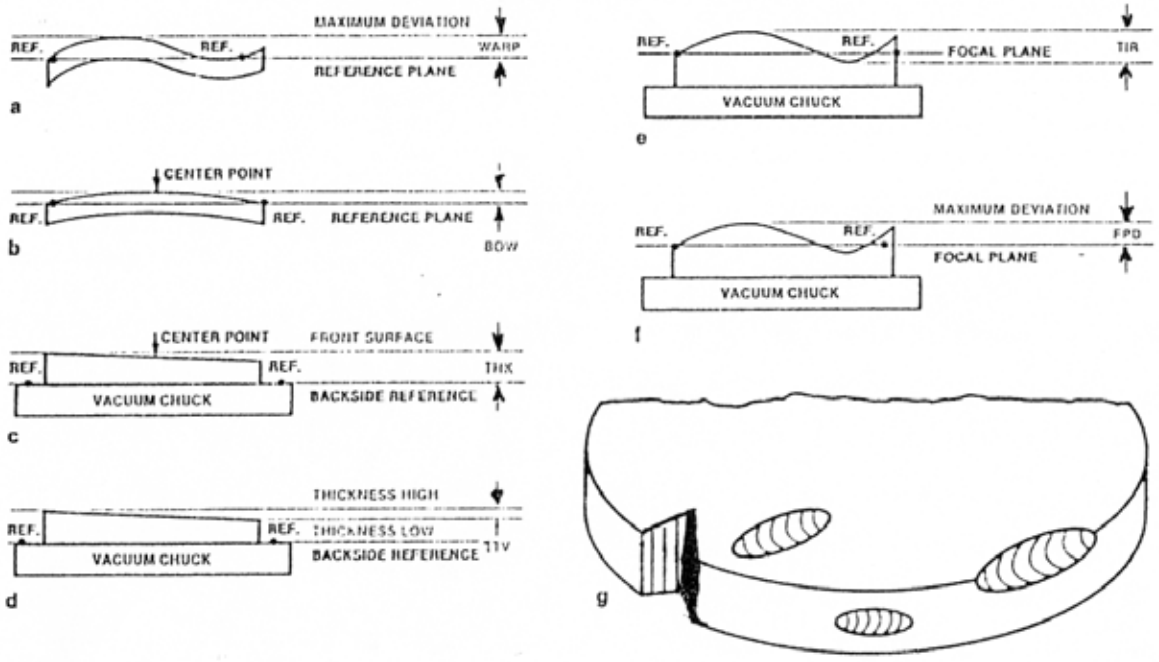


Fig. 23 Typical wafer flatness parameters (a) warp (b) bow (c) thickness (d) total thickness variation, TTV (e) total inidcator reading, TIR (f) focal plane deviation, FPD. Chips and indents in wafer shown in (g). Reprinted with permission of Microelectronics Manufacturing and Testing.

TABLE 2.3 Specifications for Polished Monocrystalline Silicon Wafers

Parameter	125 mm	150 mm	200 mm	300 mm
Diameter (mm)	125 ± 1	150 ± 1	200 ± 1	300 ± 1
Thickness (mm)	0.6–0.65	0.65–0.7	0.715–0.735	0.755–0.775
Primary flat length (mm)	40–45	55–60	NA	NA
Secondary flat length (mm)	25–30	35–40	NA	NA
Bow (μm)	70	60	30	< 30
Total thickness variation (μm)	65	50	10	< 10
Surface orientation	(100) ± 1°	Same	Same	Same
	(111) ± 1°	Same	Same	Same

NA, not available.

- 100 mm: thickness 05.-0.55 mm,
  flats: primary 30-35 mm, secondary 16-20 mm

Flats and Wafer types

- Flats are cut in the single crystal rods
- Allows wafers can to orientated and identified
- Primary flat largest: used to orientate wafer
- Secondary (minor) flat position varies with crystal and conductivity type
- Also specify wafer by resistivity (ohm-cm)
- Wafer costs: $10-$4 for 100 mm, $20 for 150 mm

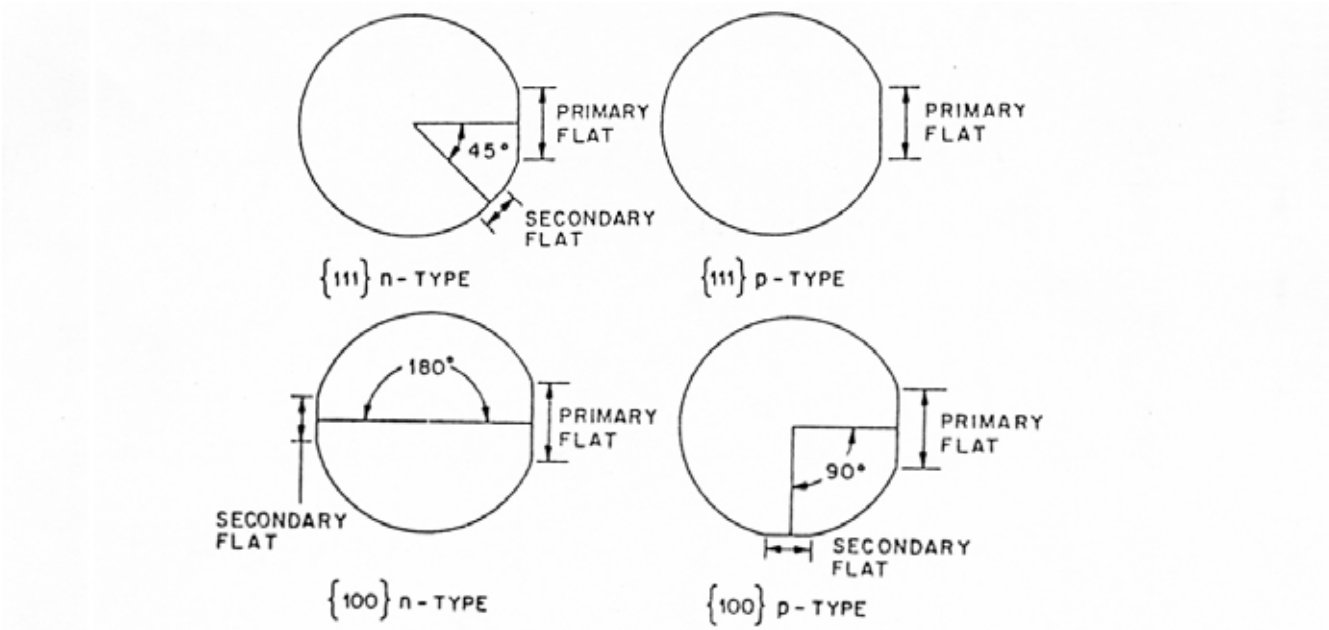


Fig. 18 Identifying flats on a silicon wafer. Reprinted with permission, from the Semiconductor Equipment and Materials Institute, Inc. Copyright the Semiconductor Equipment and Materials Institute, Inc., 625 Ellis St., Suite 212, Mountain View, CA 94043.

Thermal Oxidation and Growth of Insulators (Jaeger 3, Campbell 4)

- Oxidation of Si into SiO_2 (glass)
- Major factor in making Silicon the main semiconductor
- Glass is chemically inert
- Glass makes hard, dielectric layer

Table 3-3 Important properties of silicon dioxide

Molecular weight (amu)	60.08
Molecules ($cm^{-3} \times 10^{22}$)	2.3
Density ($g\ cm^{-3}$)	2.27
Resistivity	$\geq 10^{16}\ \Omega$ cm @ 300°K
Dielectric constant (ϵ/ϵ_0)	3.9
Melting point (°C)	~1700
Specific heat ($J\ g^{-1}\ °C^{-1}$)	1.0
Thermal conductivity ($W\ cm^{-1}\ °C^{-1}$)	0.014
Linear coefficient of thermal expansion (ppm)	0.5

Source: Reference 27, used by permission. Copyright 1967, John Wiley & Sons.

Glass Use in Semiconductors

- Looking at MosFet shows some of Glass applications

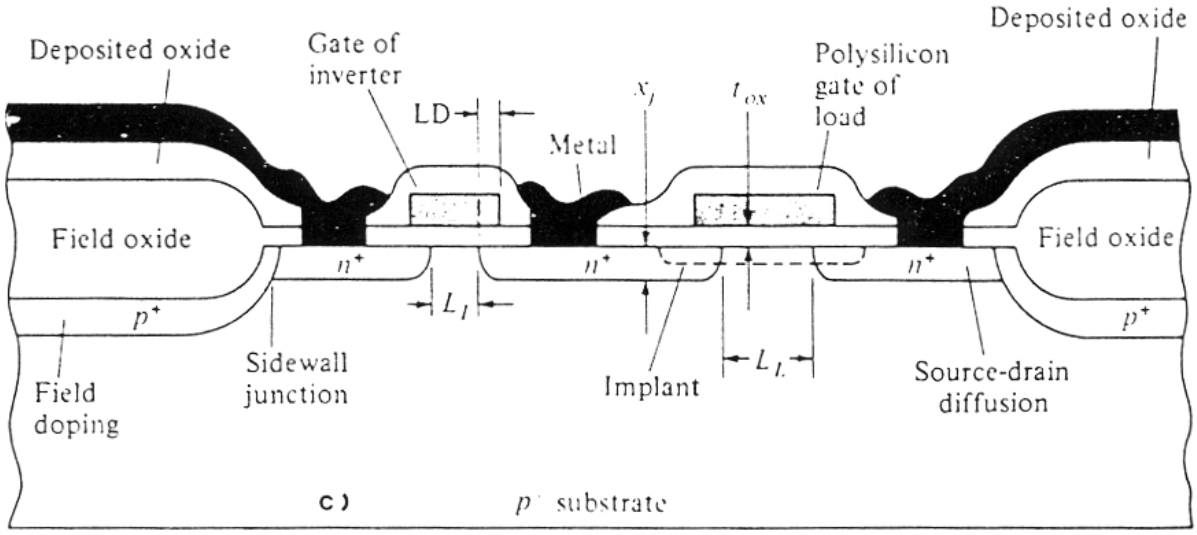


Fig. 5-13 NMOS inverter, depletion MOSFET load. (a) Schematic representation. (b) Layout. (c) Cross sectional view.[7] From D. A. Hodges and H. G. Jackson, *Analysis and Design of Digital Integrated Circuits*, Copyright, 1983 McGraw-Hill Book Co. Reprinted with permission.

Table 1. RANGE OF THERMAL SiO_2 THICKNESSES USED IN VLSI

SiO_2 Thickness	Application
60 - 100 Å	Tunneling Oxides
150 - 500 Å	Gate Oxides, Capacitor Dielectrics
200 - 500 Å	LOCOS Pad Oxide
2000 - 5000 Å	Masking Oxides, Surface Passivation Oxides
3000 - 10,000 Å	Field Oxides

Uses of Oxide Films in IC's

- Both grown oxides and Chemical Deposited (CVD) oxides

Table 1: Uses of Dielectric Films in Semiconductor Technology

- COMPONENTS IN DEVICES
- CORROSION PROTECTION
- DEVICE ISOLATION
- DOPANT DIFFUSION SOURCE
- GETTER IMPURITIES
- INCREASE BREAKDOWN VOLTAGE
- INSULATE METAL LAYERS
- MASK AGAINST DOPANTS
- MASK AGAINST IMPURITIES
- MASK AGAINST OXIDATION
- MECHANICAL PROTECTION
- PASSIVATE JUNCTIONS
- SMOOTH OUT TOPOGRAPHY

Growth of Oxide Films

- Done at high temperature in oxidizing gas
- Thickness control and density determine process
- Dry oxidation (denser oxides: gate oxide)

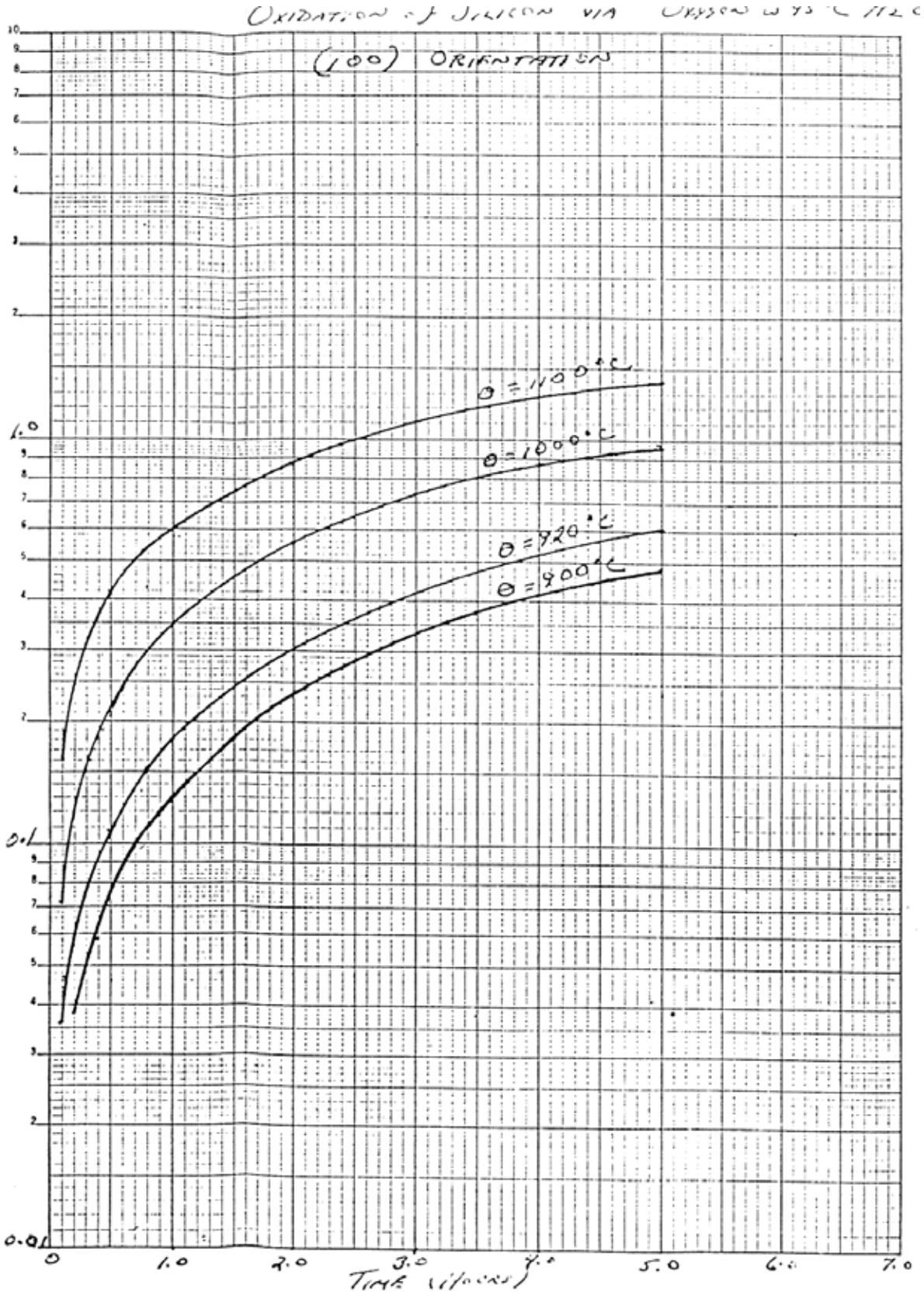
$$Si + O_2 \rightarrow SiO_2$$

- Wet Oxidation (lower density: Thick masking, Field oxides)

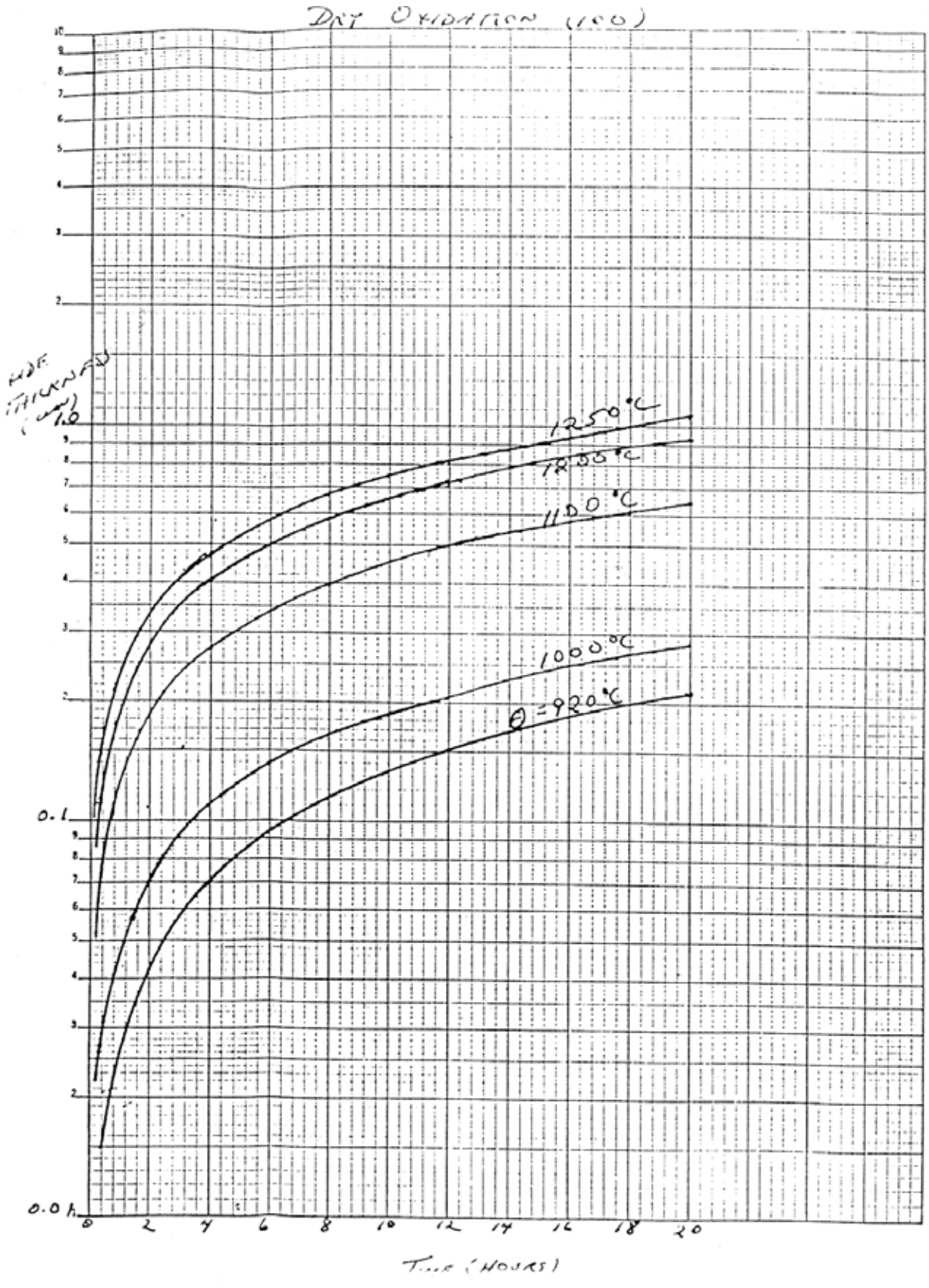
$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

- Furnace growth charts depend on wet/dry and crystal orientation

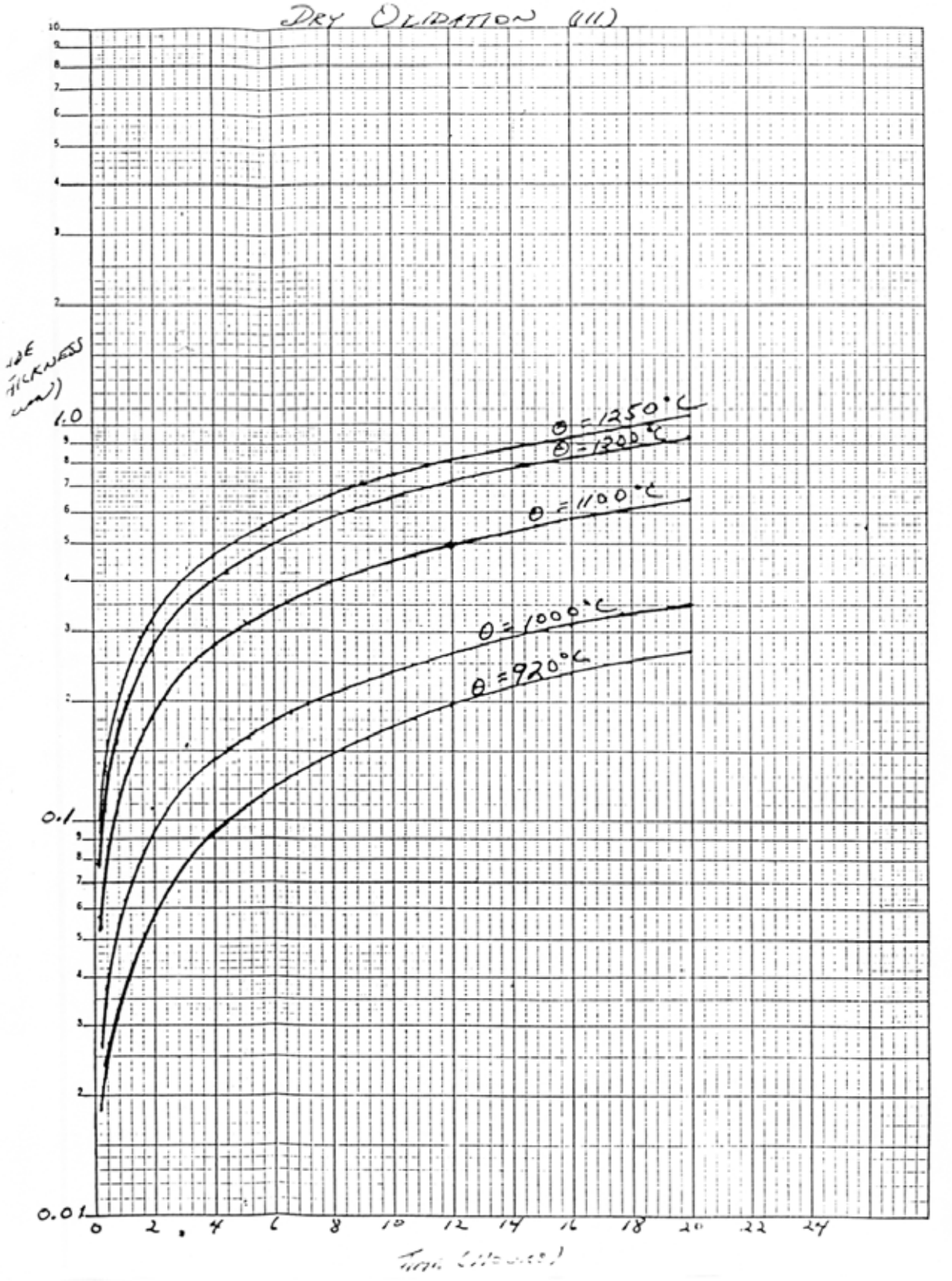
Wet Oxidation Si <100> Furnace Growth Chart



Dry Oxidation Si <100> Furnace Growth Chart



Dry Oxidation Si <111> Furnace Growth Chart



Thermal Oxidation Theory

- Consider a Si wafer with a surface oxide of thickness x_o in an oxidizing gas at some temperature T
- N_G = Density of oxidant in the gas
- Three operations occur in oxidation:
- Oxidant flows in at gas/oxide interface with flux $j_1(x_o)$
- Oxidant diffuses through oxide with flux $j_2(x)$
  x = distance above Si surface
- Oxidant consumed by reaction at Si/oxide interface $j_3(x=0)$

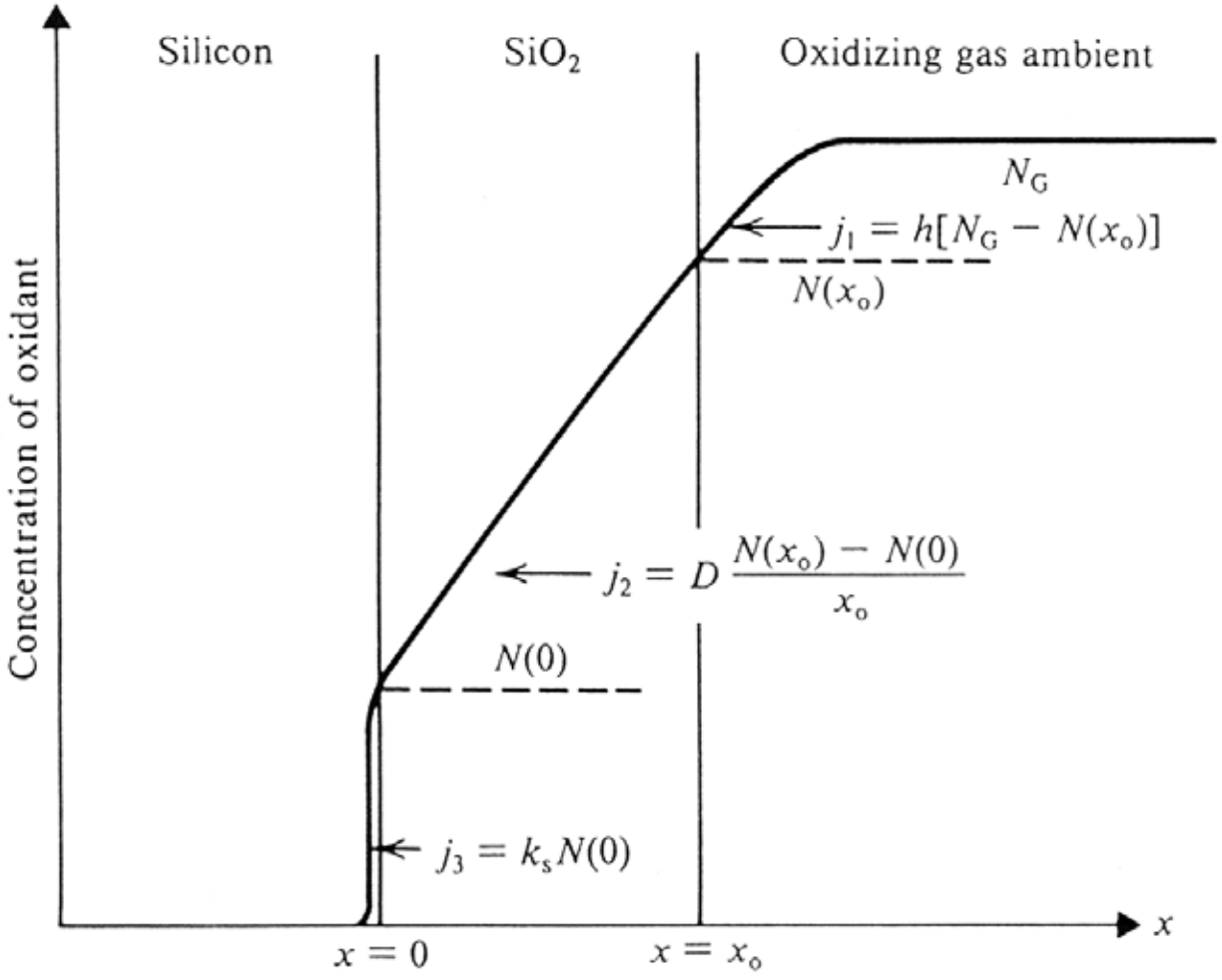


Figure 3-16 Oxidation of silicon, showing concentration of oxidant as a function of distance from Si-SiO_2 interface

Thermal Oxidation Theory

Flow at gas/SiO_2 Surface: j_1

- Flux is atoms/molecules passing given surface per unite time (unites atoms/cm^2sec)
- Oxidant declines from gas level N_G to SiO_2 surface due to flux into oxide
- Flux flow a mass transport process
- At oxide surface ($x = x_o$) the flux into the oxide is

$$j_1 = h[N_G - N(x_0)]$$

where h = mass transfer coefficient or proportionality constant
$N(x_o)$ = oxidant concentration at SiO_2 surface

- h is related to diffusion of oxidant from gas to oxide and thickness of slow moving gas layer at surface

Within oxide ($0 << x << x_o$): j_2

- Oxidant flow decreases linearly from the surface level

$$j_2(x) = D\frac{N(x_0) - N(0)}{x_0}$$

where D = Diffusion coefficient of oxidant in SiO_2
N(0) = oxidant concentration at Si surface

- Related to Fick's diffusion law

Reaction of Oxide at Si Surface: j_3

- Reaction Rate of oxide in Si surface

$$j_3(x_0) = k_s N(0)$$

where k_s = reaction rate constant

Relating Flux at Interfaces

- Oxidant is consumed only at Si: Thus under steady state

$$j_1 = j_2 = j_3$$

- Thus solving for the oxidant concentration at 0 and x_o

$$N(0) = \frac{N_G}{1 + \frac{k_s}{h} + \frac{k_s x_0}{D}}$$

$$N(x_0) = \frac{N_G\left(1 + \frac{k_s x_0}{D}\right)}{1 + \frac{k_s}{h} + \frac{k_s x_0}{D}}$$

- Growth of oxide thickness is related to reaction rate by

$$\frac{dx_0}{dt} = \frac{k_s N(0)}{\gamma}$$

where γ = no. of oxidant molecules used per unite oxide volume

$\gamma = 2.2 \times 10^{22}$ cm^{-2} for O_2 (Dry oxidation)

$\gamma = 4.4 \times 10^{22}$ cm^{-2} for H_2O (Wet oxidation)

Thermal Oxidation Solutions: Grove's Law

- Combining this with N(0) formula

$$\gamma \frac{dx_0}{dt} = \frac{k_s N_G}{1 + \frac{k_s}{h} + \frac{k_s x_0}{D}}$$

- Deal and Grove (1965) solved this assuming $x_o(t=0) = x_i$

$$x_0^2 + A x_0 = B(t + \tau)$$

with

$$A = 2D\left(\frac{1}{k_s} + \frac{1}{h}\right)$$

$$B = \frac{2DN_G}{\gamma}$$

$$\tau = \frac{x_i^2 + A x_i}{B}$$

- Thus start with film x_i which is defined to have taken time τ and grow for additional time t_2 then get film

$$x(0) = x_0(t_2 + \tau)$$

- ie: Result same as growing the film continuously for time $t = t_2 + \tau$
- Does not matter which oxidation process used for x_i time used is calculated for the process of the new growth not for process used to actually grow oxide
- Then solve the quadratic equation for x_0, using A, B & τ

Thermal Oxidation Regions

- Two main Regions

Linear Rate Constant

- When start growth limited by reaction rate when

$$(t+\tau) << \frac{A^2}{4B}$$

$$x_0 \cong \frac{B}{A}(t+\tau)$$

Parabolic Rate Constant

- Reaction is limited by diffusion mass transport when

$$(t+\tau) >> \frac{A^2}{4B}$$

$$x_0^2 \cong B(t+\tau)$$

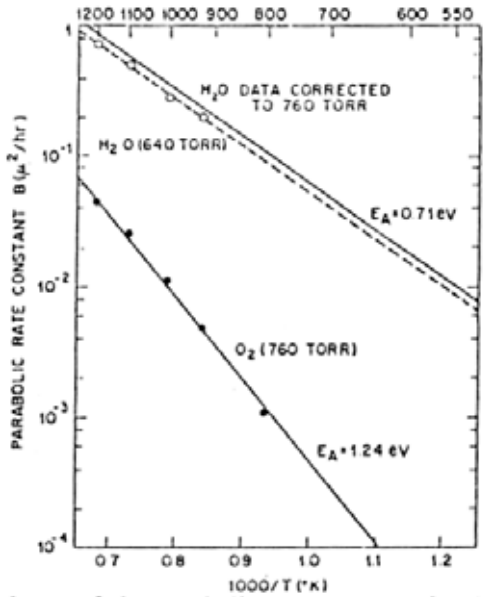


Fig. 5 The temperature dependence of the parabolic rate constant for dry and wet oxidations[3]. Reprinted with permission of the American Physical Society.

Changes of Oxidation Rate Constants

- Reaction rate k_s only depends on Si-Si bond
- Thus linear rate coefficient is

$$\frac{B}{A} = \frac{k_s h}{k_s + h}\left(\frac{N_G}{\gamma}\right) \approx k_s\left(\frac{N_G}{\gamma}\right)$$

- h experimentally has small effect
- Parabolic rate coefficient follows an Arrhenius equation
- Assumes molecules must exceed an activation energy for reaction

$$B = B_0\, exp\left(\frac{E_a}{kT}\right)$$

where T = absolute temperature (K)

E_a = activation energy (eV)

k = Boltzman's constant = 1.38×10^{-23} J/K = 8.62×10^{-5} eV/K

Table 3. RATE CONSTANTS FOR WET OXIDATION OF SILICON[3]

Oxidation temperature (°C)	A (μm)	Parabolic Rate Constant B (μm^2 /hr)	Linear rate constant B /A (μm /hr)	τ (hr)
1200	0.05	0.720	14.40	0
1100	0.11	0.510	4.64	0
1000	0.226	0.287	1.27	0
920	0.50	0.203	0.406	0

Table 4. RATE CONSTANTS FOR DRY OXIDATION OF SILICON[3]

Oxidation temperature (°C)	A (μm)	Parabolic Rate Constant B (μm^2 /hr)	Linear rate constant B /A (μm /hr)	τ (hr)
1200	0.040	0.045	1.12	0.027
1100	0.090	0.027	0.30	0.067
1000	0.165	0.0117	0.071	0.37
920	0.235	0.0049	0.0208	1.40
800	0.370	0.0011	0.0030	9.0
700	...	...	0.00026	81.0

Parabolic Rate Constants

- For Arrhenius plot Parabolic rate vs 1000/T
- Shows activation energy lower for wet oxidation (0.71 ev) than for dry (1.24 eV)

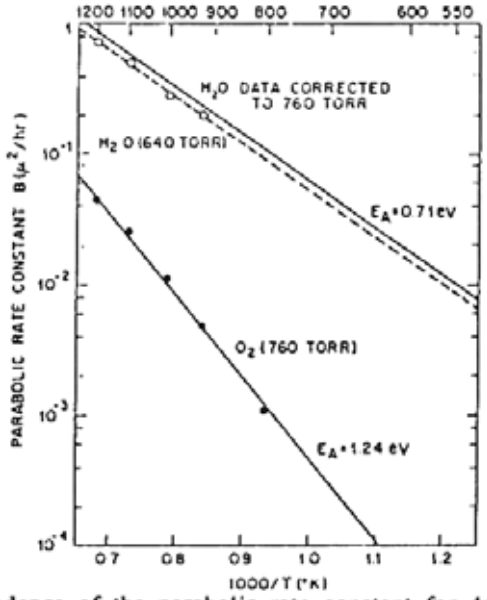


Fig. 5 The temperature dependence of the parabolic rate constant for dry and wet oxidations[3]. Reprinted with permission of the American Physical Society.

Growth of oxide film

- Oxide grows both above original Si surface
  and into the Si surface
- Si layer thickness decreased by 0.44 x_o
- Wafer gains weight from oxide
- Weight change depends difference in density of Si from SiO_2
- Note: Dry oxide has higher density than wet oxide

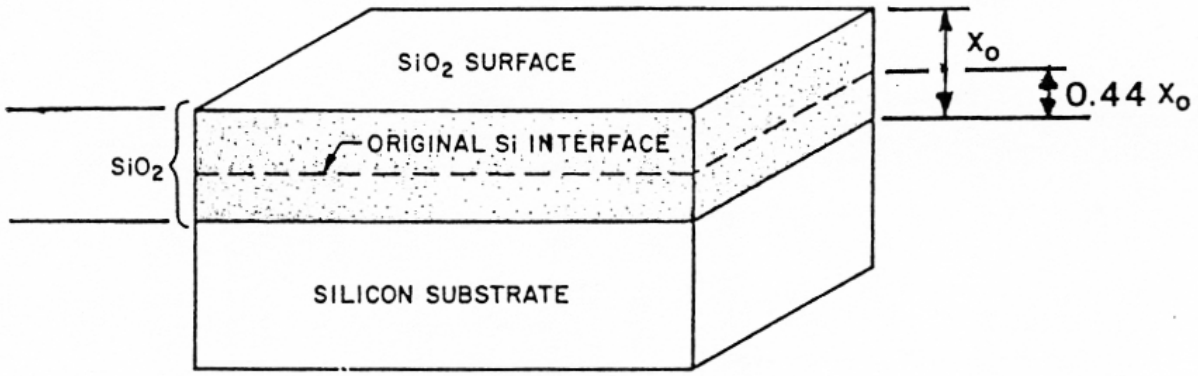


Fig. 3 The thermal oxidation of silicon model[3]. Reprinted with permission of the American Physical Society.

Good Oxide Growth Processes

- Start with removing wafers from storage
- Clean wafers
  (cleaning processes depends on previous processing)
- Load wafers into boat in Laminar Flow Hood
  (reduces particle contamination)
- Boat pushed slowly into furnace
- After time/temperature/gas cycle wafers removed
- Most important factor: Prevention of wafer contamination

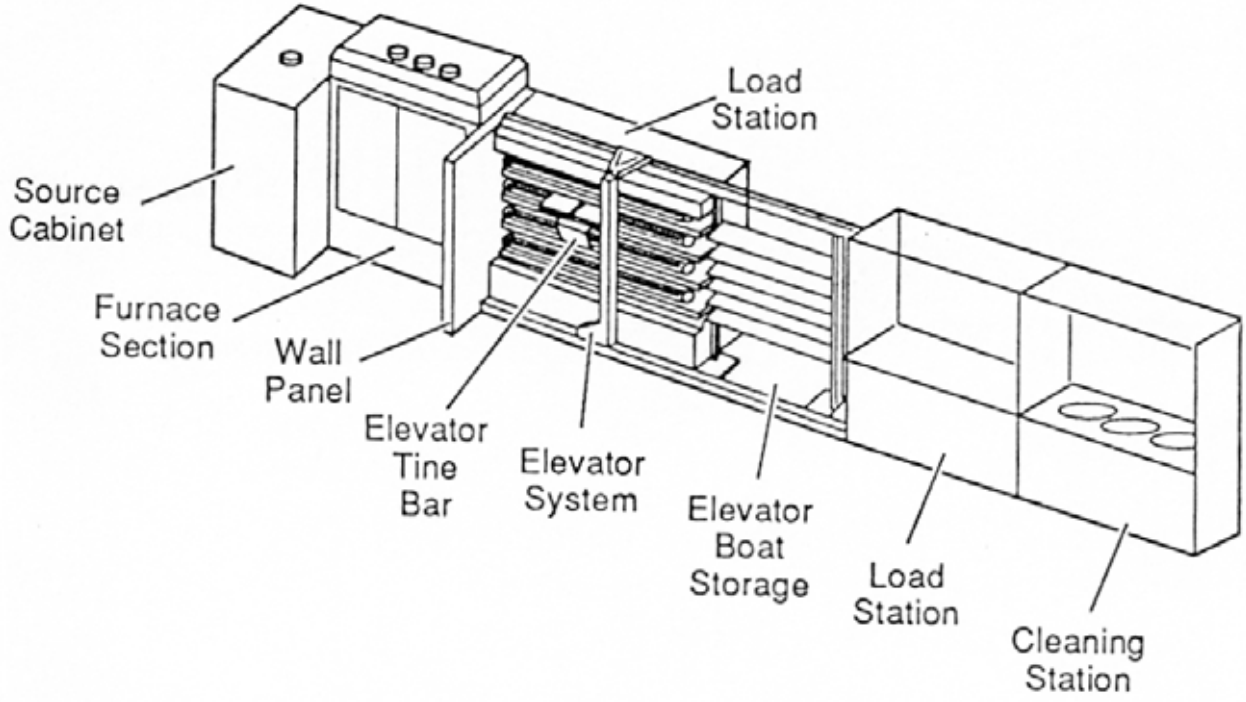


Figure 7.15 Tube furnace.

Handling Wafers

- Wafers kept in a cassette (up to 25 wafers)
- Old handling: wafer tweezers
  could damage wafers, carry dirt
- Modern: Vacuum tweezers, pencils or wands
  clean, less damage
  but more likely to drop

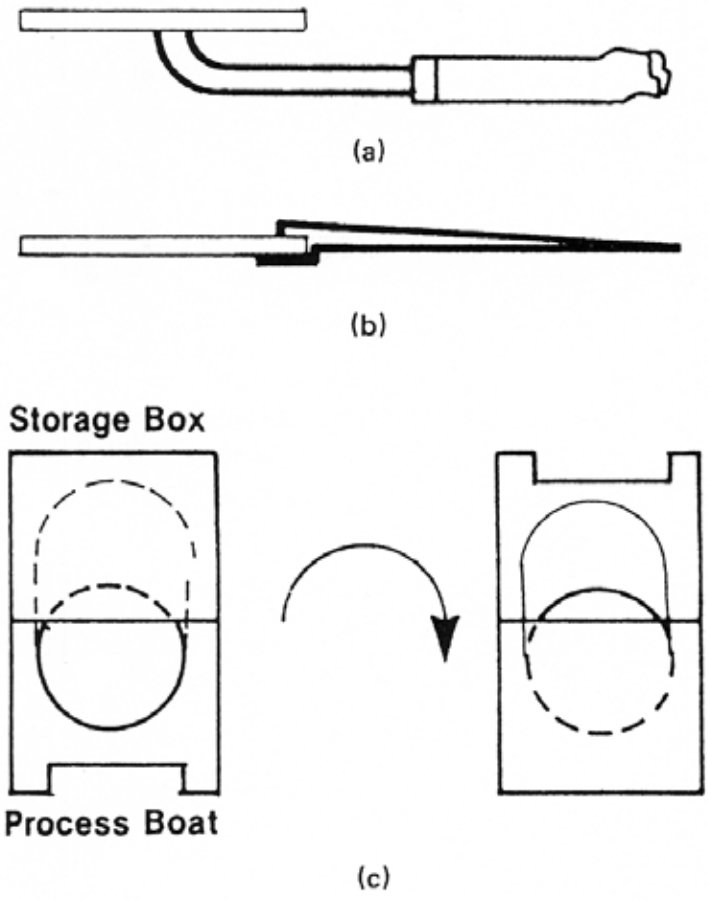


Figure 7.21 Manual wafer handling devices. (*a*) Vacuum pickup; (*b*) limited grasp tweezer; (*c*) flip transfer boats.

Standard RCA Cleaning Process

- Standard clean of wafers before any hot process
- Not possible after any metal level depositions
- Process different for initial pre-oxidation, and post oxidation

Chemicals & RCA Clean

- Always use Deionized (DI) Water
- Use Electronic Grade Chemicals
- 27% NH_4OH (Ammonium Hydroxide)
- 30% unstabilized H_2O_2 (Hydrogen Peroxide)
- 49% HF (Hydrofluroic Acid)
- 30% HCl (Hydrochloric Acid)

Step	Procedure	Temp.(^oC)	Time (S)	Purpose
1	12 parts H_2O 2 parts NH_4OH 3 parts H_2O_2	80±5	600	Organic/ Metal Removal
2	Deionized water quench	RT	>120	Rinse
3	10 parts H_2O 1 part HF *(100 part H_2O for post oxidation)	RT	30	Si surface removal
4	Deionized water quench	RT	>120	Rinse
5	14 parts H_2O 2 parts HCl 3 parts H_2O_2	80±5	600	Heavy Metal Removal
6	Deionized water cascade rinse (3 rinses)	RT	300 each	Rinse
7	Spin Dry			
8	N_2 blow dry			

Cascade Rinse

- Rinse in DI water to remove contaminates
- DI water production limited, so must control use
- Cascade 3 level final rinse
- Place wafers in lower level (twice used water)
- Move to 2nd level (once used water)
- Top level final clean

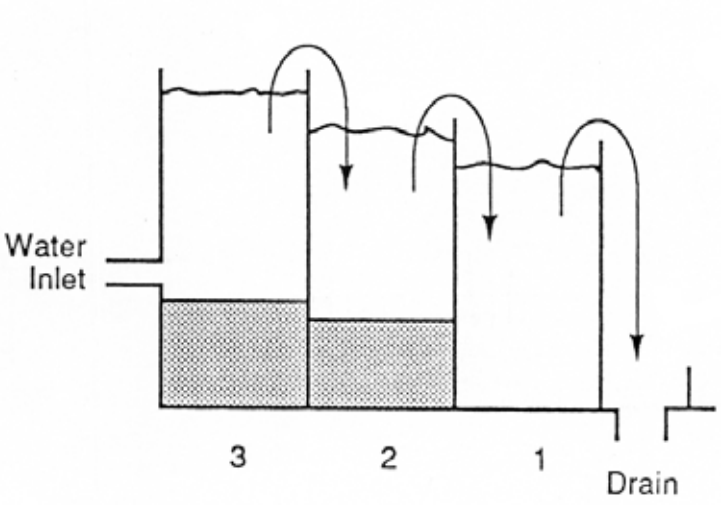


Figure 7.28 Three-stage cascade rinser.

Spin Dry

- Spin wafer to remove water
- Spin up wafer to 1000 rpm
- Removes water
- Some left on back of wafer
- Blow with high speed N_2 to remove

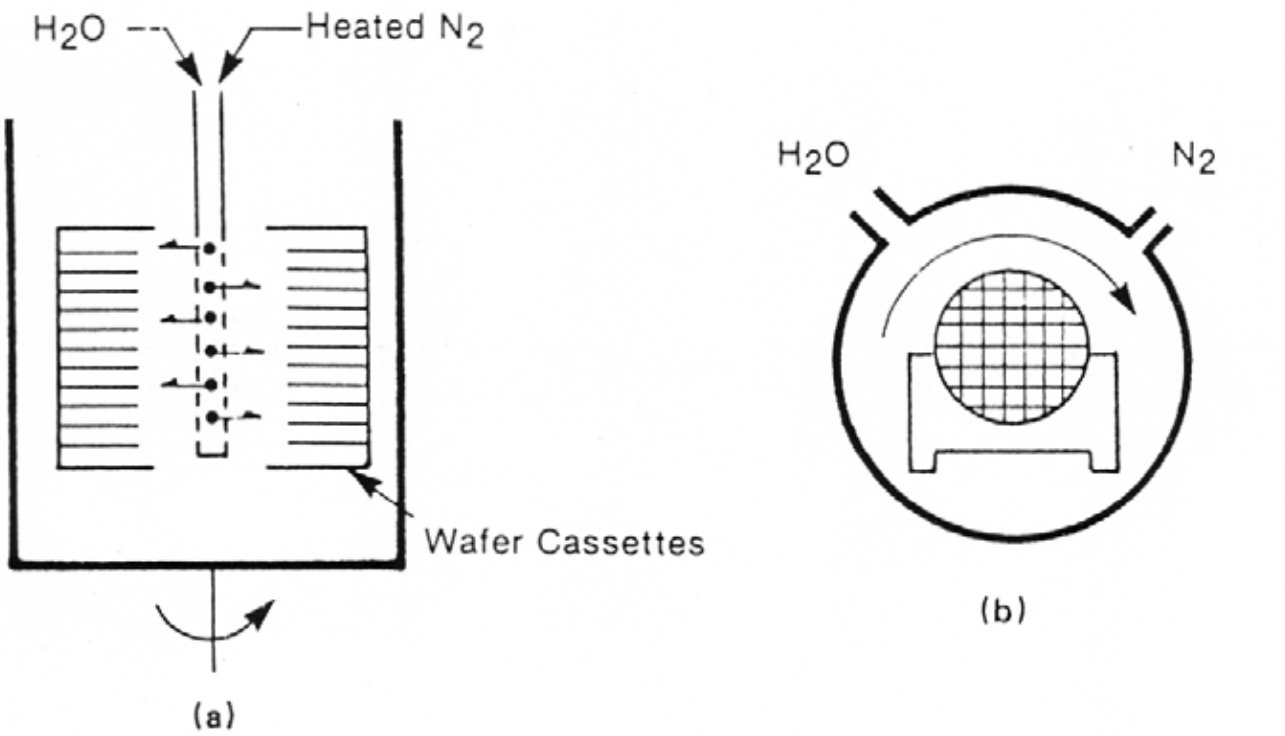


Figure 7.30 Spin rinse dryer styles. (*a*) Multiboat; (*b*) single boat axial.

Wafers Loading

- Wafers loaded into quartz boats
- Loading done in Laminar Flow Hoods

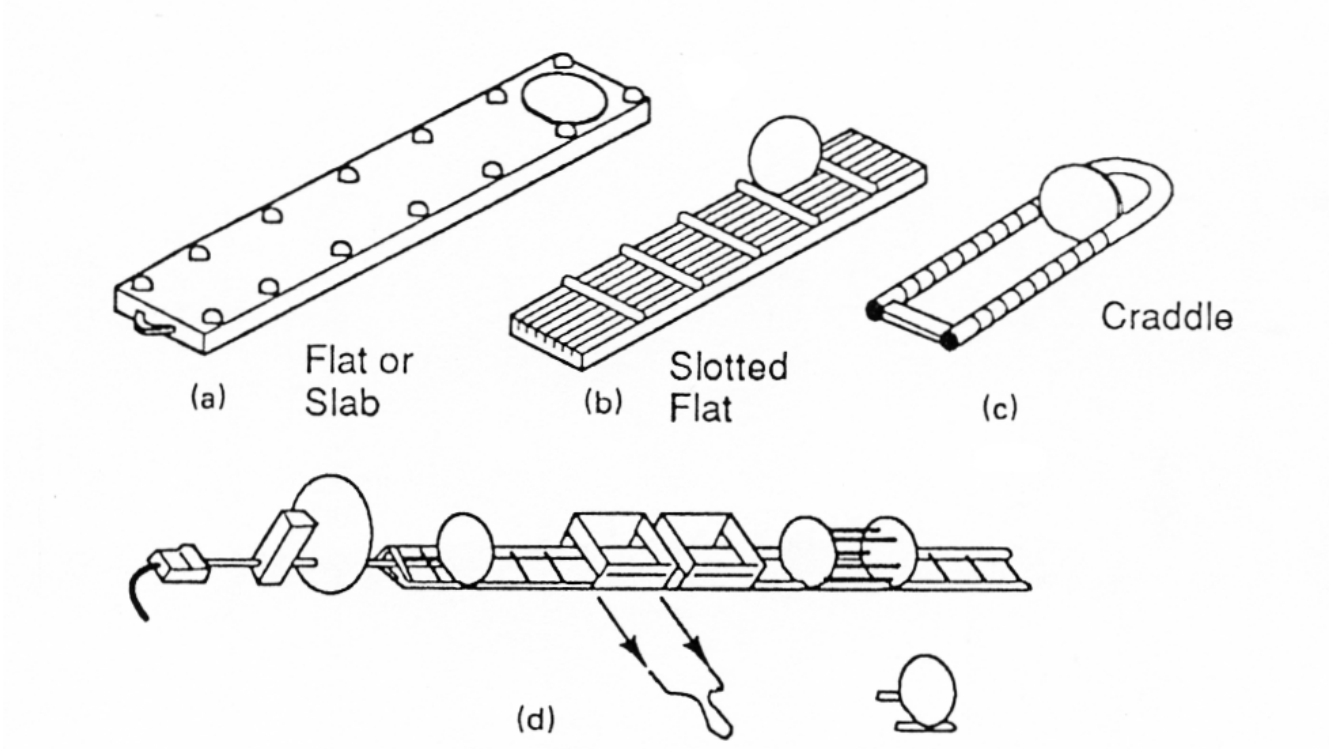


Figure 7.20 Wafer boat styles. (*a*) Flat or slab; (*b*) slotted flat; (*c*) cradle; (*d*) slotted cradle boats on paddle.

Wafers in Boat in Oxidation Furnace

- Wafers must be straight in quartz boat
- Watch for wafers sticking in boat slots

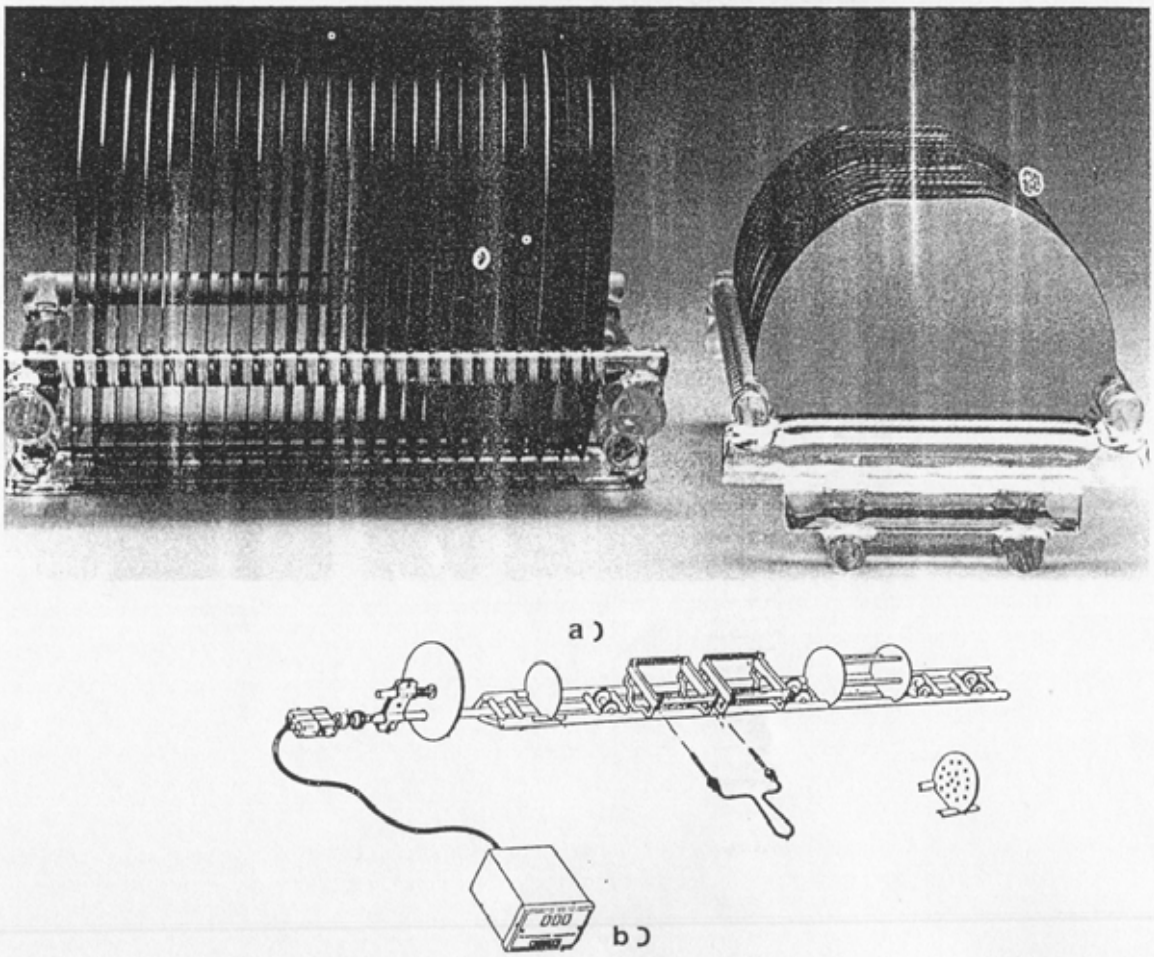


Fig. 25 (a) Wafers in an angle-slotted quartz boat. (b) Wheeled carrier. Courtesy of QBI, Inc.

Oxidation Furnace

- Wafers loaded slowly into furnace

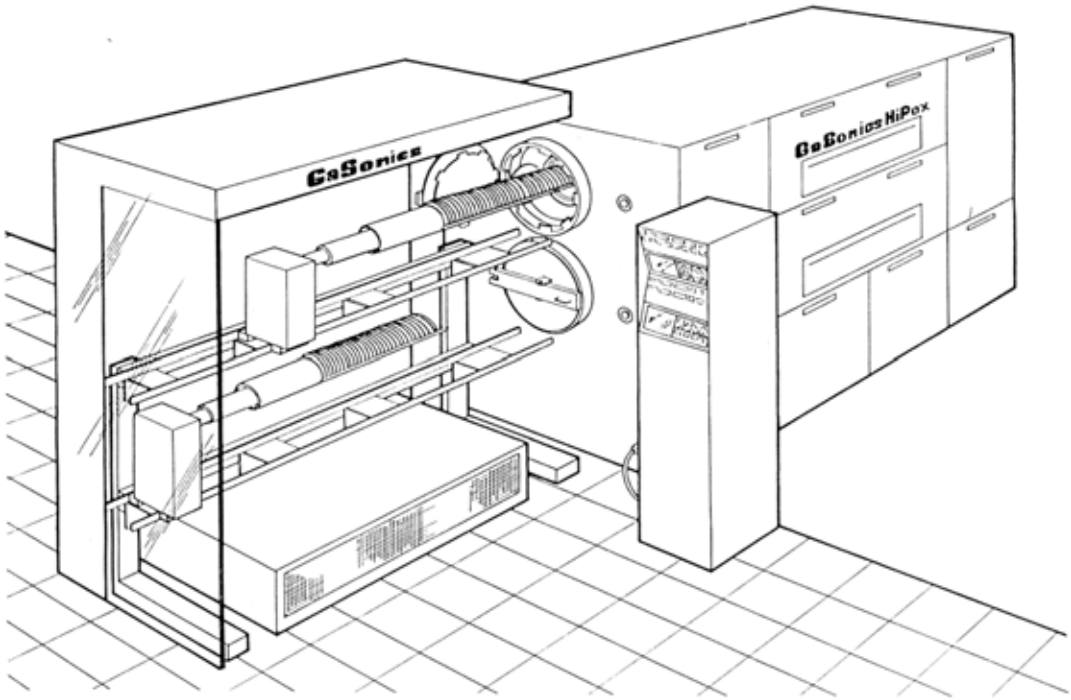


Fig. 13 Schematic representation of a commercial high pressure oxidation system. Courtesy of Gasonics, Inc.).

3 Zone Oxidation Furnace

- Furnace have 3 heat zones
- Temperature of outer zones adjusted
  keep central zone flat in temp.

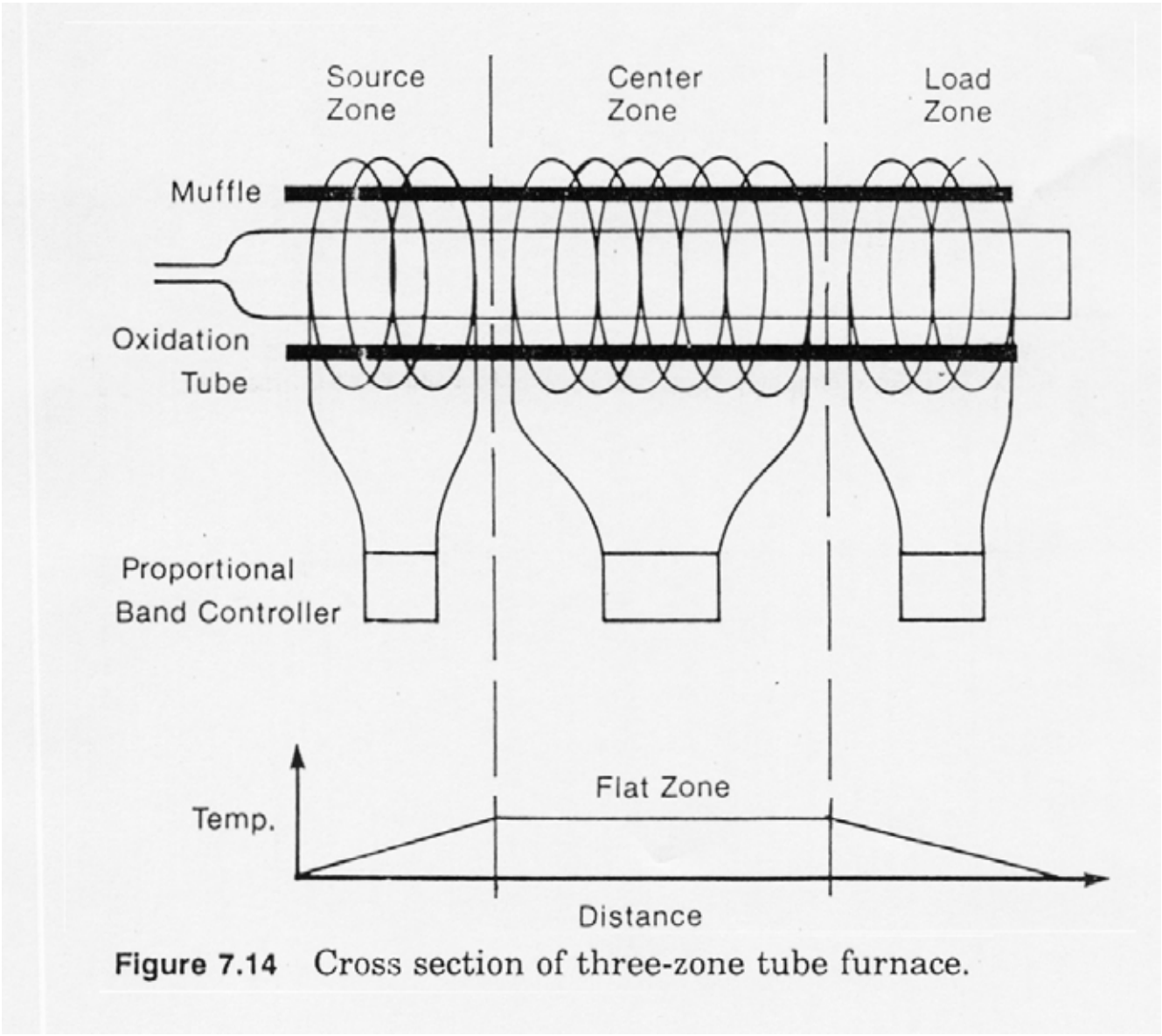


Figure 7.14 Cross section of three-zone tube furnace.

Furnace Temperature Programs

- Furnaces under computer control
- Load wafers below 700°C
- Ramp up temperature to oxidation level
  rate limited by power of furnace
- Temp. flat during oxidation
- Cool down ramp, limited by cool rate

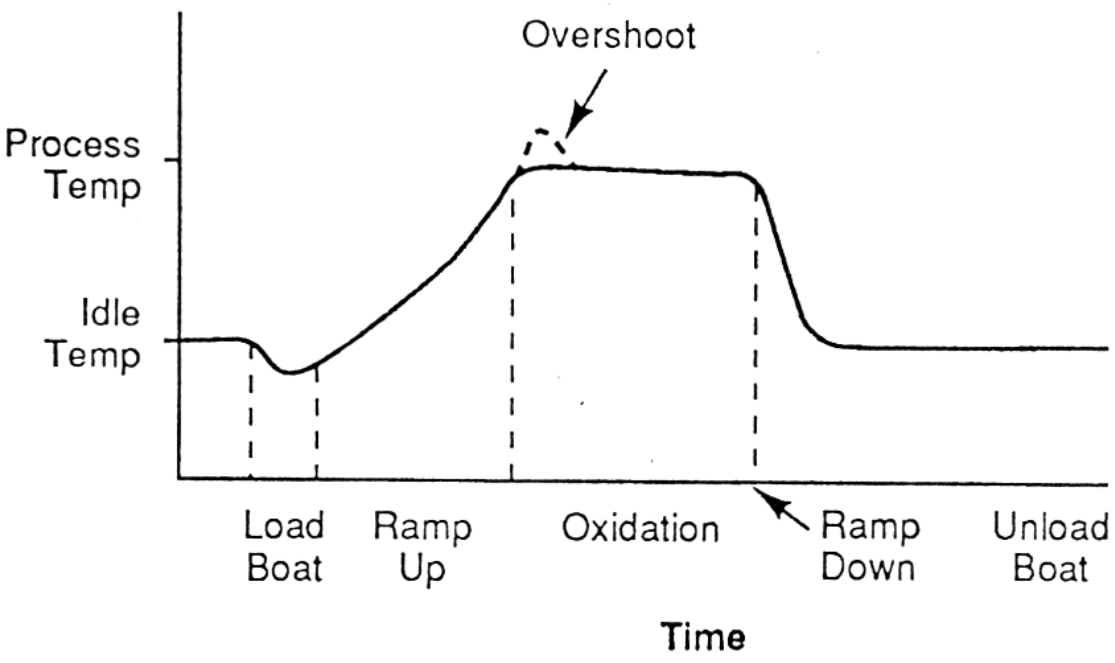


Figure 7.16 Temperature levels during oxidation.

Gas Flow in Oxidation Furnace

- Nitrogen atmosphere during ramp up and ramp down
- Little oxide growth them, keeps system clean
- During oxidation add Oxygen or steam
- Oxygen in Gas form
- Steam produced by Bubbler
  DI water in heater near 100^{o}C
- Oxygen bubbled through bubbler

Cycle	Gas	Purpose
1.	Nitrogen	Temperature Stabilization in an Inert Atmosphere
2.	Oxygen or Water Vapor	Oxide Growth
3.	Nitrogen	Stop Oxidation and Removal of Wafers in an Inert Atmosphere

Figure 7.31 Oxidation process cycles.

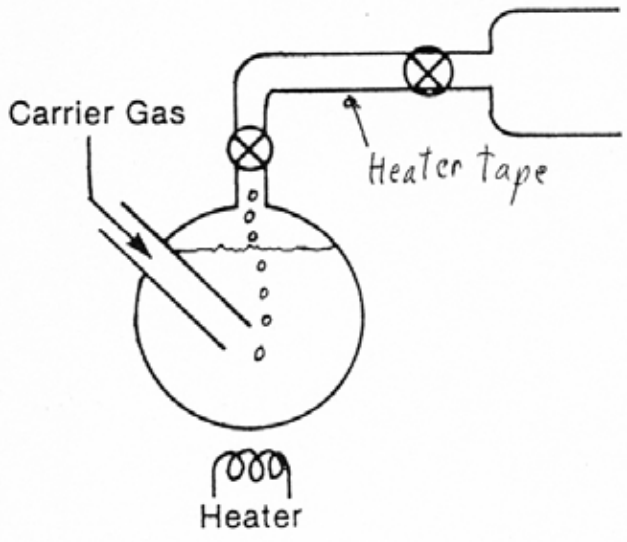


Figure 7.17 Bubbler water vapor source.

Measuring Oxide thickness with Color Chart

- Rough measure of wafer by color appearance
- Optical interference in oxide selects colors
- Colors repeat in 1/2 wavelength of light in film
- Derived by Riezman and Van Gelder (1967)
- Accurate to ±2.5 nm
- Tyger measurement system in lab uses similar interference
  Works on non-absorbing films.

Table 8. COLOR CHART FOR THERMALLY GROWN SiO_2 FILMS OBSERVED PERPENDICULARLY UNDER DAYLIGHT FLUORESCENT LIGHTING[65]

Film Thickness (μm)	Color and Comments	Film Thickness (μm)	Color and Comments
0.05	Tan	0.63	Violet red
0.07	Brown	0.68	"Bluish" (Not blue but borderline between violet and blue green. It appears more like a mixture between violet red and blue green and looks grayish)
0.10	Dark violet to red violet		
0.12	Royal blue		
0.15	Light blue to metallic blue		
0.17	Metallic to very light yellow green		
0.20	Light gold or yellow—slightly metallic	0.72	Blue green to green (quite broad)
0.22	Gold with slight yellow orange	0.77	"Yellowish"
0.25	Orange to melon	0.80	Orange (rather broad for orange)
0.27	Red violet	0.82	Salmon
0.30	Blue to violet blue	0.85	Dull, light red violet
0.31	Blue	0.86	Violet
0.32	Blue to blue green	0.87	Blue violet
0.34	Light green	0.89	Blue
0.35	Green to yellow green	0.92	Blue green
0.36	Yellow green	0.95	Dull yellow green
0.37	Green yellow	0.97	Yellow to "yellowish"
0.39	Yellow	0.99	Orange
0.41	Light orange	1.00	Carnation pink
0.42	Carnation pink	1.02	Violet red
0.44	Violet red	1.05	Red violet
0.46	Red violet	1.06	Violet
0.47	Violet	1.07	Blue violet
0.48	Blue violet	1.10	Green
0.49	Blue	1.11	Yellow green
0.50	Blue green	1.12	Green
0.52	Green (broad)	1.18	Violet
0.54	Yellow green	1.19	Red violet
0.56	Green yellow	1.21	Violet red
0.57	Yellow to "yellowish" (not yellow but is in the position where yellow is to be expected. At times it appears to be light creamy gray or metallic)	1.24	Carnation pink to salmon
		1.25	Orange
		1.28	"Yellowish"
		1.32	Sky blue to green blue
		1.40	Orange
		1.45	Violet
0.58	Light orange or yellow to pink borderline	1.46	Blue violet
		1.50	Blue
0.60	Carnation pink	1.54	Dull yellow green

Ellipsometry Film Measurement

- Non destructive optical measurement of transparent films
- Uses change of state of light polarization
  when reflected at angle from film
- Use lasers as light source
- Complicated calculations now done automatically
- Problem: Telling order of 1/2 wavelengths
  Need two measurements for that
- Index of refraction of oxide typically 1.45
- Alternative: measurement of thickness after etching

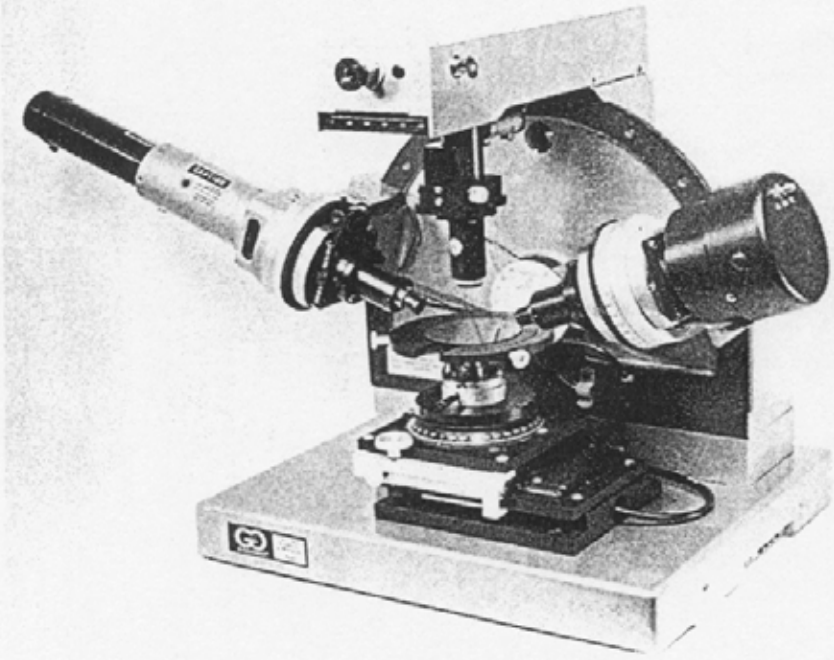


Fig. 30 Automated ellipsometer measuring system. Courtesy of Gaertner Scientific Corporation.

Trap Charge in Oxide film

- Trapped charge in dielectric films very important
- Has large effect on device behaviour, especially MOSFET's
- Trapped charge creates part of Gate Threshold Voltage
- Reason why MOSFET technology very process sensitive
- Trapped charges from 4 main sources

Interface Charge Q_{it}

- Located directly at Si-SiO_2 interface
- Caused by structural Si defects from oxidation
  metallic impurities or bond breaking at interface
- Removed by low temp. anneal: 450°C for 30 min
- $Q_{it} \sim 10^{10}$ charges/cm^2

Fixed Oxide Charge Q_f

- Q_f usually positive
- In oxide within 3.5 nm of Si-SiO_2 interface
- Caused by oxidation: depends on temperature & cooling rate
- Slow cooling: low fixed charge
- Not removable after formation (hence fixed charge)
  must compensate with dopants
- $Q_f \sim 10^{10}$ - 10^{12} charges/cm^2

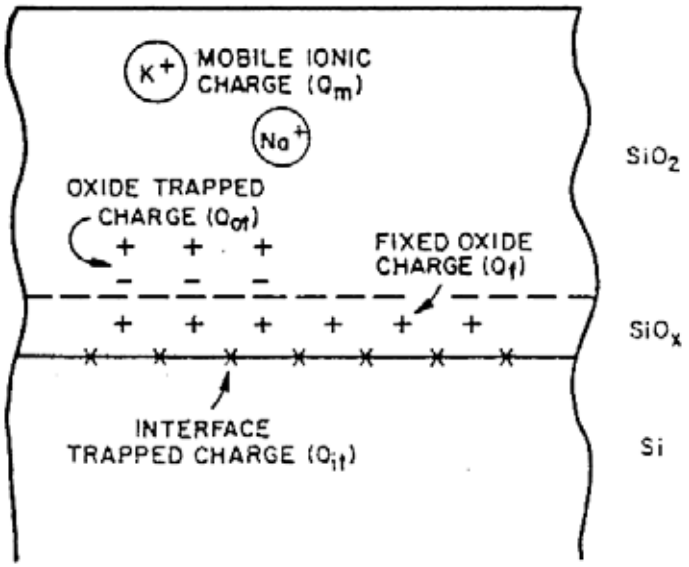


Fig. 15 Standardized terminology for oxide charges

Trap Charge in Oxide film Con'd

Mobile Ionic Charge Q_m

- Q_m from highly mobile ions of impurities
- Worse are sodium, potassium and lithium (positive charges)
- Ions move in oxide at room temp.
- $Q_m \sim 10^{10}$ - 10^{12} charges/cm^2
- Most dangerous to devices: must control impurities

Oxide Trapped Charge Q_{ot}

- Q_{ot} either positive or negative
- Defects in oxide from radiation, static charges
- $Q_{it} \sim 10^9$ - 10^{13} charges/cm^2

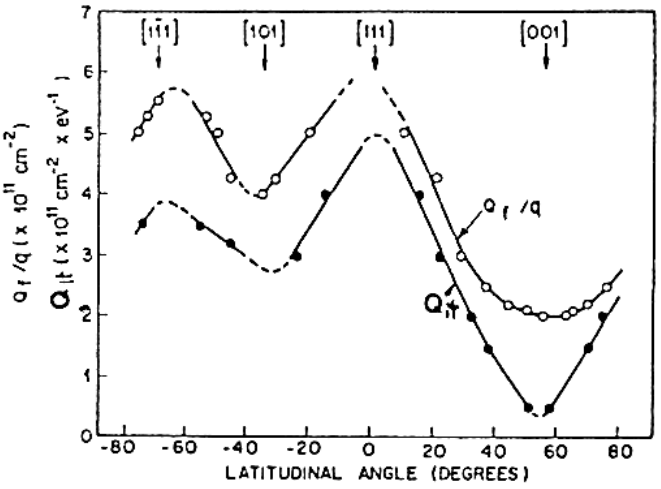


Fig. 20 Oxide fixed charge density and interface trap density as a function of the silicon orientation[49]. Reprinted with permission of the American Physical Society.

Measurement of Trapped Charges

- Measurement of trapped charge very important for Mosfets
- Done by making a metal/oxide/Si capacitor
- Measure variation of capacitance with applied voltage
- Called C-V curves (see Campbell 4.5)

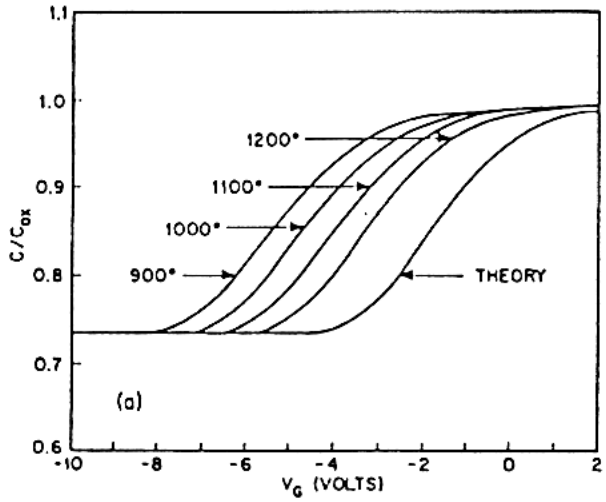


Fig. 21 High frequency C-V curves showing the effect of the presence of a positive oxide charge.[48] Reprinted with permission of the publisher, the Electrochemical Society.