**Ion Implantation**

- Most modern devices doped using ion implanters
- Ionize gas sources (single +, 2+ or 3+ ionization)
- Accelerate dopant ions to very high voltages (10-600 KeV)
- Use analyzer to selection charge/mass ratio (ie ionization)
- Bend beam to remove neutral
- Raster scan target: implant all areas at specific doping
- Just integrate charge to get total dopant level for wafer

---

**Fig. 5.1** Schematic drawing of a typical ion implanter showing (1) ion source, (2) mass spectrometer, (3) high-voltage accelerator column, (4) x- and y-axis deflection system, and (5) target chamber.
Ion Implantation

Advantages
• Precise control of doping levels
• Measure dopants dose in atom/cm²
• Much less dopant spreading (sideways & down)
• Needed for small structures

Disadvantages
• Implanters expensive $1 - $2 million
• To get depth may need high voltage/high current
double or triple ionized
• Heavy radiation damage to crystal
• Dopant need to be activated (go interstitially)
• Implant creates high temperature in resist
• Resist very hard to strip

Fig. 5.2 Gaussian distribution resulting from ion implantation. The impurity is shown implanted completely below the wafer surface (x = 0).
Ion Implant useful Formulas

• Energy $E_i$ in each ion is (in electron Volts)

$$E_i = \frac{1}{2}mv^2 = ZeV$$

Where $V =$ accelerating voltage (Volts)
$v =$ velocity of the ion
$m =$ mass of the ion
$Z = e$ charges on the ion (number of charges)
$e =$ electron charge $= 1.60 \times 10^{-19}$ C

• Thus $1 \text{ eV} = 1.60 \times 10^{-19}$ Joules

• Implant values are given as beam current in Amps
  current is same if either electrons or ions

• Total implant dose $Q$ is

$$Q = \frac{It}{ZeA}$$

Where $I =$ beam current (Amps)
t = implant time to scan area (sec)
$A =$ area (sq cm)

• Energy from ions are deposited throughout stopping range
Dopant Range with Implanter

- Ions follow a Gaussian atomic stopping range

\[ N(x) = \frac{Q}{\sqrt{2\pi} \Delta R_p} \exp \left[ -\frac{(x - R_p)^2}{2(\Delta R_p)^2} \right] \quad \text{or} \quad N_p = \frac{Q}{\sqrt{2\pi} \Delta R_p} \]

- Peak range = \( R_p \)
- Straggle of range width of Gaussian (\( \Delta R_p \))
- Both function of ion type, energy, and target (cross section for stopping in material)

Fig. 5.2 Gaussian distribution resulting from ion implantation. The impurity is shown implanted completely below the wafer surface (\( x = 0 \)).
Implanter Projected Range $R_p$

- Varies with accelerating voltage & dopant
- Ions & targets have different interaction cross sections
- Calculated using complex stopping calculations

Fig. 5.3 Projected range and straggle calculations based on LSS theory. (a) Projected range $R_p$ for boron, phosphorus, arsenic, and antimony in amorphous silicon. Results for SiO$_2$ and for silicon are virtually identical. (b) (On page 94) Vertical $\Delta R_p$ and transverse $\Delta R_{\perp}$ straggle for boron, phosphorus, arsenic, and antimony. Reprinted with permission from ref. [2].
Implanter Straggle $\Delta R_p$

- Varies with accelerating voltage & ion
- Normal straggle $\Delta R_p$ is into depth
- Transverse straggle $\Delta R_\perp$ is sideways under mask edge
Range and Straggle tables

• Implant $R_p$, $\Delta R_p$, for common ions and energies in Silicon

Table 9-1 Ion implantation characteristics of common silicon dopants

<table>
<thead>
<tr>
<th>Ion</th>
<th>Weight (amu)</th>
<th>Abundance (%)</th>
<th>$R_p$ (nm)</th>
<th>$\Delta R_p$ (nm)</th>
<th>$\Delta R_{\perp}$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B$^+$</td>
<td>10.01</td>
<td>19.78</td>
<td>106.5</td>
<td>39.0</td>
<td>46.5</td>
</tr>
<tr>
<td></td>
<td>11.01</td>
<td>80.22</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P$^+$</td>
<td>30.97</td>
<td>100</td>
<td>42.0</td>
<td>19.5</td>
<td>16.9</td>
</tr>
<tr>
<td>As$^+$</td>
<td>74.92</td>
<td>100</td>
<td>23.3</td>
<td>9.0</td>
<td>6.4</td>
</tr>
<tr>
<td>Sb$^+$</td>
<td>120.90</td>
<td>57.25</td>
<td>20.8</td>
<td>6.2</td>
<td>4.6</td>
</tr>
<tr>
<td></td>
<td>122.90</td>
<td>42.75</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$\Delta R_p$/\Delta E (approx.)(nm keV$^{-1}$)

<table>
<thead>
<tr>
<th>Ion</th>
<th>$\Delta R_p$/\Delta E (approx.)(nm keV$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B$^+$</td>
<td>3.1†</td>
</tr>
<tr>
<td>P$^+$</td>
<td>1.1</td>
</tr>
<tr>
<td>As$^+$</td>
<td>0.6</td>
</tr>
<tr>
<td>Sb$^+$</td>
<td>0.45</td>
</tr>
</tbody>
</table>

† Boron range varies sublinearly with energy above about 100 eV.

• Implant $R_p$, $\Delta R_p$, for 100 KeV Boron in different materials

TABLE 1
Boron ranges in various materials$^{13,14,15}$

<table>
<thead>
<tr>
<th>Material</th>
<th>Symbol</th>
<th>Density (g/cm$^3$)</th>
<th>$R_p$(Å)</th>
<th>$\Delta R_{\perp}$(Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>Si</td>
<td>2.33</td>
<td>2968</td>
<td>735</td>
</tr>
<tr>
<td>Silicon dioxide</td>
<td>SiO$_2$</td>
<td>2.23</td>
<td>3068</td>
<td>666</td>
</tr>
<tr>
<td>Silicon nitride</td>
<td>Si$_3$N$_4$</td>
<td>3.45</td>
<td>1883</td>
<td>408</td>
</tr>
<tr>
<td>Photoresist AZ111</td>
<td>C$<em>8$H$</em>{12}$O</td>
<td>1.37</td>
<td>10569</td>
<td>1202</td>
</tr>
<tr>
<td>Titanium</td>
<td>Ti</td>
<td>4.52</td>
<td>2546</td>
<td>951</td>
</tr>
<tr>
<td>Titanium silicide</td>
<td>TiSi$_2$</td>
<td>4.04</td>
<td>2154</td>
<td>563</td>
</tr>
<tr>
<td>Tungsten</td>
<td>W</td>
<td>19.3</td>
<td>824</td>
<td>618</td>
</tr>
<tr>
<td>Tungsten silicide</td>
<td>WSi$_2$</td>
<td>9.86</td>
<td>1440</td>
<td>555</td>
</tr>
</tbody>
</table>
Spreading of Implant Dopant from Opening

- Scattering of ions causes dopant to spread to side
- Note peak begins to die off before edge of mask
- Here assuming no implant through mask (not always true)

![Diagram showing the spreading of implant dopant from opening.](image)

Fig. 5.4 Contours of equal ion concentration for an implantation into silicon through a 1-\(\mu m\) window. The profiles are symmetrical about the \(x\)-axis and were calculated using eq. (5.4), which is taken from ref. [4].
Implant Penetration Through Masks

- Implant has dopant profile in mask but for mask material
- Note resist much less stopping power than oxide
- May result in penetration below mask
- Get tail of Gaussian
- Calculate total dopant using

![Graph showing implant impurity profile with implant peak in the oxide. The barrier material must be thick enough to ensure that the concentration in the tail of the distribution is much less than $N_B$.](image)
Buried Junctions with Implant

- Peak implant dopant is not at surface
- Thus can get n p n junctions with 1 implant
- Junction where implant falls below background \( N_b \)

![Diagram of impurity concentration](image)

**Fig. 5.6** Junction formation by impurity implantation in silicon. Two \( pn \) junctions are formed at \( x_{j1} \) and \( x_{j2} \).
Implant Variation with Crystal Angle

- $<110>$ axis has holes in structure
- Called Channeling of dopant
- Solved by putting off axis implant

![Silicon lattice diagram](image)

**Fig. 5.7** The silicon lattice viewed along the $\langle 110 \rangle$ axis. From THE ARCHITECTURE OF MOLECULES by Linus Pauling and Roger Hayward. Copyright © 1964 W. H. Freeman and Company. Reprinted with permission from refs. [3a] and [3b].

![Phosphorus impurity profiles graph](image)

**Fig. 5.8** Phosphorus impurity profiles for 40-keV implantations at various angles from the $\langle 110 \rangle$ axis. Copyright 1968 by National Research Council of Canada. Reprinted with permission from...
Dopant Depth with Implanter Voltage

- Higher implant voltages: greater depth
- Note deviation from true Gaussian:
- Light ions (e.g., Boron) backscatter from Si
- More dopant on surface side than with Gaussian
- Heavy ions (e.g., Arsenic) forward scattered (more As deeper)

Fig. 5.10 Measured boron impurity distributions compared with four-moment (Pearson IV) distribution functions. The boron was implanted into amorphous silicon without annealing. Reprinted with permission from Philips Journal of Research."
Calculation of Implant Effect

- Use Monte Carlo method to show ion spread
- Trace path of single ion as moves through crystal
- Random process included
- Launch a few million ions and measure final distribution
- eg program: Pearson Type IV distributions

FIGURE 1
Monte Carlo calculation of 128 ion tracks for 50 keV boron implanted into silicon.
Crystal Damage of Implant

- Low dose: only local damage – little effect on crystal
- Medium dose: large damage at ion point and in path
- High dose: amorphousize layer
- Increasing implants, increasing damage
- Damage areas reduce carrier velocity, create traps
- Gives poor semiconductor device characteristics

Fig. 16 Schematic representation of the disorder produced by ion implantation. (a) Low dose; light ions - individual regions with degree of disorder increasing as ions penetrate deeper into substrate, heavy ions - individual regions of more uniform disorder along entire ion trajectory. (c) Heavy doses - formation of amorphous layer.
Implant Crystal Damage

- Implant badly damages crystal
- Can turn single crystal Si into amorphous film
- Reduced by heating target - anneals out damage
- Also remove damage by raising crystal temperature after implant

Fig. 5.9 A plot of the dose required to form an amorphous layer on silicon versus reciprocal target temperature. Arsenic falls between phosphorus and antimony. Copyright 1970 by Plenum Publishing Corporation. Reprinted with permission from ref. [6].
Ion Implant and Dopant Locations

- Recall dopant atoms must be substitutional: for activation
- Ion implant tends to create Interstitial dopant: pushes out Si
- Interstitial implant ions do not contribute carriers
- True Interstitial dopant atoms: not activated

![Diagram of atomic diffusion in a two-dimensional lattice. (a) Substitutional diffusion, in which the impurity moves among vacancies in the lattice; (b) interstitialcy mechanism, in which the impurity atom replaces a silicon atom in the lattice, and the silicon atom is displaced to an interstitial site; (c) interstitial diffusion, in which impurity atoms do not replace atoms in the crystal lattice.](attachment:diagram.png)
Annealing Damage & Activating Dopants

- Need to heat surface to remove damage
- As implant level increases activation ratio decreases
- Heat moves dopant atoms into substitution point
- By $10^{14}/\text{cm}^2$ less than 10% activated at implant
- Hence heating needed to activate
- Must reach a critical temperature $\sim 800-900^\circ\text{C}$

**FIGURE 25**
Isochronal annealing of boron. The fraction of activated dopant is plotted against anneal temperature for different implant doses. (After Seidel and MacRae, Ref. 42.)
Implant Activation Defect Healing

- Heating to remove crystal electrical damage (Primary Damage)
- Dopant activation second requirement
- Problem: High temperature cause dopant to diffuse
- Activation changes dopant profiles!

![Diagram of Implant Activation Defect Healing](image-url)

Fig. 15 Ion implantation damage and annealing.
**Rapid Thermal Annealing**

- Furnace activation moves dopant around: changes profile
- Use light to heat only dopant surface
- Reach high local temperature: rapid healing/activation
- Rapidly cools when light off
- Little chance for dopant diffusion

**FIGURE 27**
Comparison of annealed profiles using furnace and scanned-laser RTA methods. Laser annealing activates the dopant without significant diffusion. (*After Gat et al., Ref. 46.*)
Rapid Thermal Annealing Systems

- Lasers expensive, heat small area
- Use light box of Halogen Heat Lamps
- Raises temperature of whole surface in seconds
  - Can actually melt wafer surface
- Water cool back of target
- As only heat surface (not whole wafer) cools quickly

![Diagram of Rapid Thermal Annealing System](image-url)

**FIGURE 5.12**
(a)Concept of a rapid thermal processing (RTP) system. (b) Applied Materials 300 mm RTP System. (Courtesy Applied Materials, Inc.)
Dopant Movement in Later Processes

- All later thermal processes change dopant positions
- Thermal processes cause diffusion
- Hence must adjust profile to take into account following processes
- Called process integration

Oxidation Dopant Segregation

- Oxidation causes N dopant to pile up at surface
- Oxidation causes P dopant depletion (into oxide)

Figure 11.26  Pile-up and depletion of dopants during oxidation. (a) Pile-up of N-type dopants; (b) depletion of P-type dopants.
Silicon Etching (Ruska Ch. 6)

- Poly Crystalline Silicon widely used as a conductor
- Called Poly Si:
- Modest resistance conductor
- Usually highly doped silicon
- Gate conductor in self aligned process
- Gate creates the position of the source/drain
- Poly Silicon etches similar to single crystal Si
- Changes depend on crystal size and doping

![Diagram of CMOS transistor polysilicon gate electrode](image)

**Figure 13.5** CMOS transistor polysilicon gate electrode. *(From Ref. 4.)*
Etching Silicon

- Typical etch: HF and HNO₃ (nitric acid) combination
- Oxidation/reduction reaction
- Nitric oxidizes the silicon
- HF removes the oxide formed

\[ 3\text{Si} + 4\text{HNO}_3 + 18\text{HF} \rightarrow 3\text{H}_2\text{SiF}_6 + 4\text{NO} + 8\text{H}_2\text{O} \]

- Ratio of HF/Nitric set etch rate
Typical Isotropic Silicon Etches

- Typically dilute with Acetic acid CH₃COOH
- Reduces the etch rate

### Table 16

<table>
<thead>
<tr>
<th>Formula</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 HF, HNO₃</td>
<td>See diagram</td>
</tr>
<tr>
<td>2 HF, HNO₃, H₂O or CH₃COOH</td>
<td>Various combinations give different etch rates</td>
</tr>
<tr>
<td>3 900 ml HNO₃, 95 ml HF, 5 ml CH₃COOH, 14g NaClO₂</td>
<td>15 µm/min</td>
</tr>
<tr>
<td>4 745 ml HNO₃, 105 ml HF, 75 ml CH₃COOH, 75 ml HClO₄</td>
<td>170 A/sec</td>
</tr>
<tr>
<td>5 50 ml HF, 50 ml CH₃COOH, 200 mg KMnO₄ (fresh)</td>
<td>Epi Etching 0.2 µm/min</td>
</tr>
<tr>
<td>6 108 ml HF, 350g NH₄F per L H₂O</td>
<td>Epi Etching  $n$ type 0.2-0.8 ohm-cm; 0.43 A/min  $p$ type 0.4 ohm-cm; 0.45 A/min  $p$ type 15 ohm-cm; 0.23 A/min</td>
</tr>
</tbody>
</table>
Diluted HF/Nitric/Acetic

- Etch rates depend on dilution

Figure 6-8 Etch rates for single-crystal silicon as a function of HF, HNO₃, and diluent concentrations. These etch rates are for dual-sided etching and must be divided by 2 to obtain the etch rate on a single surface. (Reference 8. Reprinted by permission of the publisher, The Electrochemical Society, Inc.)
Common PolySilicon Etches

- Similar to single crystal
- Must control etch rate

<table>
<thead>
<tr>
<th>Formula</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Shipley remover 1112A</td>
<td>See Shipley data sheet</td>
</tr>
<tr>
<td>2 70.4% HNO₃, 28% H₂O, 1.4% HF</td>
<td>21°C</td>
</tr>
<tr>
<td>3 100 ml HNO₃, 40 ml H₂O, 28 ml HF</td>
<td>8000 A/min</td>
</tr>
<tr>
<td>4 33 ml CH₃COOH, 26 ml HNO₃, 1 ml HF</td>
<td>1500 A/min</td>
</tr>
<tr>
<td>5 6 ml H₂O₂, 10 ml NH₄F, 1 ml HF</td>
<td>2000 A/min</td>
</tr>
<tr>
<td>6 80% HNO₃, 20% HBF₄</td>
<td>20°C</td>
</tr>
<tr>
<td>7 IM solutions Tetramethylammonium Hydroxide</td>
<td>25-45°C</td>
</tr>
</tbody>
</table>
Anisotropic Etching of Silicon

- Etching that proceeds along crystalline planes
- typically <111> plane slowest
- <100> fastest (ratio 30:1 to 100:1)
- Used extensively in micromachining & power transistors
- <100> wafers get "V" groves
- <110> wafers get vertical side walls

Fig. 14 Orientation-dependent Si etching (a) etch pattern profiles on <100>-Si,
(b) profiles on <110>-Si\textsuperscript{22}. (© 1978 IEEE).
Typical Anisotropic Etchants of Silicon

- EDP (Ethylenediamine Pyrocatecol & water) most common
- Advantages: attacks silicon, not oxide or aluminum
- Disadvantage: poisonous
- Potassium Hydroxide (KOH)
- Advantages: good crystal plane selectivity silicon
- Advantages: attacks aluminum

Table 6-2 Some formulations for crystallographically selective etching of silicon

<table>
<thead>
<tr>
<th>Ingredients</th>
<th>Composition</th>
<th>Temperature (°C)</th>
<th>Relative rate</th>
<th>Absolute Rate†</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>KOH in water/isopropanol</td>
<td>19 wt. % KOH</td>
<td>80</td>
<td>—</td>
<td>400 1</td>
<td>0.59 μm sec⁻¹</td>
</tr>
<tr>
<td>N₂H₄/water</td>
<td>100 g/50 mliters</td>
<td>100</td>
<td>10</td>
<td>1</td>
<td>0.3</td>
</tr>
<tr>
<td>Ethylenediamine/Pyrocatecol/</td>
<td>17 mliters</td>
<td>110</td>
<td>50</td>
<td>30 3</td>
<td>50</td>
</tr>
<tr>
<td>water</td>
<td>3 g</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8 mliters</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

† Etch rate for fastest-etching orientation, i.e., the one italicized under relative rate.
Aluminum Multilayer Structures

- Aluminum most common conductor in CMOS
- Conductive and easy to deposit
- Easy to etch
- Problem is to make multilevel structures
- Must make contact between Al layers
- Aluminum grows a protective insulating oxide

Figure 13.2 Cross section of typical planarized two-level metal VLSI structure showing range of via depths after planarization. (Courtesy of Solid State Technology.)
Ohmic Contacts

- Aluminum oxide can create diode like contacts
- Want a pure Ohmic contact (linear resistance)
- Get this by sinter in dry nitrogen at end
- Typical 450°C for 30 minutes
- Removes the oxide, creates ohmic contact
Aluminum Alloys

- Pure aluminum has reliability problems
- Sinter & high temperature creates difficulties
- Add Copper and Silicon
- Makes it much harder to etch

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Melting Point (°C)</th>
<th>Al/Si Eutectic (°C)</th>
<th>Density (g/cm³)</th>
<th>Resistivity (µΩ·cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>Al</td>
<td>660</td>
<td>577</td>
<td>2.70</td>
<td>2.7</td>
</tr>
<tr>
<td>Aluminum/4%Cu</td>
<td>Al 4%Cu</td>
<td>650</td>
<td>~577</td>
<td>2.95</td>
<td>3.0</td>
</tr>
<tr>
<td>Aluminum/2%Si</td>
<td>Al 2%Si</td>
<td>640</td>
<td>~577</td>
<td>2.69</td>
<td>2.9</td>
</tr>
<tr>
<td>Aluminum/4%Cu 2%Si</td>
<td>Al 4%Cu 2%Si</td>
<td>~577</td>
<td>2.93</td>
<td>3.2</td>
<td></td>
</tr>
</tbody>
</table>
**Aluminum Spike Through**

- When Aluminum heated penetrates silicon
- Si moves in Al, Al into Si
- Get spikes which can short junctions
- Suppressed by adding 1-2% Si to Al

**Fig. 2** Junction spiking and silicon migration during contact sintering.
Phase diagram

- Silicon 1.5% Aluminum Eutectic
- Lowest melting point alloy

**Fig. 1** Phase diagram of the aluminum-silicon system. From M. Hansen and A. Anderko, *Constitution of Binary Alloys*, 1958. Reprinted with permission of McGraw-Hill Book Co.
Preventing Spike Through

- Adding Si to Al prevents spikes
- Also put down barrier metal layers
- Tungsten, Molybdenum most common
- Refractory metals

**Figure 13.6** Eutectic alloying of aluminum and silicon contacts.
Aluminum and Hillocks

- When Al heated grows Hillocks
- Spikes up to 1 micron high!
- Can punch through intermetal glass layers
- Add copper to suppress
- Also for electromigration:
  	
tendency of metal to move when current applied
- Problem is Si/copper makes etching difficult

Fig. 36 Comparison of hillock-free and hillock containing films.
Aluminum Etching

• Oxidation: removal of electrons or ions from material
  \[ M \rightarrow M^+ + e^- \]

• Reduction: addition of electrons to reactant
• Redox reaction: both oxidation and reduction
• Aluminum etches are redox reactions
  \[ 6H^+ + Al \rightarrow 3 H_2 + Al^{3+} \]

• Must remove aluminum oxide for reaction
Typical Aluminum Etchants

- Most are Phosphoric Acid based (H₃PO₄)
- Acetic for dilution
- Note: without oxide Al would etch in water

**FORMULAS FOR ALUMINUM ETCHING**

**Table 11**

<table>
<thead>
<tr>
<th>Formula</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Phosphoric Acid Based Solutions</strong></td>
<td></td>
</tr>
<tr>
<td>1 77 ml H₃PO₄, 20 ml CH₃COOH, 8 ml HNO₃</td>
<td>40 - 60°C</td>
</tr>
<tr>
<td>2 73 ml H₃PO₄, 3.5 ml CH₃COOH, 4 ml HNO₃, 19.5 ml H₂O</td>
<td>40 - 60°C</td>
</tr>
<tr>
<td>3 90 ml H₃PO₄, 5 ml HNO₃, 5 ml H₂O</td>
<td>40 - 60°C</td>
</tr>
<tr>
<td>4 80 ml H₃PO₄, 5 ml CH₃COOH, 5 ml HNO₃, 10 ml H₂O</td>
<td>40 - 60°C</td>
</tr>
<tr>
<td>5 80 ml H₃PO₄, 5 ml HNO₃, 15 ml H₂O</td>
<td>40 - 60°C</td>
</tr>
<tr>
<td>6 40 ml H₃PO₄, 40 ml CH₃COOH, 10 ml HNO₃, 10 ml H₂O</td>
<td>40 - 60°C</td>
</tr>
<tr>
<td>7 75 ml H₃PO₄, 5 ml HNO₃, 20 ml H₂O</td>
<td>40°C</td>
</tr>
</tbody>
</table>
Creating a Sloped Sidewall for Al

- Want sloped sidewall for step coverage
- Thus over etch aluminum
- Allow resist to lose adhesion
Sand Removal in AlSi or AlSiCu

- Metal etch leaves Al rich Si sand
- Copper makes reaction worse
- must remove with a "sand remover" wet etch
  29% H$_2$O, 70% HF, 1% HNO$_3$
Lift Off Techniques

- Put defined resist below metal deposition
- Al goes through holes
- Then dissolve resist
- Extra Al floats away
- Problem is the "Sky is Falling Syndrome" material left behind

**FIGURE 9**
A schematic representation of two techniques for transferring resist features into a layer. (a) Shows the resist/deposition strip sequence of lift off, and (b) shows the deposit/resist/etch/strip sequence of etching.
Isotropic Etching Example

- Want 3 micron wide lines at top
- Made in oxide, 1 micron thick
- Etch with BOE at 100 nm/min
- Assume film thickness varies by ±5% over wafer
- What is the width of resist need for (a) unvaried film
  (b) Film with variation
- What is line width at substrate (a) unvaried film
  (b) Film with variation