ENSC 495/851 Lab 2 Writeup
V3.3 Apr. 11, 2012
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Purpose:

Lab 2 continues with levels 2 (N diffusion), 3 (Contact window), 4 (Metal) masks to produce functional 4 mask level device. At completion you will have created active devices (diodes, transistors, etc.), and test structures. Instruction details for each level are in the lab run sheets.

The aim of the write up will be to document what you have learned in characterizing the boron diffusion on monitor wafers, levels 2 (n diffusion), 3 (contact cuts), 4 (metal) definition/deposition processes. You will be required to measure electrical characteristics of test devices. In this write-up the theory, introduction, procedure sections can be skipped or kept to a minimum. You are only required to document observations, results, analysis and conclusions. Final report length should be 10-15 pages, not including the lab Run Sheets and large diagrams. Include in the appendix one set of your lab Run Sheets. At the end of this document, you can find the test chip layout and the layouts of the 4 individual layers in Figures 1-5 at the end of this document. Figure 6-9 show the test structures for probing. Appendix A shows the cross section of the structure for each step.

Lab 2, Week 8: Phosphorus N Diffusion photo

(1) Use oxide grown in the boron drive as the phosphorus diffusion mask. Pattern this oxide with the level 2 mask to create windows for phosphorus diffusion (for emitter and N contacts).

(2) Apply photoresist* and pattern the oxide with level 2 mask using the photo process sheets. Check the alignment during the inspection before etching. Do not pattern monitor wafers.

* While waiting for soft and hard bake, you can carry out step (5).

(3) Using BOE, etch the field oxide using the oxide etch process sheet. Etch to de-wet (estimate the time from the oxide thickness estimate) and inspect. Strip the resist. Do not pattern the monitor wafers. Just do an oxide strip (this step may be carried out by Andras or Kourosh ahead of time).

(4) Inspect the wafers. Measure misalignment error on one wafer. Take digital photo of alignment plus signs at center and 4 compass corners of the wafer. Extract alignment errors and carry out analysis based on these photos. Use other computers to view these photos so as not to hold up the microscope station. Measure the width of lines and spaces on the level two 10-micron etch test structures at wafer center.

(5) On the monitor wafer measure the sheet resistance of the boron diffusion (after last week's drive in) using a 4 point probe.

(6) On a regular wafer measure the oxide thickness using profilometer (Alpha Step 500) on the large openings of the second level etch test structure (30-micron test structures) and the alignment structure (plus sign).

Phosphorus Mask Writeup (level 2)

(1) For each step of the clean, note the process step name, what did you observe on the wafer (was it clean, did the step run over time, did anything go wrong). Comment on what could be done to improve the process, both from a point of speeding it up, and of increasing the cleanliness.

(2) From the colour chart and the time/temperature oxidation parameters, estimate the oxide thickness on your wafer. Also obtain actual oxide thickness using the profilometer. Compare the oxide

thickness determined by these two methods. How does actual oxide thickness compared to that expected from the process parameters? Suggest what process parameters have the most significant effect on this discrepancy.

(3) Based on the measured alignment results, what are the rotation/translation/run out errors for this level? How good is your mask alignment operation? What are the widths of the lines and spaces of the 10μm L test structures? How good is your oxide etch?

(4) What was the sheet resistance of the monitor wafer measured using the 4 point probe? Assuming the initial diffusion from the boron solid source produced Boron solubility limit at the wafer surface. Estimate the sheet resistivity of the boron diffusion layer after drive in, and compare that to the measured result. Do they agree? (This is part of the Lab1 report. No need to repeat in Lab2 report)

Lab 2, Week 9: Phosphorus Diffusion

You will use the patterned oxide mask produced in Week 8 for phosphorus diffusion this week.

(1) Start with an RCA clean to remove residual resist from the wafers, but using a 100:1 HF step. Use the Modified RCA clean process sheets. Monitor wafers do not have oxide diffusion mask, and can be cleaned using RCA clean or Modified RCA clean.

(2) Phosphorus diffusion (see phosphorus run sheets). Clean wafers are loaded face towards the phosphorus oxide/nitride disks. Max of 8 wafers can be done at one time. Furnace will be loaded at 800^{o}C and ramped to 1000^{o}C in nitrogen, followed by 60 minutes 1000^{o}C diffusion, and ramp down to 800^{o}C. Unload wafers.

Diffusion Drive in (level 2)

(1) Remove wafers from the phosphorus diffusion furnace and transfer directly to the boat for the oxidation furnace.

(2) Do an oxidation to drive in the phosphorus, and to make the field oxide for the contact cuts. Use 1000^{o}C for 20 minutes in steam and 20 minutes in N2. Measure the oxide using the colour charts.

N Phosphorus Diffusion Step Writeup (level 2)

(1) For each step of the clean (done before diffusion) note the process step name, what you observed on the wafer (was it clean, did the step run over time, did anything go wrong). Comment on what could be done to improve the process, both from a point of speeding it up, and of increasing the cleanliness.

(2) Note the time/temperature used in the process. Did anything occur that might indicate alterations in the process?

(3) What did the wafers look like after diffusion? Relate the defect pattern (if any) to how the wafer was treated in the cleaning process. For the diffusion process, note any problems (like spots seen on the wafer).

(4) From the colour chart and the time/temperature oxidation parameters, estimate the oxide thickness on your wafer. Also obtain actual oxide thickness using the profilometer (to be carried out next week after you make the contact cut). Compare the oxide thickness determined by these two methods. How does actual oxide thickness compared to that expected from the process parameters? Suggest what process parameters have the most significant effect on this discrepancy.

Lab 2, Week 10: Contact Cut (Level 3)

Use oxide grown in the phosphorus drive in step to electrically isolate metal layer from silicon, except at places where we want to make electrical connections to silicon via the contact cut.

(1) Using the oxide layer grown during phosphorus drive in last week for field oxide. Level 3 mask patterns oxide to produce metal-to-silicon contact via.

(2) Apply photoresist* and pattern the oxide layer with level 3 mask using the photo process sheets. Check the alignment during the inspection before etching. Do not pattern monitor wafers.

* While waiting for soft and hard bake, you can carry out step (5).

(3) Using BOE, etch the field oxide using the oxide etch process sheet. Etch to de-wet (estimate the time from the oxide thickness estimate) and inspect. Strip the resist. Do not pattern the monitor wafers. Just do an oxide strip.

(4) Inspect the wafers. Make sure there is no gross overetch of the oxide layer that may render the wafer useless.

(5) On the monitor wafers measure the sheet resistance of the phosphorus diffusion (after last week's drive in) using a 4 point probe.

(6) On a regular wafer measure the oxide thickness using profilometer (Alpha Step 500) on the large openings of the third level etch test structure (one of the 10-micron, 20-μm or 30-μm test structures) and the N MOSFET (going through the contact cuts).

(7) * An attempt will be made before metallization (optional, Albert will help you with this) to measure the beta of NPN transistor.

Contact Cut Writeup (level 3)

(1) For each step of the clean, note the process step name, what did you observe on the wafer (was it clean, did the step run over time, did anything go wrong). Comment on what could be done to improve the process, both from a point of speeding it up, and of increasing the cleanliness.

(2) From the temperature oxidation parameters, estimate the oxide thickness on your wafer. Also obtain actual oxide thickness using the profilometer. How does actual oxide thickness compared to that expected from the process parameters? Suggest what process parameters have the most significant effect on this discrepancy. Summarize the theoretical and actual oxide thicknesses obtained in the three layers of oxide: boron diffusion window, phosphorus diffusion window and the contact window mask. (You can use the spreadsheet from HW#2 solutions to reduce calculation time). Suggest one possible reason why the actual thicknesses are different from those predicted by theory.

(3) Based on your inspection, will your alignment error and over etch degrade device performance?

(4) Assuming the initial n diffusion from the solid phosphorus source was a very thin layer (say 1-10 nm) at the phosphorus solubility limit, what depth of layer would you estimate from the drive in (do not forget that this is going into the boron doped p region)? Estimate the sheet resistivity of the phosphorus diffusion layer after last week's drive in, and compare that to the measured result. Do they agree?

Lab 2, Week 11 : Metallization Definition step (level 4)

The Metallization deposition on your wafers will be carried out by Bill prior to this lab.

(1) Spin on photoresist and pattern the oxide with level 4 mask using photoresist process sheets. Align to the level 4 plus signs the level 1 alignment structures. Note that as this is a light field mask the structure is place inside the level one structure. Make certain to check alignment during inspection before etching.

(2) Etch with the aluminum etch (phosphorus acid) -see metal etch process sheets.

(3) Measure the aluminum thickness with the profilometer. Use the 30μm L resolution test structures.

(4) Sinter the wafers at 450^{o}C for 30 minutes in nitrogen to make the contacts.

Metallization Writeup (level 4)

(1) What does the metal layer look like on the wafers after deposition? Do you expect good step coverage from inspection? Is the profilometer metal thickness measurement consistent with wafer weight difference measurement? Explain any discrepancy.

(2) For each spin coating, exposure, and development step, did anything happen which might have affected the result? After definition but before etching what type of defects did you see on the wafer? Can you suggest causes for these?

(3) What was the metal etch time? What did you use for the end point of the etch, and how much over etch did you give it?

(4) After metal etching what type of defects did you see on the wafer? Can you suggest causes for these? What did you use to see if there was any remnant oxide (metal) left? Look at the edges of the oxide between metal fingers on the snake or solar cell.

(5) After the sinter step did the metal change appearance?

(6) Based on your inspection, will your alignment error and over etch degrade device performance? If so, describe them qualitatively.

Lab 2, Week 12: Measurements and Writeup

Process Measurements

These are measurements that establish the some the process result

(1) Alignment mark measurements. Using the microscope measurement system measure the alignment mark structures widths of each levels. Then use this measurement to scale a captured microscope photo of the alignment mark to establish the misalignment of each level relative to level 1, and each other level.

(2) Using the profileometer measure the profile of the finished structures. In particular, do the profile of the metal lines on a flat surface (the metal level 4 L's – see Figure 1). This gives the base thickness of the metal. Then do a profile of the metal probe pads for the Boron and Phosphorus contact. Finally profile the oxide etch step in the metal step coverage devices (see Figure 8)

Electrical and Device Measurements

ENSC 495 students will do at least parts 1 to 5. Graduates with a minor project the full set of tests. For the curve tracer use a digital camera to take the curve traces for the characteristics. Download the Tektronix 576 manuals to consult on using the curve tracer.

Before starting any measurements confirm the probes are working properly. To do this place one probe on the contact pad making good contact (instructions in the lab). Then place a second probe on the same contact pad and make certain that you get a short between them (use the curve tracer or ohm meter). Check each probe this way (this also gets you used to putting the probes down).

(1) Using the 20-micron Van de Pauw & 4-Point resistance test structures shown in Figure 6 to measure sheet resistance of the aluminum, boron diffusion and phosphorus diffusion layers. Use dimensions given to calculate the sheet resistance for each layer. Compare the three sets of sheet resistance values (4-point probe, Van de Pauw, and 4-Points test structure) and comment on difference observed.

(2) Measure the contact resistance between the two adjacent substrate contacts (see Figure 7). Calculate the resistance per contact.

(3) Using the substrate contact and the diode (boron) contacts (see Figure 7) with a curve tracer measure the diode IV characteristics. What is the turn on voltage? From the photographs of the curve tracer take a measurements at a few forward and reverse voltages. Find the following: forward resistance of the diode, reverse leakage current, breakdown voltage.

(4) Use a curve tracer measure the solar cell first as a diode (in the dark). Use the substract contact (Figure 7) and the Solar cell contact pad (Figure 8) for the measurement. Measure reverse leakage current and breakdown voltage. Repeat with microscope light turned on at different levels (control knob settings 1, 2 and 3).

(5) Test the dual-base-contact NPN transistor using the curve tracer. Use the substrate transistor contact as the collector (See Figure 9 for the Collector, Base and Emitter contacts). Measure the transistor characteristics (in the dark). What do the transistor action characteristic curves look like (note the base current, collector current etc)? Calculate the transistor beta (current gain) at collector currents around 100μA and 3mA. Also use the curve tracer to measure the base-to-emitter and base-to-collector diode characteristics.

(6) Use the Boron and Phosphorus diffusion specifications, diffuse source data sheets, information from textbook(s), measured parameters, and anything else you can get your hands on to give a very rough estimate of the impurity profile and junction depths. Use this simplified model to predict the beta of the NPN transistor and compare that to the measured value. I don't expect them to match, or even close. Give a qualitative account of why this simplified model does not predict the beta well.

(7) Display the transistor action characteristic curves of a lateral PNP (find one in the test chip and show a sketch of its structure in your report). What is the β?

(8) Measure and display the transistor action characteristic curves with the curve tracer of either a NMOS or a PMOS transistor (you can do both if you want) using the curve tracer. See Figure 9 for the Source (S) Drain (D) and Gate (G) contacts. What appears to be the threshold voltage for the devices

Additional Lab Report Structure

Lab Write-up and Process Sheets

Include a combined copy of your process (run) sheets in the report. You may combined all the notes into one sheet set or create an assembled set. Attached scanned or copied version of these to the report – you will need to keep the originals for the final report. Note length of the report does not include these process sheets.

Final Write-up Conclusions

On the basis of the results what can you comment about where you found problems in each step – what gave you the most difficulty or created the most problem. Identify which wafer you think is the best at this point in the lab. In the report state how much work each student in your group did on the report.

The Lab report will be due one week after the end of lab 1. Submit the report both in paper and electronic form (pdf file). The electronic form is so that we can collect data from all groups over the years to help us improve the fabrication process.

Figure 1 ENSC 495/851 test chip layout

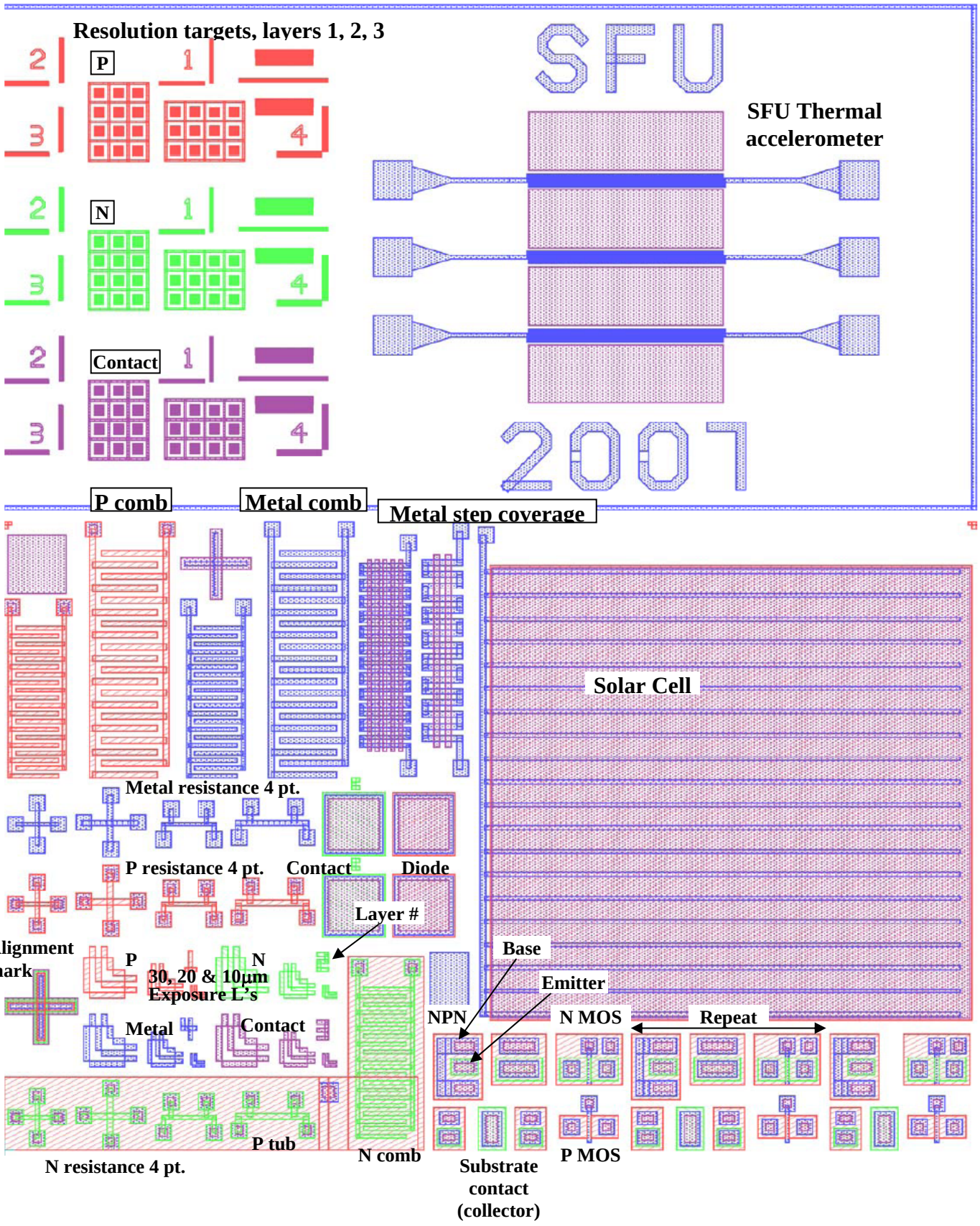


Figure 2 PDIF mask (level 1)

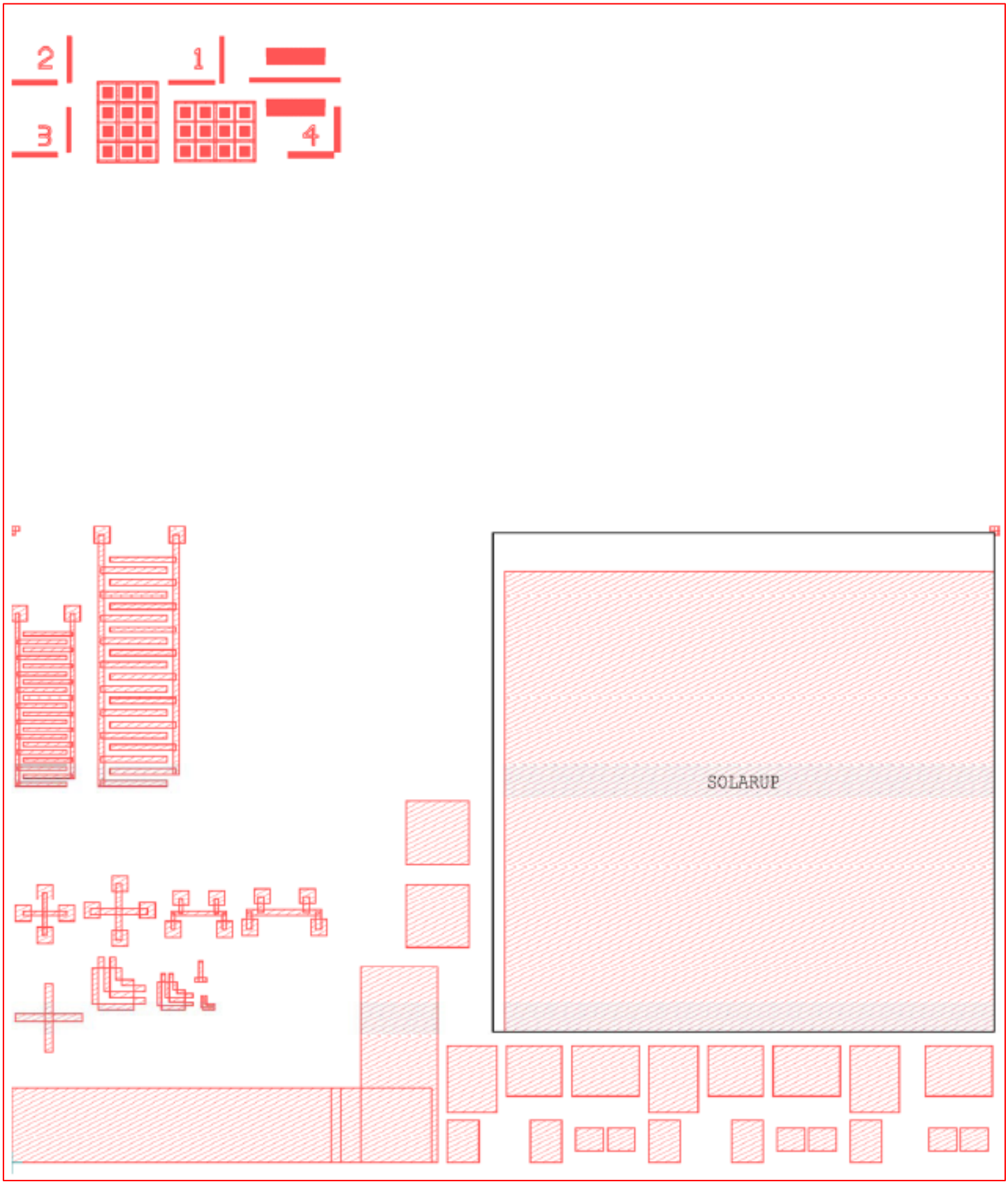


Figure 3 NDIF mask (level 2)

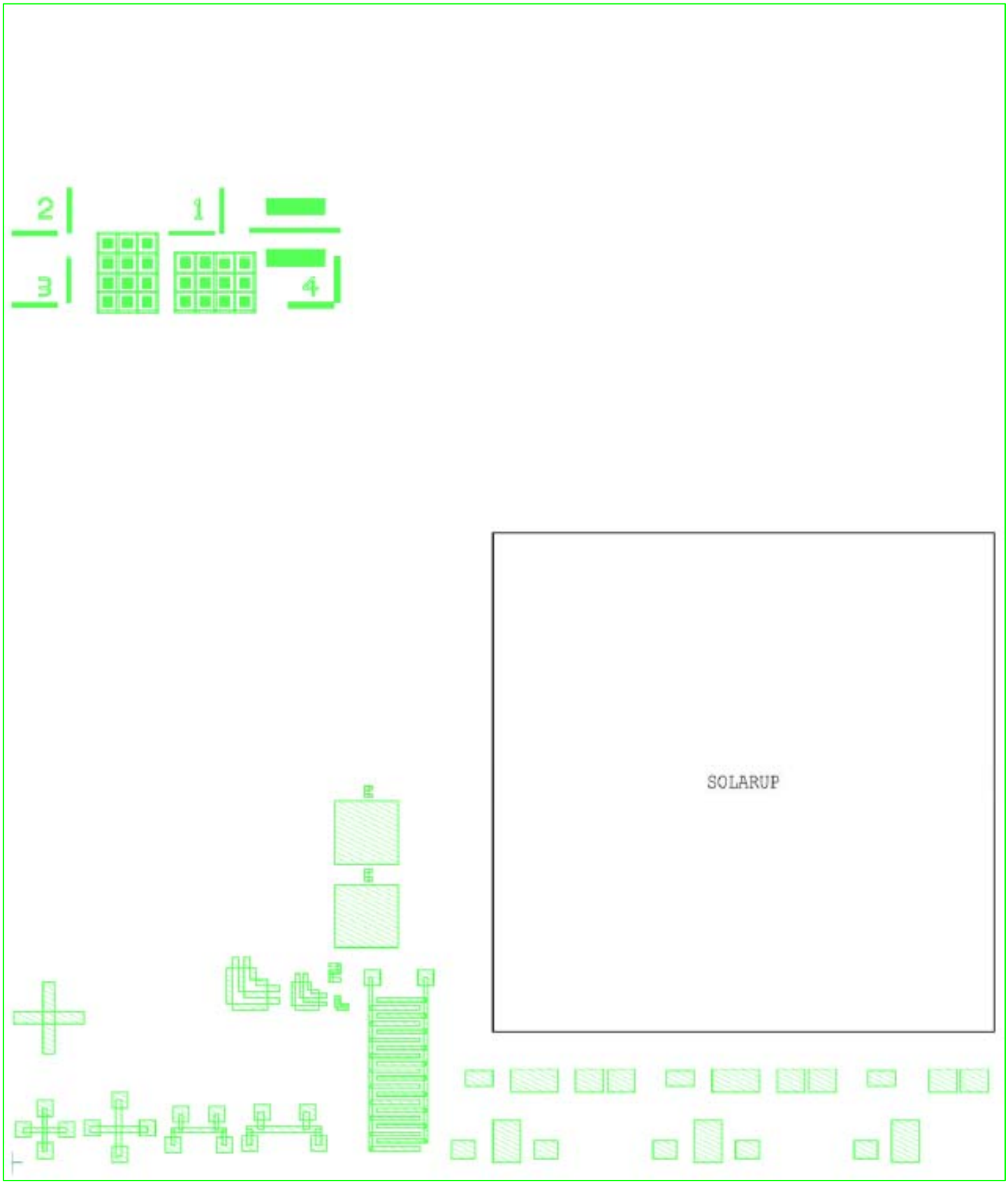


Figure 4 CONT mask (level 3)

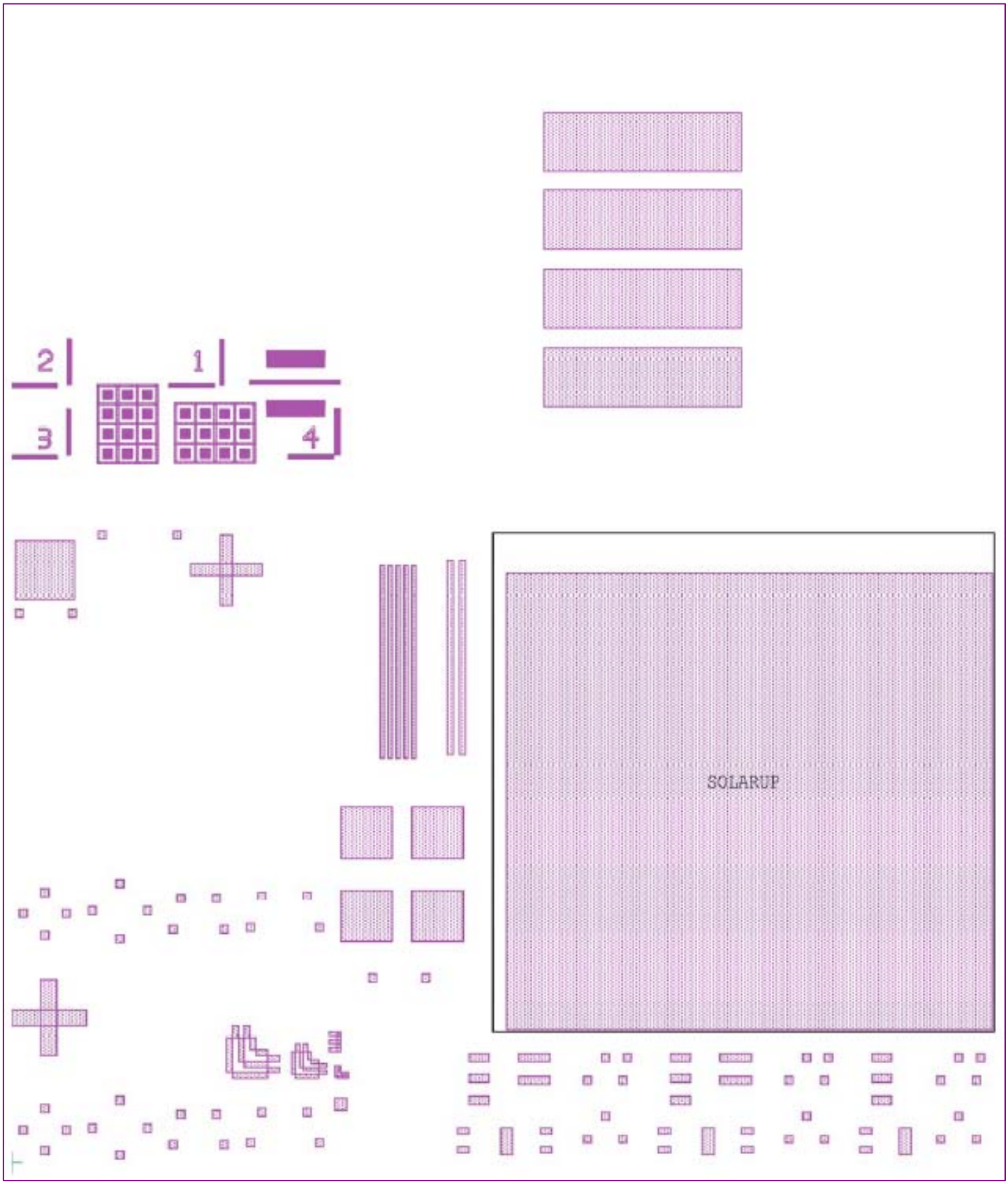


Figure 5 METL mask (level 4)

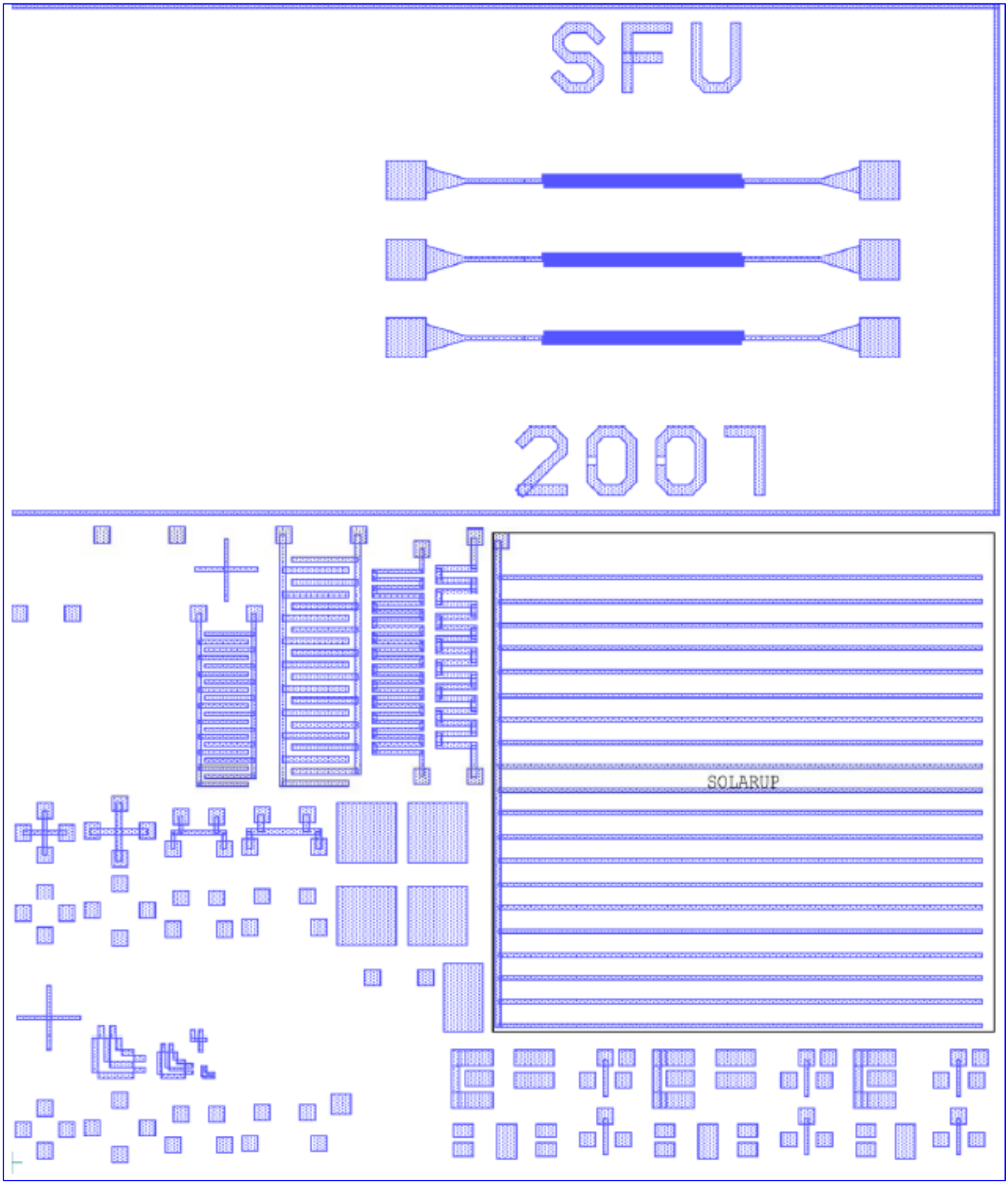
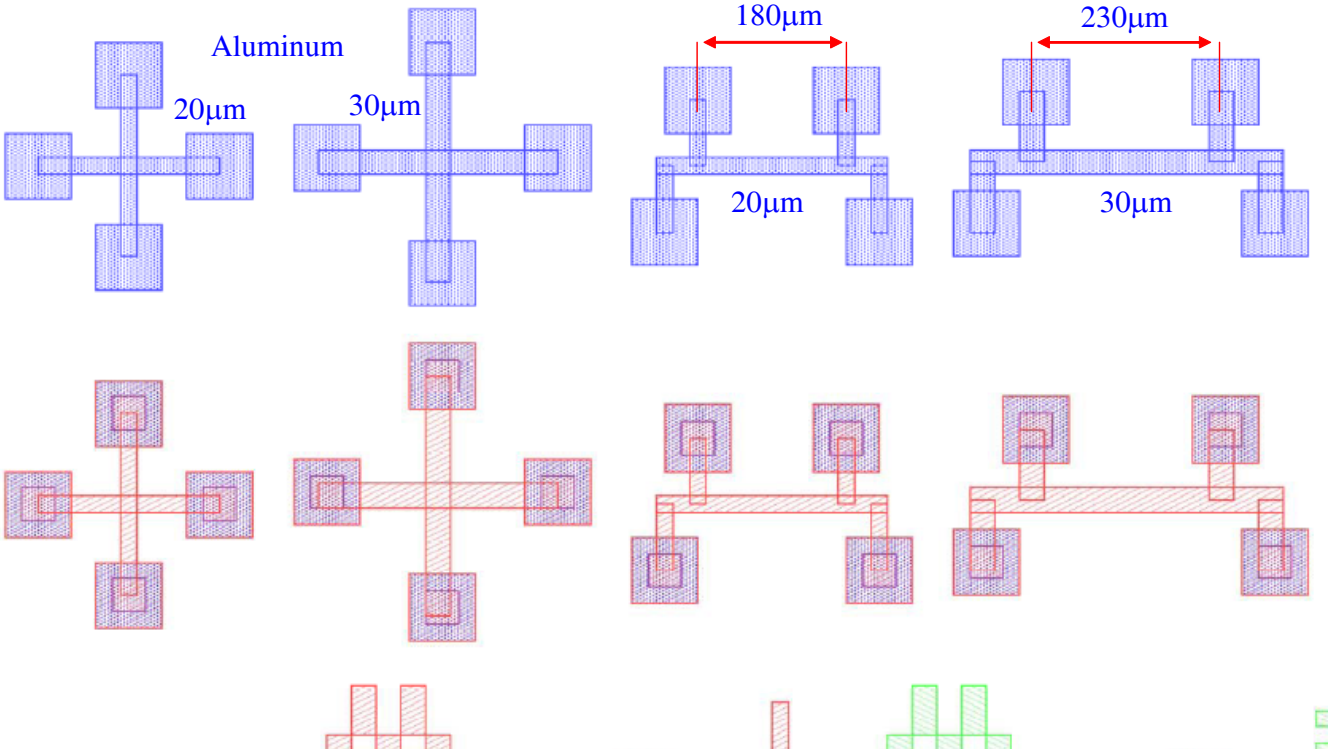


Figure 6 Van de Pauw & 4-Point resistance test structures



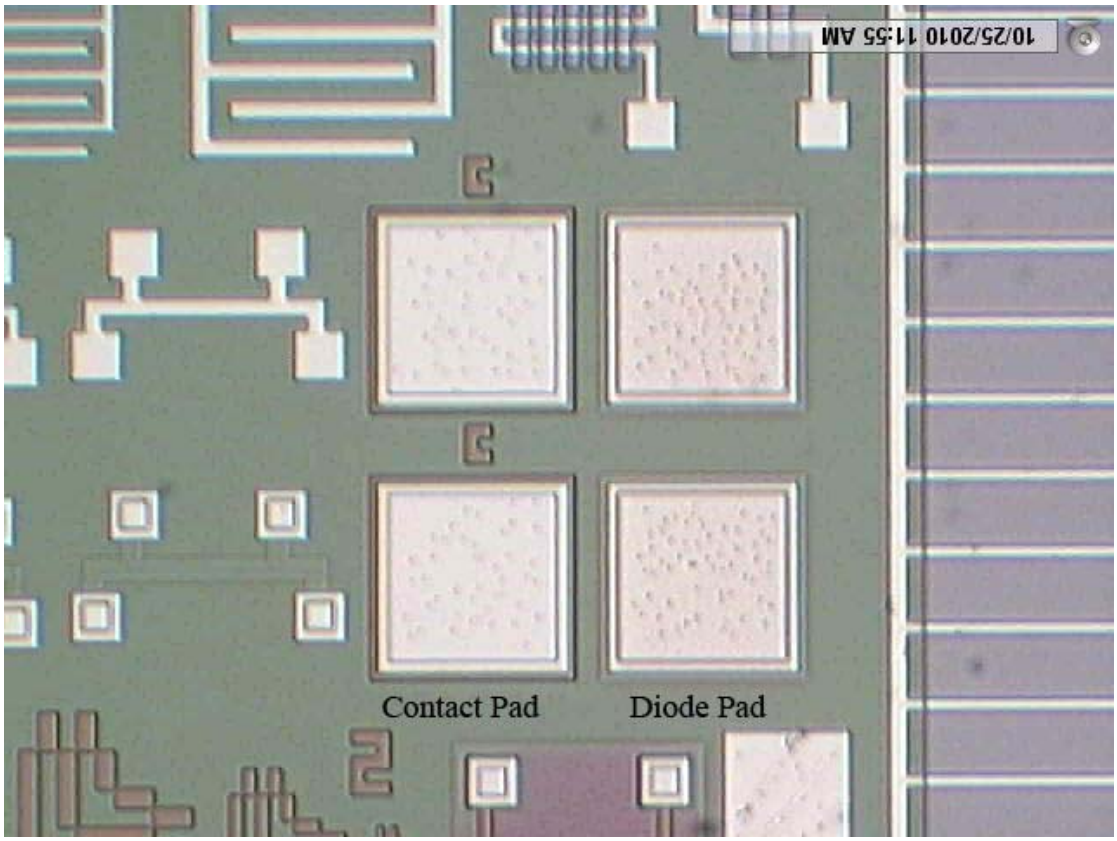


Figure 7: Contact cuts and diode pads

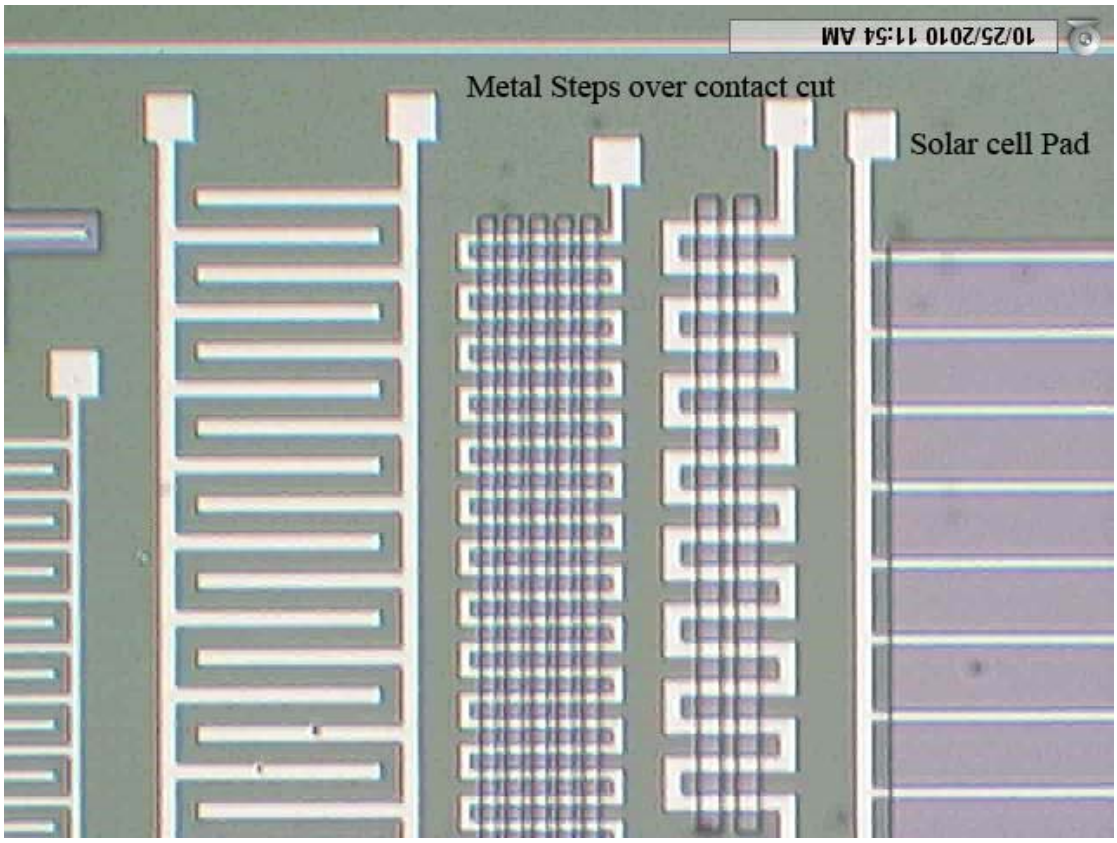


Figure 8: Metal Steps over contact cuts, and solar cell probe pad

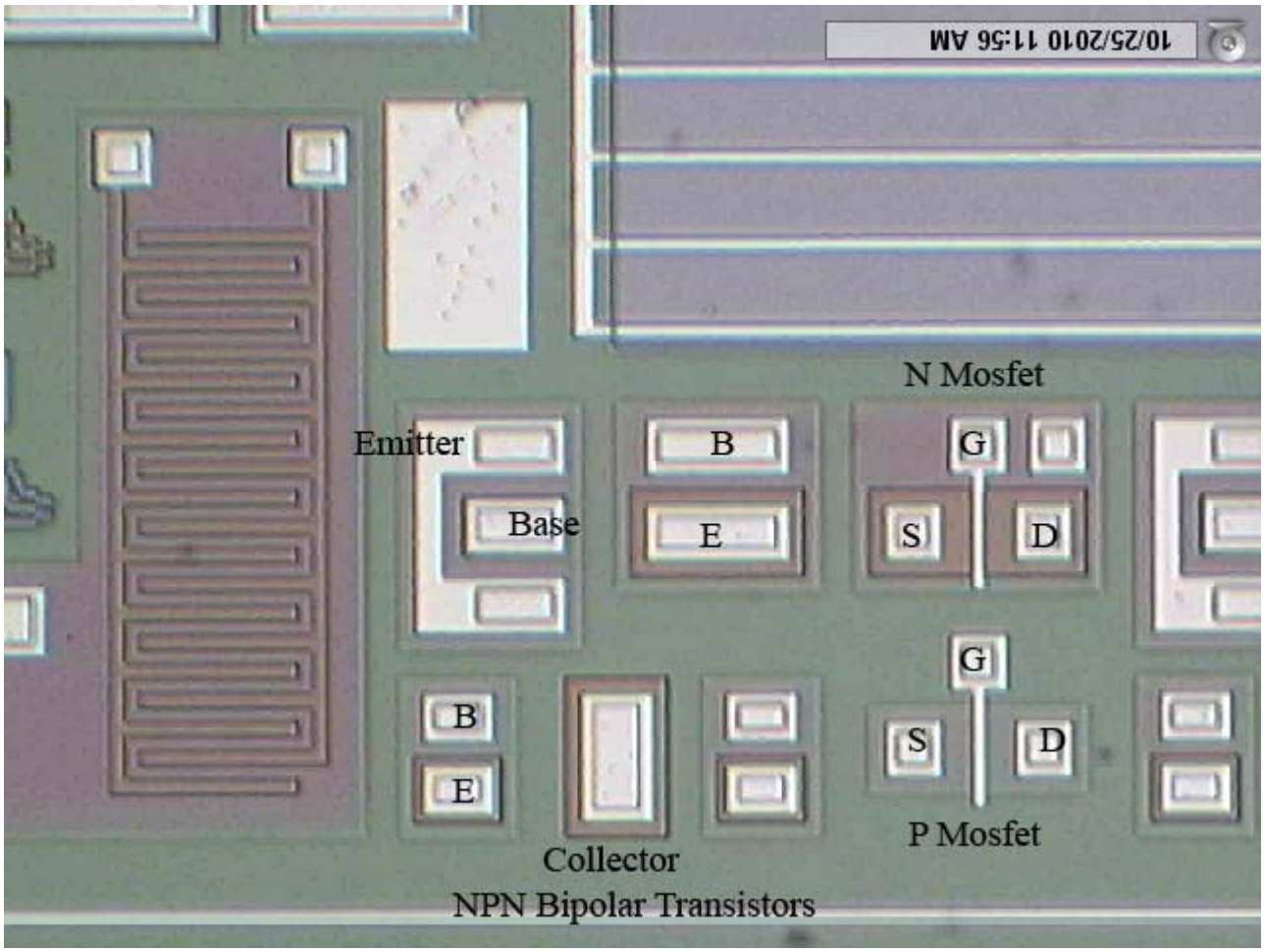


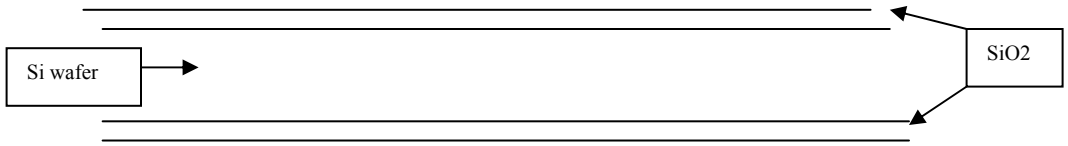
Figure 9: NPN Bipolar, N Mosfet and P Mosfet pads

Appendix A

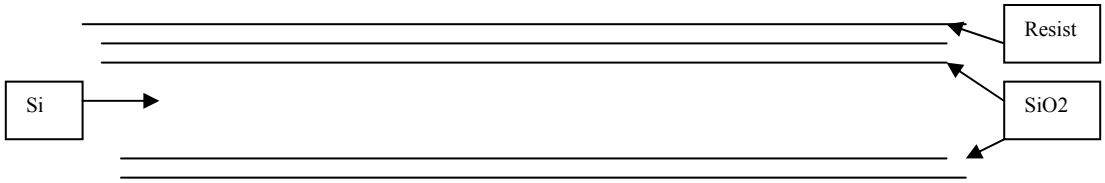
ENSC 495: Process description: (cross sectional sketches are schematic only; they are not to scale and do not show slopes, etc.)

1. RCA clean new, bare wafers. We will use an N type, phosphorous doped, <100>, test grade, 100 mm wafer. It is about 500 micrometers thick, is polished on one side, and has one major flat and one minor flat separated by 180 degrees. Its bulk resistivity is about 1 to 10 ohm-cm. We will perform a 4 mask process on it to form resistors, test structures, diodes, solar cells and transistors.

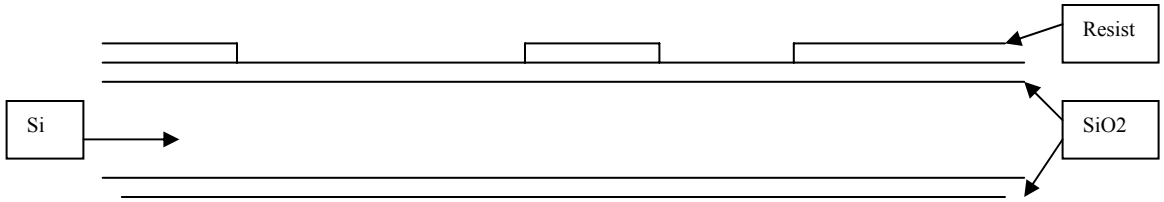
2. Grow a thermal field oxide (in steam) on the wafer to sufficient thickness to act as a barrier for subsequent boron doping operation. This oxide is about 400 to 450 nanometers thick (4000 to 4500 A). It grows evenly all over the wafer.



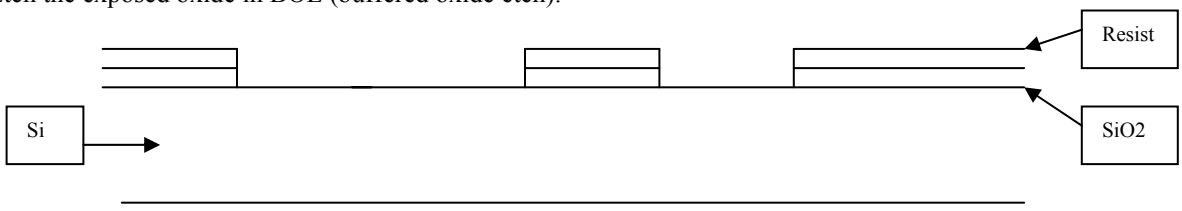
3. Spin photoresist onto front (polished) side of wafer and soft bake. You can also protect back side of wafer with resist if you want to keep the oxide there. This step is Photo 1 and opens vias (holes) in the oxide where we want to place boron (P type) doping.



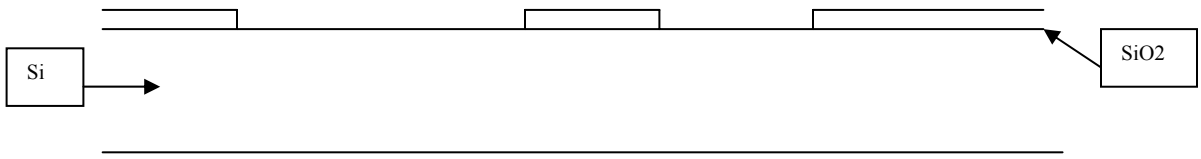
4. Expose, develop and hard bake resist. Use a dark field mask.



5. Etch the exposed oxide in BOE (buffered oxide etch).

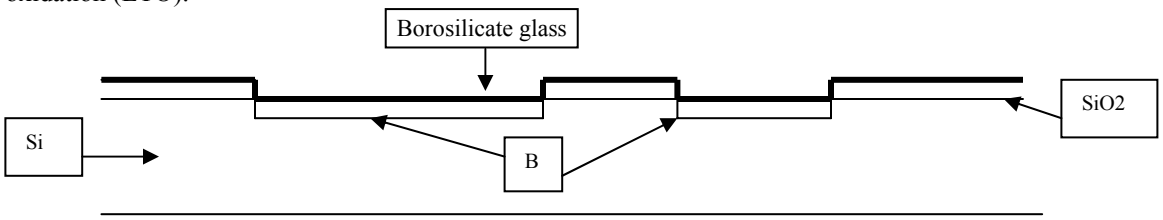


6. Strip resist in acetone.

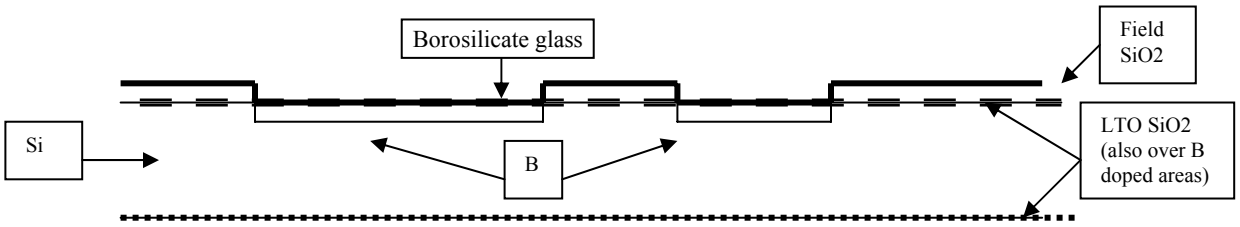


7. RCA clean.

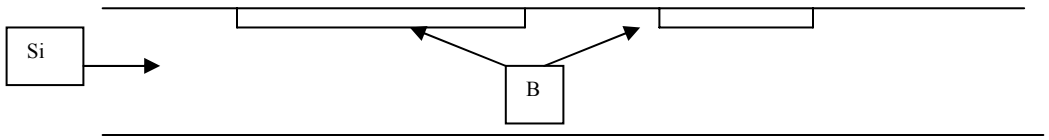
8. Using solid sources, perform boron diffusion in N2 atmosphere in furnace. Along with the boron in the silicon, some borosilicate glass will form on the surface. This can be hard to etch, so we will perform the next step, low temperature oxidation (LTO).



9. Perform LTO (low temperature oxidation in steam) on wafer in furnace. This forms a thin, pure oxide that is more easily etched than the boron enriched field oxide or the borosilicate glass. This should help to remove the oxide and glass in subsequent etching. Note that the LTO oxide forms under the original field oxide and borosilicate glass. It will not be as thick in the boron doped areas as in areas where it can access clean silicon.

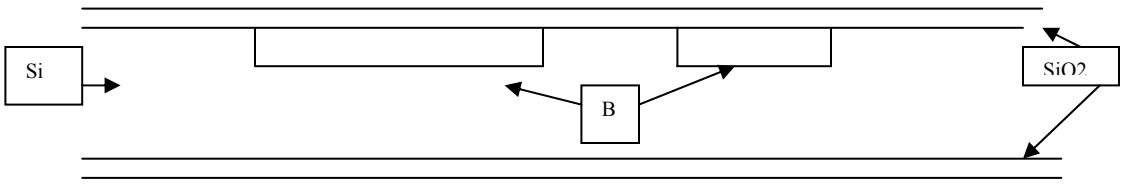


10. Strip the wafer clean of all oxide in BOE. Patterns that were previously etched and doped will still be visible in the silicon.

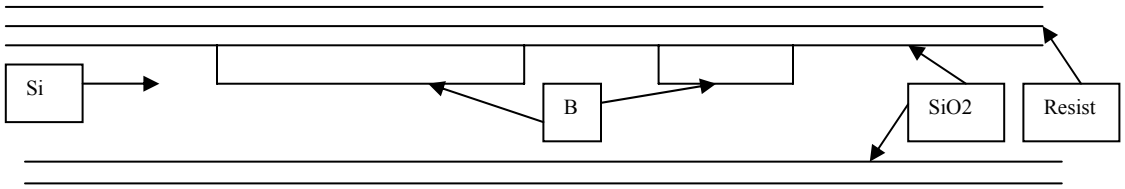


11. RCA clean.

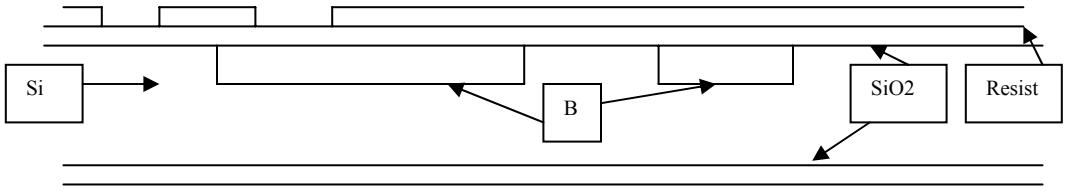
12. Perform drive-in and wet oxidation in the furnace. The boron will move slightly sideways and will be forced farther down into the wafer. Thermal oxide is grown over the whole wafer. Note that it is slightly thinner over the boron doped areas. This oxide is our diffusion stop for phosphorous diffusion. Because it will not be stripped, it is also our insulator for subsequent steps.



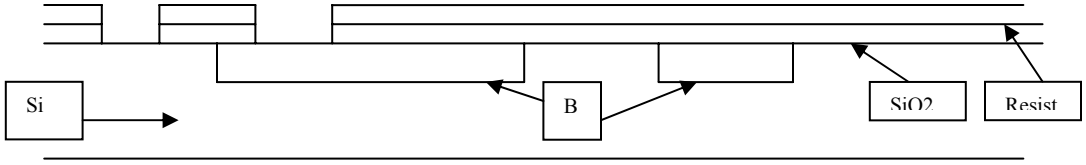
13. Spin photoresist onto front (polished) side of wafer and soft bake. You can also protect back side of wafer with resist if you want to keep the oxide there. This step is Photo 2, and opens vias in the resist where we want to place phosphorous (N type) doping. Some phosphorous will be placed in previously formed boron P wells and some in the silicon to form N++ areas for silicon substrate contact.



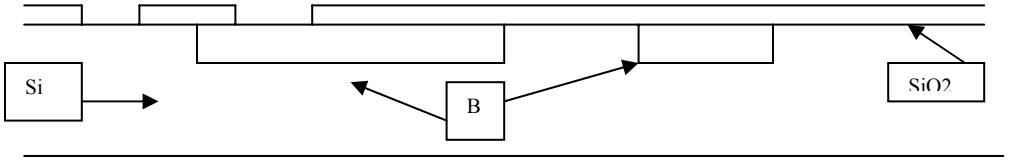
14. Expose, develop and hard bake resist. Use a dark field mask.



15. Etch the oxide in BOE (buffered oxide etch).

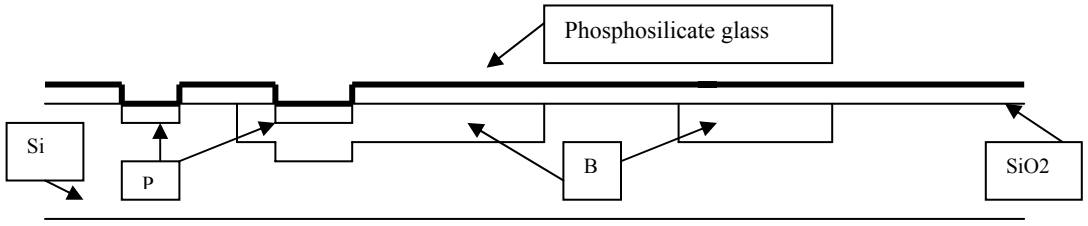


16. Strip resist in acetone.

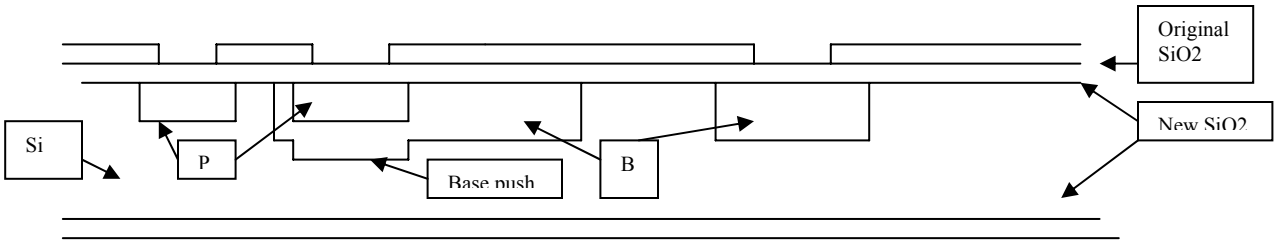


17. RCA clean.

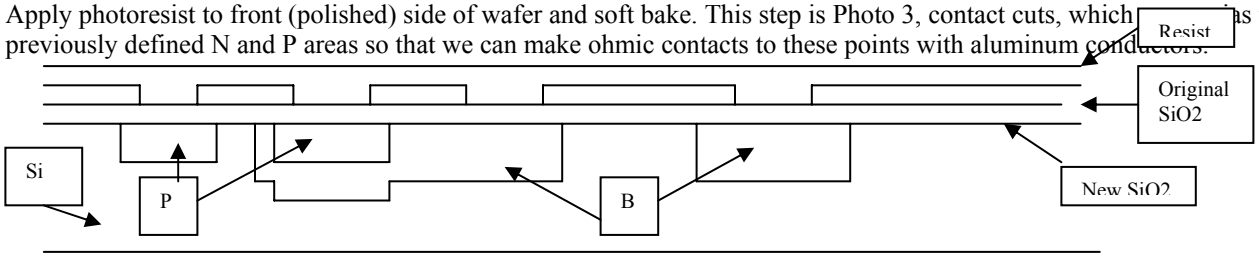
18. Using solid sources, perform phosphorous diffusion in N2 atmosphere in furnace. Along with the phosphorous deposition, some phosphosilicate glass will form on the surface. This is easy to etch; therefore we will not do LTO and strip. We might strip these parts if lab time permitted; this would permit us to grow a cleaner, thinner field oxide.



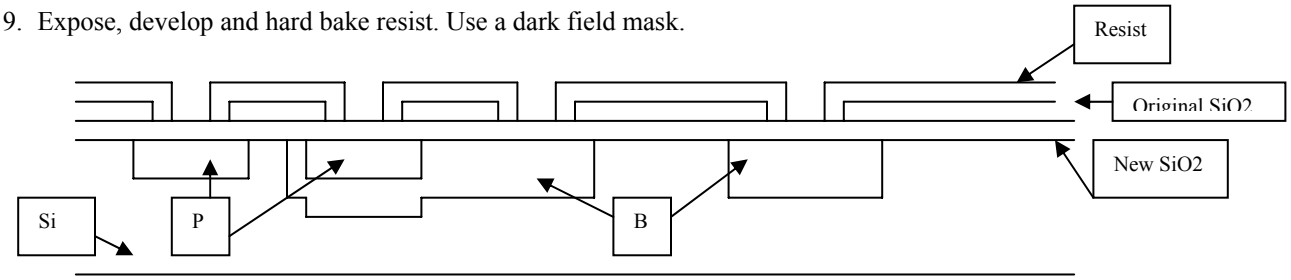
19. Go straight from diffusion furnace to oxidation/drive-in furnace. Perform drive-in and wet oxidation. The phosphorous will move slightly sideways and will be forced farther down into the wafer. The boron will also move, which it also did during the phosphorous diffusion above. The boron will move even farther where "pushed" by the phosphorous. This is called a "base push". The depth of the boron will be somewhere around 1 to 2 microns. Thermal oxide is grown over the whole wafer.



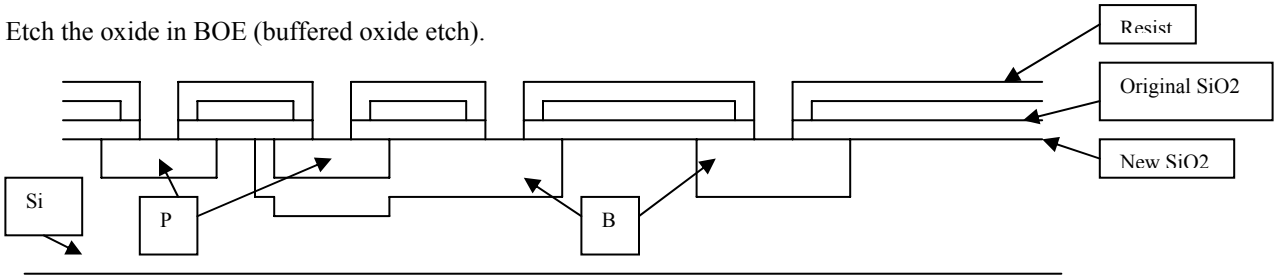
18. Apply photoresist to front (polished) side of wafer and soft bake. This step is Photo 3, contact cuts, which opens to the previously defined N and P areas so that we can make ohmic contacts to these points with aluminum conductors.



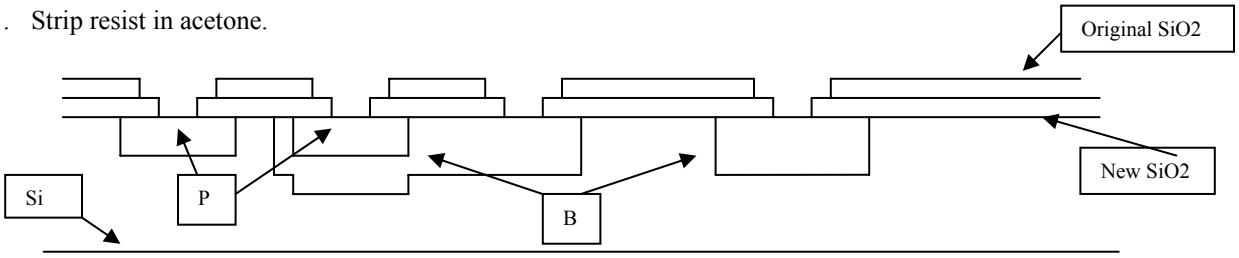
19. Expose, develop and hard bake resist. Use a dark field mask.



20. Etch the oxide in BOE (buffered oxide etch).

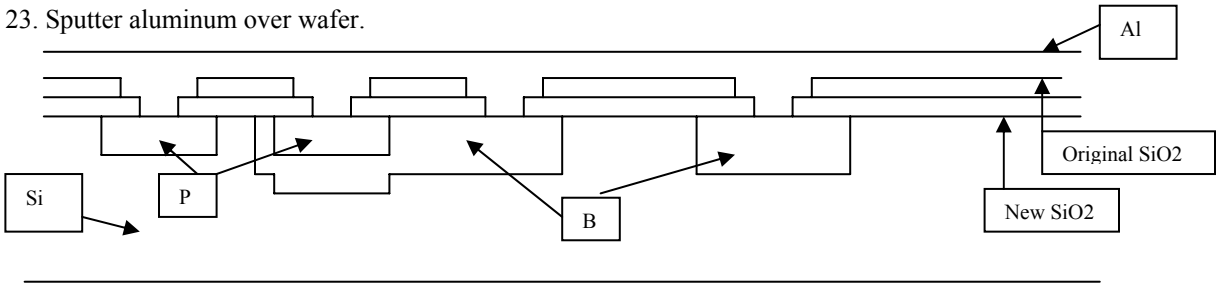


21. Strip resist in acetone.

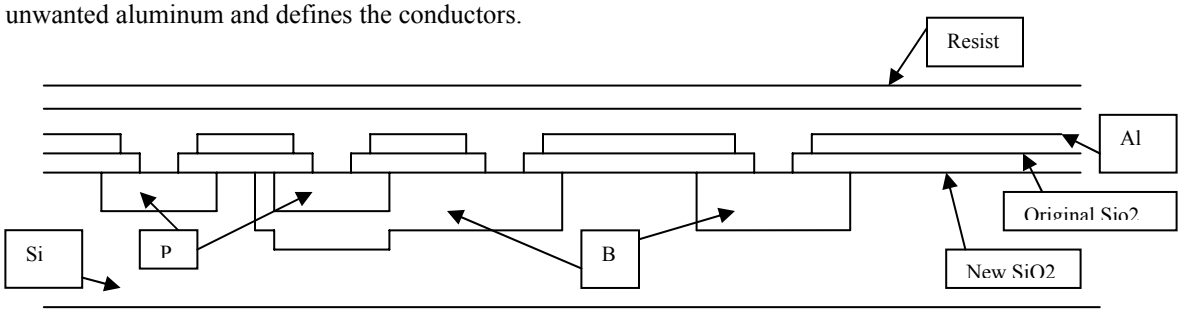


22. RCA clean

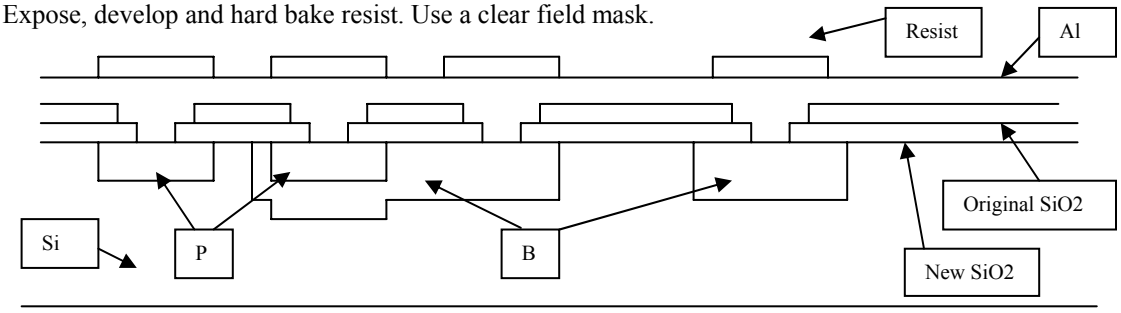
22. 23. Sputter aluminum over wafer.



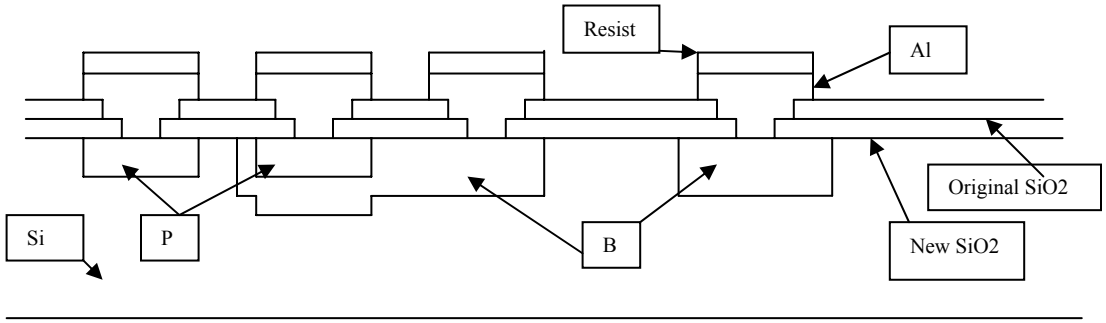
23. Spin photoresist on front (polished) side of wafer and soft bake. This step is Photo 4, aluminum definition, which removes unwanted aluminum and defines the conductors.



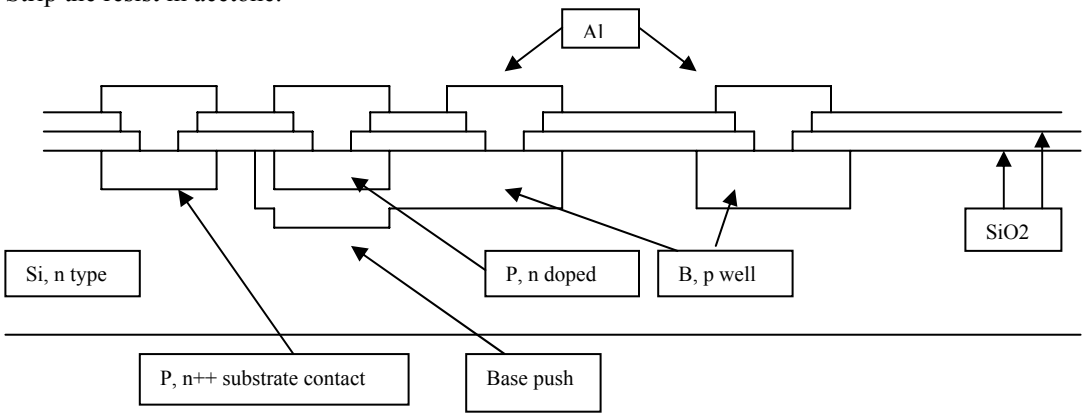
24. Expose, develop and hard bake resist. Use a clear field mask.



25. Etch the aluminum in aluminum etch.



26. Strip the resist in acetone.



27. Anneal aluminum in furnace to improve the ohmic contacts.

28. Probe test.