ENSC 895: SPECIAL TOPICS: THEORY, ANALYSIS, AND SIMULATION OF NONLINEAR CIRCUITS

FINAL PROJECT

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Study on the stability of nonlinear circuits

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Abstract: In this project, the stability of operating point of nonlinear circuits is investigated. Green’s “Γ-test” methods for identifying unstable dc operating points of nonlinear resistive networks are summarized. Moreover, $U^o$ and $U^u$ operating points are introduced and degree theory is applied to identify unstable operating points. After the general theory is applied to transistor circuits especially, three two-transistor circuits are simulated by using PSpice and MATLAB. Finally, some conclusions are given and further work and improvements are suggested.

1. Introduction

Stability is an important characteristic for dynamic systems. Checking the stability behavior of a circuit is a crucial stage in circuit design process. Electric circuit design requires accurate methods for evaluating circuit performance. Because of the enormous complexity of modern integrated circuits, computer-aided circuit analysis is essential and can provide information about circuit performance. With the development of software, it is popular for designers to use various circuit simulation software packages, such as SPICE, PSpice and OrCAD, to evaluate circuit’s performance before practical production. However, it is well known that in many circuits with multiple operating points, some of these operating points, although satisfying circuit’s equations, are never observable in real life. But, from the point of dc circuit simulation, when using an iterative algorithm to solve the nonlinear equations describing a dc circuit, the iterations still might converge to an unstable solution. It is evident that the numerical stability of the Newton-Raphson (or similar) algorithm used in PSpice is not necessarily related to the physical stability of the operating point that is being simulated. In fact, provided that the starting point is close enough, the Newton-Raphson algorithm is guaranteed to converge to any operating point of a circuit, stable or unstable. Therefore, even though, the circuit simulator finds an operating point, we still need to check whether the circuit can work at this operating point stably or not.

In the recent decades, some researchers (Green, and Willson) have made substantial progress on the subject of stability of operating points [1~7]. In this project, Green’s theory on stability of nonlinear circuits have been summarized and applied especially to two-transistor circuits. In addition, degree theory is adopted to analyze the stability of operating points. After theoretical review, we simulate three two-transistor circuits to verify the theorems. During our simulation, we first analyze the structure and equations of the circuits, and then use PSpice to find the multiple operating points. After that, we make program by using MATLAB to compute $\Gamma$. The unstable operating points are identified through observing the sign of $\Gamma$.

2. Theory on the stability of operating point

2.1 Π criterion for unstable operating point

As for a circuit, we first make a clear distinction between its equilibrium point and its
operating point. In any dynamic system described by a set of differential equations:

\[ \dot{x} = f(x) \]  

(1)

where \( x \in \mathbb{R}^n \) and \( f : \mathbb{R}^n \to \mathbb{R}^n \), the set of equilibrium (or singular) points is defined to be \( \{ x : f(x) = 0 \} \). Equilibrium point is within the context of a given dynamic system. When the dynamic system is an electric circuit, the derivative terms in (1) will necessarily arise from the presence of capacitors and inductors.

A natural starting point, when analyzing a dc circuit, is to solve for its operating point. This entails ignoring all capacitors and inductors while solving for the voltages and currents across all branches of the static elements. In such an analysis there are no state variables defined, hence the concept of an equilibrium point has no meaning. The set of dc branch voltages and currents constitutes the operating point, defined independently of any dynamic system, i.e., it is independent of the value or location of any capacitor and inductor in the circuit.

**Definition 1**: An equilibrium point \( x^* \) is said to be **stable** if, for each \( \varepsilon > 0 \), there exists \( \delta > 0 \) such that \( \| x(t) - x^* \| < \varepsilon \), for all \( t \geq t_0 \), whenever \( \| x(t_0) - x^* \| < \delta \). Otherwise, the equilibrium point is said to be **unstable**.

There are many methods to ascertain whether a given equilibrium point is stable or unstable. Two well known methods are Lyapunov’s first and second methods. Here, Lyapunov’s first method is adopted, which entails linearizing the system around the equilibrium point in question and then examining the natural frequencies there. If all natural frequencies are located in the open left half-plane then the equilibrium point is stable. If at least one natural frequency is in the open right half-plane then the equilibrium point is unstable.

**Definition 2**: A circuit’s operating point is said to be **potentially stable** if, by inserting some set of positive-valued shunt capacitors and series inductors into the circuit, the corresponding equilibrium point of the resulting dynamic circuit is stable, and if the equilibrium point of any dynamic circuit created by augmenting this dynamic circuit with an arbitrary set of shunt capacitors and series inductors, whose values are sufficiently small, is also stable.

**Definition 3**: An operating point that is not potentially stable is said to be **unstable**.

**Remark**:

1. The definition of potentially stable operating point involves first augmenting the dc circuit with a certain set of capacitors and inductors and evaluating the resulting dynamic circuit’s stability, and then augmenting the dynamic circuit with additional sets of capacitors and inductors, whose values are sufficiently small. The second augmentation is required to ensure that the definition of potential stability is robust in the sense that the circuit’s stability is not changed due to the presence of arbitrarily small stray capacitors and inductors.
2. If an *equilibrium point* is unstable this means with respect to a *particular* set of capacitors and inductors values. If an *operating point* is unstable, this means unstable for any set of positive-valued capacitors and inductors.
3. That operating point stability (like the operating point itself) is independent of the values and locations of the circuit’s capacitors and inductors (assuming, all capacitors and inductors possess only positive values).
4. The stable category requires the adjective “potentially” because, in general, a potentially stable
operating point will require the presence of appropriate shunt capacitors and/or series inductors to become a stable equilibrium point of a dynamic circuit.

Consider the linear dynamic circuit shown in Fig. 1(a).

![Fig. 1 Generalized linear circuits](image)

We presume that this comes from the linearization, around a particular operating point, of some nonlinear circuit. The linear n-port $N$ contains only positive-valued resistors. Ports 1 through $k$, called dependent-source ports, are each terminated by either a dependent current source in parallel with a positive-valued capacitor or a dependent voltage source in series with a positive-valued inductor. A controlling signal, shown in Fig. 1(a), as $x_i$ or $x_j$, is the voltage across a dependent current source or the current through a dependent voltage source. The value of a dependent source gain $a_i$ may be zero. (This is useful when a port $i$ corresponds to an open-circuit voltage or a short-circuit current that is used as a controlling signal but is not directly connected to an actual, nonzero dependent source.) Ports $k+1$ through $n$, called outside ports, are terminated with positive-valued capacitors and inductors, called outside capacitors and outside inductors, as shown.

The class of nonlinear circuits from which this linear circuit can be derived is quite general. We assume that all capacitors and inductors in the original circuit are uncoupled and have strictly monotone-increasing charge-voltage and flux-current characterizations. All static elements are assumed to be modeled by a set of resistive multiport elements $R_a$ each of which can be represented as a $n_a$-port hybrid function. In general, any circuit consisting of positive-valued resistors, diodes, transistors (BJT, JFET, MOS, GaAs, etc.) and capacitors and inductors with strictly monotone-increasing charge-voltage or flux-current characteristics, respectively, linearized at a given operating point, can be modeled by the Fig. 1(a) circuit.

We also assume that no set of dependent current (voltage) source ports forms a cut set (loop) by itself or with any set of outside capacitors (inductors). Otherwise, the circuit in Fig. 1(b) derived from Fig. 1(a) when analyzed at dc, could be ill-posed, in that it could contain cut sets of dependent current sources and/or loops of dependent voltage sources.

In addition, let us initially assume that there exist no cut sets (loops) made up exclusively of
outside capacitors (inductors). Then, the resistive $n$-port $N$ in Fig. 1(a) can be characterized at its ports by

$$
\begin{bmatrix}
Q_A & Q_B \\
Q_C & Q_D
\end{bmatrix}
\begin{bmatrix}
y_d \\
y_o
\end{bmatrix} +
\begin{bmatrix}
x_d \\
x_o
\end{bmatrix} = 0
$$

(2)

where the vector $x$ consists of the usual state variables (capacitors voltages and inductors currents), and is partitioned into $x_d$, a vector whose components are the state variables appearing at the dependent source ports, and $x_o$, a vector of state variables appearing at the outside ports. Vectors $y_d$ and $y_o$ are the respective port-variable complements of $x_d$ and $x_o$. The $n \times n$ matrix $Q$, shown partitioned in (2) has a nonnegative determinant, since $N$ contains only passive reciprocal elements.

The port constraints of the circuit in Fig. 1(a) are given by

$$
\begin{bmatrix}
y_d \\
y_o
\end{bmatrix} = K \frac{d}{dt} \begin{bmatrix}
x_d \\
x_o
\end{bmatrix} + \begin{bmatrix}
A_d & 0 \\
0 & 0
\end{bmatrix} \begin{bmatrix}
x_d \\
x_o
\end{bmatrix}
$$

(3)

where $K$ is a diagonal $n \times n$ matrix whose diagonal elements specify the positive linearized capacitor and inductor values. Matrix $A$, shown partitioned in (3), is the $n \times n$ matrix whose elements specify the appropriate dependent source gains. Notice that its entries are nonzero only in the upper left-hand $k \times k$ submatrix, since all controlling variables and dependent sources are, by assumption, confined to ports 1,..., $k$. Combining (2) and (3) we have the dynamic equations of the circuit:

$$
QK \frac{d}{dt} \begin{bmatrix}
x_d \\
x_o
\end{bmatrix} + (QA + I_n) \begin{bmatrix}
x_d \\
x_o
\end{bmatrix} = 0
$$

(4)

where $I_n$ denotes the $n \times n$ identity matrix. From this, the natural frequencies of the circuit can be found; they are the values of $s$ that satisfy

$$
\det[sQK + (QA + I_n)] = 0
$$

(5)

A constant $\Gamma$ is defined as follows:

$$
\Gamma \equiv \det(Q_A A_d + I_k)
$$

(6)

Now, we can state the following theorem:

**Theorem 1 ([3]):** Given an operating point of a circuit which can be linearized as in Fig. 1(a) with its dynamic equations written as in (4), if $\Gamma < 0$ then the operating point is unstable.

Notice that $Q_A$ and $A_d$, from (2) and (3), are associated with the dc equations of the circuit that results when $y_o$ is set to zero—that is, when all outside capacitors are replaced with open circuits and all outside inductors are replaced with short circuits. In order to use theorem 1 for any given circuit, we need only define a port for each dependent source and ignore the presence of any outside capacitors and inductors. Then we observe the sign difference in the circuit’s corresponding characteristic polynomial, which implies instability. This result is summarized in the next theorem.

**Theorem 2 ([3]):** Given the linear dynamic circuit shown in Fig. 1(a), let a capacitor be
modeled in parallel with each dependent current source and let an inductor be modeled in series with each dependent voltage source. If \( \Gamma < 0 \), then regardless of whether or not any additional outside capacitors and inductors are modeled, the resulting characteristic polynomial will have its highest and lowest order nonzero coefficients of opposite signs, making it apparent that the corresponding operating point is unstable.

### 2.2 \( U^o \) and \( U^e \) operating point

Although theorem 1 gives a sufficient condition for an operating point to be unstable, it is not a necessary condition. There might be unstable operating points where \( \Gamma > 0 \) holds. To show why this is true, consider the following characteristic equation, assumed to have been derived from an augmentation with capacitors and inductors of the Fig. 1(b) circuit:

\[
a_n s^n + a_{n-1} s^{n-1} + \ldots + a_1 s + \Gamma = a_n \prod_{k=1}^{\infty} (s - \lambda_k) = 0
\]  

(7)

where \( a_n > 0 \) and each \( \lambda_k \) is a root of the equation. Clearly, \( \Gamma / a_n = \prod_{k=1}^{\infty} (-\lambda_k) \), and in general this product can be factored into three parts, corresponding to positive real roots, negative real roots, and complex roots:

\[
\frac{\Gamma}{a_n} = \prod_{r=1}^{R} \alpha_r \cdot \prod_{l=1}^{L} \alpha_l \cdot \prod_{c=1}^{C} (\alpha_c + j\beta_c) (\alpha_c - j\beta_c) = \prod_{r=1}^{R} \alpha_r \cdot \prod_{l=1}^{L} \alpha_l \cdot \prod_{c=1}^{C} (\alpha_c^2 + \beta_c^2)
\]  

(8)

Here we assume that there are \( R \) positive real roots, implying that each \( \alpha_r \) is negative; \( L \) negative real roots, implying that each \( \alpha_l \) is positive; and \( C \) pairs of complex conjugate roots. Since all but the \( \alpha_r \) terms must be positive and \( a_n > 0 \), (8) implies

\[
\text{sgn} \, \Gamma = (-1)^R
\]  

(9)

which shows that \( \Gamma < 0 \) if and only if there is an odd number of positive real roots for the capacitor/inductor augmentation at issue. This leads to the following definition:

**Definition 3:** If an operating point \( O \) of a dc circuit satisfies theorem 1 and, equivalently, if every robust dynamic circuit (that is, all capacitor/inductor-augmented circuits with a sufficient number of arbitrarily small, but positive, capacitors and/or inductors included) that can be constructed around \( O \) has an odd number of natural frequencies in the open right half-plane, then \( O \in U^o \).

A circuit possesses an odd number of open right half-plane roots if and only if it possesses an odd number of positive real roots.

It is natural to question whether circuits exist which, when the dc biasing is appropriate, possess operating points having an even number of positive real natural frequencies. Such operating points would also be unstable, but they would not be identified as such by Theorem 1, since the constant term \( \Gamma \) in any corresponding characteristic polynomial would be positive. The following definition identifies such operating points.

**Definition 4:** Given an opening point \( O \) of a dc circuit, if every robust dynamic circuit that can be constructed around \( O \) has an even nonzero number of natural frequencies in the open right half-plane, then \( O \in U^e \).
The following theorem proves that $U^e$ operating points do indeed exist.

**Theorem 3** ([5], [8]): Let two dc circuits, one biased at operating point $O_1$ and the other biased at operating point $O_2$, be connected at at most one node when all dc sources are set to zero. Define $O_1 \cup O_2$ as the operating point of the overall dc circuit. If $O_1 \in U^o$ and $O_2 \in U^o$, then $O_1 \cup O_2 \in U^e$.

### 2.3 Application of degree theory to stability of nonlinear circuits

We first define a mapping $F : \mathbb{R}^n \to \mathbb{R}^n$ and let it be a $C^1$ mapping. Let $D$ be a bounded, open subset of $\mathbb{R}^n$. $\partial D$ denotes the boundary of $D$, and $\overline{D}$ denotes the closure of $D$; thus $\overline{D} = D \cup \partial D$. $C(\overline{D})$ refers to the space of all continuous functions defined on $\overline{D}$ that map into $\mathbb{R}^n$. Finally, let $x^* \in \mathbb{R}^n$ denotes a singular point of $F$; i.e., $F(x^*) = 0$.

**Definition 5:** The index of an isolated singular point $x^*$ of $F(x)$, written $I_F(x^*)$, is given by:

$$I_F(x^*) = \begin{cases} +1, & \text{if } \frac{DF}{Dt}(x^*) > 0 \\ 0, & \text{if } \frac{DF}{Dt}(x^*) = 0 \\ -1, & \text{if } \frac{DF}{Dt}(x^*) < 0 \end{cases}$$  \hspace{1cm} (10)

**Definition 6:** The degree of $F$ with respect to $D$, written $d(F; D)$, is given by

$$d(F; D) = \sum_{x^* \in D} I_F(x^*)$$  \hspace{1cm} (11)

**Definition 7:** A singular point $x^*$ of $F$ is said to be structurally stable if, for any $\varepsilon > 0$, there exists $\delta > 0$ such that there is at least one singular point in the set $\{x : \|x - x^*\| < \varepsilon\}$ for any $F_{\delta} \in C(\overline{D})$ with $\|F_{\delta} - F\| < \delta$.

**Property 1:** An isolated singular point is structurally stable if and only if its index is nonzero.

**Property 2:** If $h(x, \lambda) \neq 0$ for all $x \in \partial D$ and for all $\lambda \in [0, 1]$, then $d(h; D)$ is constant for all $\lambda \in [0, 1]$. In particular, $d(F_1; D) = d(F_2; D)$.

We now consider the general nonlinear circuit shown in Fig. 2(a), partitioned into its linear part $L$, made up of positive-valued linear resistors and dc independent sources, and its nonlinear part $NL$, made up of a set of passive nonlinear static elements such as transistors and diodes.

We assume that each nonlinear element can be modeled by a voltage-controlled multiport, characterized by a $C^1$ mapping from its set of port voltages to its set of port currents. Bipolar junction transistors, diodes, MOSFETs and JFETs can be modeled in this way. Thus the port equations for the nonlinear $n$-port $NL$ can be written as

$$i = B(v)$$  \hspace{1cm} (12)

where the components of $i$ and $v$ are the port currents and voltages, respectively, of $L$ and $NL$, and $B(v) : \mathbb{R}^n \to \mathbb{R}^n$. The passivity assumption on the nonlinear elements is of course true for real transistors and diodes, and it imposes some additional constraints on their model parameters.
We also make a topological assumption: we assume that there exist neither cut sets nor loops consisting exclusively of the ports defined for the nonlinear elements. This is consistent with physical circuits in that there are always small series resistances and small parallel conductances associated with any circuit element. On the basis of this topological assumption, the linear $n$-port $L$ can be characterized by

$$i + Gv - b = 0$$  \hfill (13)

Matrix $G$ is the positive definite conductance matrix of $L$, the constant vector $b$ accounts for the presence of the independent sources in $L$, and $i$ and $v$ are defined as before. Combining (12) and (13) we construct the circuit map $N(v): R^n \rightarrow R^n$ whose singular points are the operating points of the Fig. 2(a) circuit:
The Jacobian matrix of $N$ is

$$\frac{\partial N}{\partial v} = \frac{\partial B}{\partial v} + G$$

(15)

By assumption, the nonlinear n-port $NL$ can be modeled, after linearization around an operating point, by a set of voltage-controlled dependent current sources and positive-valued conductances connected across the ports, as shown in Fig. 2(b) The conductance matrix describing this linear active n-port $NL'$ is given by

$$\frac{\partial B}{\partial v} = A + D$$

(16)

The entries of $A$ are the dependent current source coefficients and $D$ is the conductance matrix of the n-port that results when all dependent source gains in $NL'$ are set to zero. Substituting (16) into (15), we have:

$$\frac{\partial N}{\partial v} = A + D + G$$

(17)

By assumption, $G$ is positive definite and $D$ is positive semidefinite; hence

$$\det(D + G) > 0$$

(18)

A representation of the Fig. 2(a) circuit, linearized at a particular operating point, is shown in Fig. 2(c). In the representation, the set of resistors and the set of dependent current sources originally in $NL'$ have been separated. The linear n-port $L'$ is derived from setting all independent sources in $L'$ to zero. The passive part of the Fig. 2(c) circuit consists of $L'$ augmented as shown with the resistors originally in $NL'$. The active part consists of the set of dependent current sources originally in $NL'$.

The passive part can be characterized by

$$\tilde{v} + (G + D)^{-1}\tilde{i} = 0$$

(19)

where $G$ and $D$ are defined as before. The port constraints due to the active part are given by

$$\tilde{i} = A\tilde{v}$$

(20)

The Fig. 2(c) circuit is of the same form as the Fig. 1(b) circuit. We can therefore write

$$\Gamma = \det[(G + D)^{-1}A + I_n]$$

(21)

using (18), we have

$$\text{sgn} \Gamma = \text{sgn} [\det(A + G + D)] = \text{sgn} \left[\det \left( \frac{\partial N}{\partial v} \right) \right]$$

(22)

Therefore, by theorem 1, definition 5 and (22), any isolated $U^o$ operating point of the circuit must correspond to a singular point of $N$ having index -1, and any structurally stable isolated operating point that is not $U^o$ must correspond to index +1.

Theorem 4 ([5], [8]): Let a dc circuit contain positive-valued resistors, independent sources,
and passive, voltage-controlled nonlinear elements whose ports form neither loops nor cut sets. If the circuit has a finite number of operating points, all of which are isolated, then it possesses an odd number of structurally stable operating points.

Theorem 5 ([5], [8]): If a dc circuit as specified in Theorem 3 has \( n \) structurally stable operating points, then \( (n - 1)/2 \) of them must be \( U^o \) and therefore must be unstable.

It is not necessarily true that the remaining \( (n+1)/2 \) operating points, all of which have an index -1, will be potentially stable; a \( U^e \) unstable operating point also has an index of +1.

2.4 Application to transistor circuit

In this section, we will apply Theorem 1 and degree theory to the general classes of transistor circuits.

Fig. 3 Nonlinear and linear transistor models

Fig. 3(a) shows the Ebers-Moll model of a bipolar junction transistor, modeled as a two-port. The transistor modeling assumptions are as follows. The junction diode currents are specified by \( f_1(v_1) \) and \( f_2(v_2) \), strictly monotone increasing functions of the junction voltages, and the current gains \( \alpha_1 \) and \( \alpha_2 \) are contained in the half-open interval \( [0, 1) \). We will assume that \( df_1/dv_1, df_2/dv_2 > 0 \) for all \( v_1 \) and \( v_2 \). The model of the transistor, linearized at some operating point, is shown in Fig. 3(b) with the linearized diode conductances \( d_1, d_2 > 0 \).

We assume that the linear circuit in Fig. 4 contains, for \( k \) even, \( k/2 \) transistors. We can write a set of equations for the linear \( k \)-port \( N' \) in the form

\[
Qi' + v = 0
\]

(23)

The relation between the vectors \( i' \) and \( i \) is

\[
i' = i - Dv
\]

(24)

where \( D = \text{diag}[d_1, \ldots d_k] \)

The equation describing \( N \) is

\[
Qi + Pv = 0
\]

(25)

where \( P \equiv (I_k - QD) \). The port-variable constraints imposed by the linearized transistors are given by

\[
i = TDv
\]

(26)

where \( T \) is defined to be a block diagonal matrix consisting of a set of 2×2 submatrices of the form
Combining (25) and (26), we have

\[(QTD + P)v = 0\]  

(27)

In order to apply the result presented here to results in theorem 1, we show some equivalence. First, we see that (23) is in the same form as \(Q_dv_d + x_d = 0\) in (2), provided all dependent sources are voltage-controlled current sources. Second, \(A_A\), as defined in (4), is given here by

\[A_A = i' / v = (i - Dv) / v = (TDv - Dv) / v = (T - I_k)D\]  

(28)

Thus, the quantity \((Q_dA_A + I_k)\) from theorem 1 is now given by

\[Q(T - I_k)D + I_k = QTD + (I_k - QD) = QTD + P\]  

(29)

Therefore, for transistor circuits:

\[\Gamma = \det(QTD + P)\]  

(30)

For transistor circuits which can be written as \(PV + QI + b = 0\) where \(i = TF(v)\), so, \(PV + QTF(v) + b = 0\), we construct the circuit map \(N(v) : R^d \rightarrow R^d\) whose singular points are the operating points of the Fig. 4 circuit:

\[N(v) = QTF(v) + PV + b\]  

(31)

The Jacobian matrix of \(N\) is

\[\frac{\partial N}{\partial v} = QTD + P\]  

(32)
\[ \text{sgn} \left[ \det \left( \frac{\partial N}{\partial v} \right) \right] = \text{sgn} \left[ \det \left( QTD + P \right) \right] \] (33)

So, the identification of unstable operating points for transistor circuits by using degree theory is identical to that using \( \Gamma \) criterion.

Especially, for two-transistor circuit, we have following theorems:

**Theorem 6** ([1], [3]): If a two-transistor circuit has three operating points, the middle one is unstable, while the outside two are potential stable.

**Theorem 7** ([1], [3]): If a two-transistor circuit has two operating points, one must be unstable and the other potentially stable.

**Theorem 8** ([1], [3]): If a two-transistor circuit has one operating points, it must be potentially stable.

3. Simulations

3.1 Example 1 Flip-flop circuit

The first example we are studying is flip-flop circuit which is shown is Fig. 5.

![Fig. 5 Flip-flop circuit](image)

**Step 1**: Analyze the circuit

Since there is feedback structure in the flip-flop circuit, it might have multiple operating points. Write circuit equations in the form

\[ i + Gv + c = 0 \]

where

\[ G = \begin{bmatrix}
G_{b1} + G_{b2} + G_{c1} & -(G_{c1} + G_{b2}) & -(G_{b1} + G_{b2}) & G_{b1} \\
-(G_{c1} + G_{b2}) & G_{c1} + G_{b2} & G_{b2} & 0 \\
-(G_{b1} + G_{b2}) & G_{b2} & G_{b1} + G_{b2} + G_{c2} & -(G_{c2} + G_{b1}) \\
G_{b1} & 0 & -(G_{c2} + G_{b1}) & G_{c2} + G_{b1}
\end{bmatrix} \quad \text{and} \quad c = \begin{bmatrix} G_{c1}E \\ -G_{c1}E \\ G_{c2}E \\ -G_{c2}E \end{bmatrix} \]

\( G_{b1} = 1/R_{b1}, \ G_{b2} = 1/R_{b2}, \ G_{c1} = 1/R_{c1}, \ \text{and} \ G_{c2} = 1/R_{c2}. \)

We now connect a dc voltage source \( V_s \) between the two bases and form an auxiliary circuit as
shown in Fig. 6. This destroys the feedback structure the original circuit has had, which implies that the Fig. 6 circuit can possess only one operating point for each value of $V_s$. We can draw a graph of port characteristic: $I_s$ versus $V_s$ shown in Fig. 7. The operating point of the original Fig. 5 circuit are given by the intersections of the curve in Fig. 7 with the $V_s$ axis; i.e., the points where $I_s = 0$. It is shown that such a curve can intersect the $V_s$ axis no more than three times. Hence, a two-transistor circuit can possess no more than three operating points.

![Fig. 6 Auxiliary circuit of flip-flop circuit](image1)

![Fig. 7 v-i characteristics of auxiliary circuit](image2)
Step 2: Search operating points

We use PSpice to simulate original flip-flop circuit. Without any specification, PSpice sets initial values of all node voltage be zero. The first operating point OP1 is listed as follows and plotted in Fig. 9.

\[
\begin{align*}
\text{OP1: } & V_1 = 5.0000\, \text{V}, \quad V_2 = 0.9631\, \text{V}, \quad V_3 = 0.9631\, \text{V}, \quad V_4 = 0.7029\, \text{V}, \quad V_5 = 0.7029\, \text{V}.
\end{align*}
\]

Based on Fig. 8, we set the initial values of each node voltage as \( V_1(0) = 0\, \text{V}, \quad V_2(0) = 4.7\, \text{V}, \quad V_3(0) = 0.1\, \text{V}, \quad V_4(0) = 0\, \text{V}, \quad V_5(0) = 0.75\, \text{V} \) and get the second operating point OP2 shown in Fig.
10.

OP2: $V_1 = 5.0000V, V_2 = 4.6105V, V_3 = 0.0861V, V_4 = 0.0861V, V_5 = 0.7156V.$

Similarly, we set $V_1(0) = 0V, V_2(0) = 0.1V, V_3(0) = 4.7V, V_4(0) = 0.75V, V_5(0) = 0V,$ and get the third operating point OP3 shown in Fig 11.

OP3: $V_1 = 5.0000V, V_2 = 0.0861V, V_3 = 4.6105V, V_4 = 0.7156V, V_5 = 0.0861V.$

**Fig. 10 The second operating point of example 1**

**Fig. 11 The third operating point of example 1**

**Step 3: Identify unstable operating point**

In order to compute $\Gamma$, we need to use parameters of transistors which can be found in PSpice.

For Q1 and Q2, the default maximum forward beta $\beta_f = 416.4$, and default maximum reserve
beta \beta_r = 0.7371.

So, \alpha_r and \alpha_f in matrix T are \alpha_r = \beta_r / (1 + \beta_r) and \alpha_f = \beta_f / (1 + \beta_f).

In \( f(v_i) = m_i (\exp(nv_i) - 1) \), \( m_1 \) and \( m_3 \) are reserve saturation current of the base-emitter junction. \( m_2 \) and \( m_4 \) are reserve saturation current of the base-collector junction. We have following relations [11]: \( \alpha_i m_i = \alpha_{i+1} m_{i+1} = I_s. \) \( (i = 1, 3). \)

where \( I_s \) is the p-n saturation current. Here, for two transistors \( I_{s1} = I_{s2} = 6.734e-15. \)

\( n \) is a constant at a certain temperature. \( n = q / kT \), where \( q \) is electron charge, \( k \) is Boltzmann’s constant and \( T \) is temperature (in Kelvin).

Notice: For PNP transistors, \( m, n > 0 \), and for NPN transistors, \( m, n < 0 \).

D is a diagonal matrix with elements \( d_1 \sim d_4. \)

\[ d_i = m_i n \exp(nv_i) \quad (i = 1, 2, 3, 4) \]

We use MATLAB to compute \( \Gamma \) of each operating point and get the results as follows.

OP1: \( \Gamma_1 = \det(QTD + P) = -2.8077e-10 < 0 \)

OP2: \( \Gamma_2 = \det(QTD + P) = 4.0475e-10 > 0 \)

OP3: \( \Gamma_3 = \det(QTD + P) = 4.0475e-10 > 0 \)

Therefore, the middle operating point OP1 must unstable and based on theorem 6, two outside operating points OP2 and OP3 are both potentially stable. This result is consistent with above theorems.

3.2 Example 2 Circuit in assignment

\[ \begin{array}{c}
1 \\
& \theta_R 110 \\
& \theta_E 110 \\
& \theta_{T_1} \\
& \theta_{T_2} \\
& \theta_{21.5} \\
& \theta_{R_3} \\
& \theta_{T_1} \\
& \theta_{3} \\
& \theta_{0} \\
\end{array} \]

Fig. 12 The second example circuit

Step 1: Analyze the circuit

The circuit shown in Fig. 12 has no feedback structure when driven by voltage source. While, when the circuit is driven by a current source, there exists a feedback structure, which means the circuit probably has multiple operating points when it is driven by a current source.

We first bias the circuit with a voltage source sweeping from 0V to 5V (Fig. 13). The \( v-i \) characteristic and each node voltage are shown in Fig. 14.
From the v-i characteristic, we find that when the circuit is driven by a current source, it may exist three operating points. (i.e. $I = 200mA$). We write circuit equations in the form:

$$Pv + Qi = c$$

where
\[ P = \begin{pmatrix} -G_2 & 0 & 0 & 0 \\ 1 & -1 & -1 & 0 \\ 0 & 0 & 0 & G_3 \\ G_2 & G_i & 0 & G_i \end{pmatrix}, \quad Q = \begin{pmatrix} -1 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 1 \\ 1 & 1 & 0 & 0 \end{pmatrix} \quad \text{and} \quad c = \begin{pmatrix} I_s \\ 0 \\ 0 \\ 0 \end{pmatrix} \]

where \( G_1 = 1/R_1, \ G_2 = 1/R_2, \) and \( G_3 = 1/R_3. \)

**Step 2: Search operating points**

Without setting any node voltage initial values, we get the first operating point shown in Fig. 15.

\( \text{OP1: } V_1 = 1.555V, V_2 = 765.95mV, V_3 = 848.14mV. \)

Based on Fig. 14, we set the initial values of each node voltage as \( V_1(0) = 5V, V_2(0) = 0.8V, \) and \( V_3(0) = 0.2V, \) and get the second operating point OP2 shown in Fig. 16.

\( \text{OP2: } V_1 = 3.999V, V_2 = 1.015V, V_3 = 281.7mV. \)

Similarly, we set the initial value of each node voltage as \( V_1(0) = 1V, V_2(0) = 0.4V, V_3(0) = 0.8V. \)

We get the third operating point OP3 shown in Fig. 17.

\( \text{OP3: } V_1 = 924.15mV, V_2 = 462.07mV, V_3 = 864.42mV. \)

![Fig. 15 The first operating point of example 2](image-url)
Step 3: Identify unstable operating point

The parameters in transistors are identical to those in example 1. The procedure is the same with that in example 1.

For Q1 and Q2, the default maximum forward beta $\beta_f = 416.4$, and default maximum reserve beta $\beta_r = 0.7371$. 
So, $\alpha_r$ and $\alpha_f$ in matrix $T$ are $\alpha_r = \beta_r/(1+\beta_r)$ and $\alpha_f = \beta_f/(1+\beta_f)$.

In $f(v_i) = m_i(\exp(nv_i)-1)$, $m_1$ and $m_3$ are reserve saturation current of the base-emitter junction. $m_2$ and $m_4$ are reserve saturation current of the base-collector junction. We have following relations: $\alpha_r m_i = \alpha_r (m_{i+1} = I_s, (i = 1, 3)$.

where $I_s$ is the $p-n$ saturation current. Here, for two transistors $I_{s1} = I_{s2} = 6.734e-15$.

$n$ is a constant at a certain temperature. $n = q/kT$, where $q$ is electron charge, $k$ is Boltzmann’s constant and $T$ is temperature (in Kelvin).

Notice: For PNP transistor, $m, n > 0$, and for NPN transistor $m, n < 0$.

$D$ is a diagonal matrix with elements $d_1$ to $d_4$.

$$d_i = m_i n \exp(nv_i) \quad (i = 1, 2, 3, 4)$$

We still use MATLAB to compute $\Gamma$ of each operating point and get the results as follows:

- **OP1**: $\Gamma_1 = \det(QTD+P) = -0.7546 < 0$
- **OP2**: $\Gamma_2 = \det(QTD+P) = 1.2171e+3 > 0$
- **OP3**: $\Gamma_3 = \det(QTD+P) = 0.0734 > 0$

So, the conclusion is that the middle operating point OP1 is unstable and two outside operating points OP2 and OP3 are both potentially stable.

### 3.3 Example 3: Chua’s Circuit

**Step 1: Analyze the circuit**

The configuration of this circuit shows there are feedback structures when the circuit is driven either by voltage source or current source. Here, we first drive the circuit with a current source to form an auxiliary circuit shown in Fig. 19. The current source sweeps from 0 to 20mA.
We get the \( v-i \) characteristic of the current source and variation of voltages at each node which are shown in Fig. 20.

From Fig. 20, we see there exist S-type NDR. If we drive the circuit with a voltage source (i.e. \( V_s = 12V \)), there will be three operating points. We still write circuit equations in the form:

\[
P_v + Q_i = b
\]
Step 2: Search operating points

Without setting any node voltage initial values, we get the first operating point shown in Fig. 21.

OP1: $V_1 = 12V$, $V_2 = 10.67V$, $V_3 = 11.3V$, $V_4 = 5.44V$, $V_5 = 4.758V$.

Based on Fig. 20, we set the initial values of each node voltage as: $V_1(0) = 12V$, $V_2(0) = 11V$, $V_3(0) = 11V$, $V_4(0) = 12V$ and $V_5(0) = 11V$. We get the second operating point OP2 shown in Fig. 22.

OP2: $V_1 = 12V$, $V_2 = 11.06V$, $V_3 = 11.74V$, $V_4 = 11.73V$, $V_5 = 11.02V$

Similarly, we set the initial value of each node voltage as $V_1(0) = 12V$, $V_2(0) = 12V$, $V_3(0) = 12V$, $V_4(0) = 1V$ and $V_5(0) = 1V$ and get the third operating point OP3 shown in Fig. 23.

OP3: $V_1 = 12V$, $V_2 = 10.67V$, $V_3 = 10.96V$, $V_4 = 805.98mV$, $V_5 = 521.74mV$.

![Fig. 21 The first operating point of example 3](image-url)
Step 3: Identify unstable operating point

Since we use different transistor models in this example, we need to read the parameters of each model from PSpice.
For Q1, default maximum forward beta $\beta_f = 231.7$ and default maximum reserve beta $\beta_r = 3.563$. For Q2, default maximum forward beta $\beta_f = 255.9$ and default maximum reserve beta $\beta_r = 6.092$.

In each model, $\alpha_r$ and $\alpha_f$ in matrix $T$ are still $\alpha_r = \beta_r/(1+\beta_r)$ and $\alpha_f = \beta_f/(1+\beta_f)$.

In $f(v_i) = m_i(\exp(nv_i)-1)$, $m_1$ and $m_3$ are reserve saturation current of the base-emitter junction. $m_2$ and $m_4$ are reserve saturation current of the base-collector junction. We have following relations: $\alpha_r m_i = \alpha_r m_{i+1} = I_s$. ($i = 1, 3$).

where $I_s$ is the $p-n$ saturation current. Here, $I_{s1} = 650.6e^{-18}$; $I_{s2} = 14.34e^{-15}$.

$n$ is a constant at a certain temperature. $n = q/kT$, where $q$ is electron charge, $k$ is Boltzmann’s constant and $T$ is temperature (in Kelvin).

Q1 is a PNP transistor, so, $m, n > 0$, but Q2 is a NPN transistor, so, $m, n < 0$.

D is a diagonal matrix with elements $d_i$.

\[ d_i = m_i \exp(nv_i) \quad (i = 1, 2, 3, 4) \]

We still use MATLAB to compute $\Gamma$ of each operating point and get the results as follows:

OP1: $\Gamma_1 = \det(QTD+P) = -6.2522e-5 < 0$

OP2: $\Gamma_2 = \det(QTD+P) = 0.2942 > 0$

OP3: $\Gamma_3 = \det(QTD+P) = 6.6814e-13 > 0$

Therefore, the conclusion is still that the middle operating point OP1 is unstable and two outside operating points OP2 and OP3 are both potentially stable.

4. Discussions and Conclusions

In this project, Green’s $\Gamma$ criterion for identification of unstable operating point is introduced. Theory on the stability of operating point for general nonlinear circuits is investigated. Degree theory is applied to identify unstable operating points. All these have been applied to two-transistor circuits with three simulation examples. The results of simulations demonstrate the correctness of theorems.

There are still some parts which can be improved and further studied. In order to identify the stability of operating points, we first need to use simulator PSpice to find all possible operating points. Then, we compute $\Gamma$ and identify their stability. During searching for all operating points, we plot the variation of voltage of each node, based on which we set initial values of node voltage. Sometimes, we need set the initial values of node voltages carefully in order to find the operating point that we want. Since Homotopy method can find all node voltages simultaneously, if we apply the result of using Homotopy method to identify operating points, the process of finding operating points would become much easier. Moreover, it would be of interest to discover properties regarding limit cycles and regions of attraction around potentially stable and unstable operating points.

References