Parallel Dynamic Voltage and Frequency Scaling for Stream Decoding using a Multicore Embedded System

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Outline

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Introduction

• Multicore Embedded System
  – With applications needing a more powerful CPU, the newly proposed multi-core designs is a trend for saving power.

• Power Consumption
  – Compared to single core platform, multi-core system needs a power managing mechanism to avoid excessive power consumption.
Related Work

• Parallel Computing
  – Increase a system processing speed in case of large amount of data or highly complex calculations
  – may be grouped into two main types:
    • Front-wave parallel processing
    • Internal parallel processing.
Related Work

• DVFS: Dynamical Voltage and Frequency Scaling
  - Be used to adjust the system voltage or frequency and achieve lower power consumption.

![Graphs](Image)

(a) Without DVFS

(b) DVFS
Common Feature: HMC Architecture Overview

- **Application Level**: Applications
- **Software Level**: Client/Server Architecture Integration
- **Hardware Level**: GPP(MPU), GPP OS, SPP(DSP), SPP(GPU), Interconnect

Common Feature:
H264 Decode Flowchart

- Entropy Decoding: CAVLC, CABAC
- IQ/IT: Inverse Quantization, Inverse Transform
- Intra/Inter Prediction: Spatial domain compression
- Deblocking: Eliminate blocking-effect
System Overview
H.264 Decode on HMC Embedded System
Parallel Model

The parallel model divided into two parallel ways based on different video format.
- Data dependent decoding
- Data independent decoding

\[ T = \frac{FEB}{S} + T_{proc} + D \]
DVFS Approach
DVFS Model

- We log the decoded time and frequency, and predict the process time for next frame.
- The different frame format uses the related coefficient.

\[
C_{\text{sim}} = \begin{cases} 
C_{\text{I frame}} & \text{for I frame} \\
C_{\text{P frame \& \& } \alpha \geq 15\%} & \text{for } \text{P frame \& \& } \alpha \geq 15\% \\
C_{\text{P frame \& \& } \alpha < 15\%} & \text{for P frame \& \& } \alpha < 15\% \\
C_{\text{B frame}} & \text{for B frame}
\end{cases}
\]
DVFS Approach with Buffer Mechanism

- Overestimation: Time Slack, Power Loss
- Underestimation: Video frame broken
- FEB: Buffer streaming data, Reconstruct overestimation
- BEB: Buffer decoded data, Reconstruct underestimation
The Android System Structure and Procedure

- Android 2.2 kernel
- OpenCORE framework
- The DVFS predictor decoder load perform prediction of the appropriate DVFS level.
- ioctl transfer data to the DSP Power Management Driver and performs DSP voltage and frequency control
Power Analysis

• Platform
  – PAC Duo Platform

• Video Format
  – H.264 Baseline Profile(1I29P)

• Power analysis
  – FLUKE 8846A
  – FLUKEView
Energy Consumption Saving
Distribution of the Deadline Miss

![Graph showing distribution of deadline misses for different categories: container, hall, mother, news, silent, akiyo. The x-axis represents the categories, and the y-axis represents the percentage of late submissions.](image-url)
Conclusion

- In this research, we introduced a parallel decoder streaming process for power efficiency perception in a multi-core embedded system by combining multi-core scheduling and a DVFS mechanism to provide a highly efficient and energy multi-media decoding mechanism.

- The experimental results show the decrease of 36.2% to 41.9% in power usage.
REFERENCES


