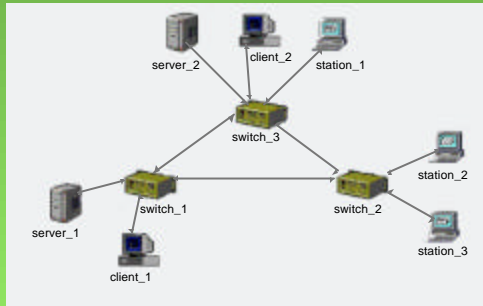
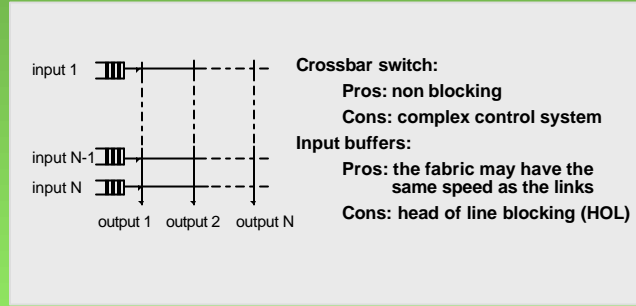


VHDL Implementation of a Crossbar Packet Switch

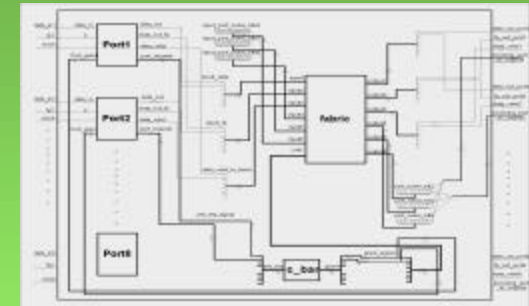
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 Communication Networks Laboratory, School of Engineering Science, Simon Fraser University



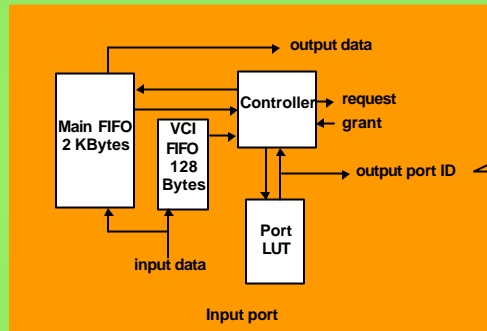
An ATM switch is a network element that forwards ATM packets to their destinations.



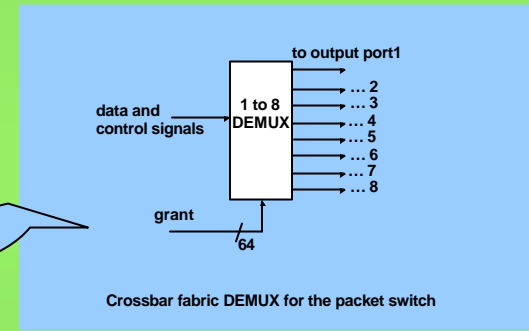
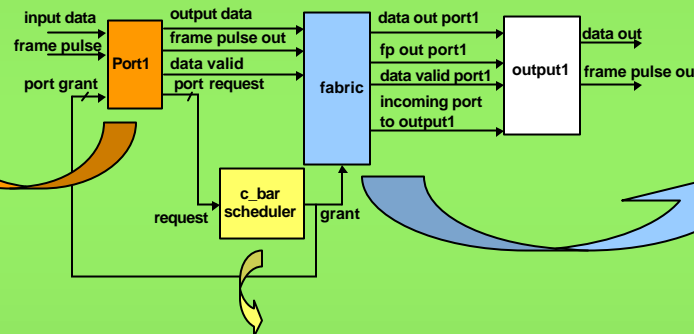
Input buffered crossbar switch



Our switch consists of input ports, a centralized scheduler, output ports, and a switch fabric.



Input port



Crossbar fabric DEMUX for the packet switch

Simple 4x4 arbiter

- Shaded cells are cells with grants
- Disadvantage: fixed priority for 1,1 arbiter

Logic inside an arbiter cell

A grant signal is only issued when there are no grants issued for cells on the top and left

A cyclic two-dimensional ripple carry arbiter

- Shaded cells are cells with grants, assuming (2,3) is the highest priority cell
- Disadvantage: combinational feedback loop

Rectilinear Propagation Arbiter (RPA) architecture

- Highest priority cell = (1,1)

Modified arbitration cell for RPA architecture

Diagonal Propagation Arbiter (DPA) architecture

- Shaded cells are cells that have received grants
- Disadvantage: first diagonal always has the highest priority

DPA architecture with priority rotation

- Shaded cells are cells with grants, when the highest priority is the first diagonal

Reference: J. Hurt, A. May, X. Zhu, and B. Lin, "Design and implementation of high-speed symmetric crossbar scheduler," Proc. ICC'99 Vancouver, Canada, June 1999, s37-6.