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Compiled Messages

[Print](#)[Save as File](#)**Subject:** About the Final Demo Tomorrow**Topic:** Technical Course Project Discussions**Author:** Jian Li**Date:** November 26, 2009 9:21 PM

Hi Everyone,

Here are some notes that might be helpful for your final demos tomorrow,

- Slides

- * Be sure to include your algorithm flowchart and block diagrams, because they help the judges to understand your design (those from your project proposal will be a good start).
- * It would also be helpful to have a summary of your design, ie, how many resources are used, how fast it runs; if you have a performance bottleneck what is it and why.
- * You can also briefly outline the problems you encountered and what you learned from it.
- * Split the demo and your slides properly, so that each member can demo their portion of work.
- * Each demo lasts about 20min (including questions), so keep your slides compact and to the point.

- Setup

- * You should setup *EVERYTHING* before the demo starts, i.e. bitstream, serial terminals, monitors, speakers, keyboards, software, your slides and etc. so please arrive early and get ready.
- * If you need to demo on the computers in LAB1 (the larger lab, not LAB1A), do remember to test everything again, because the tools on those computers are (10.1.02) different than those on LAB1A computers (10.1.03).

- Last but not least, get prepared and be confident.

Good luck.

Cheers,
Jian

[Reply](#)[Forward](#)**Subject:** TA office hours remain the same today**Topic:** Technical Course Project Discussions**Author:** Jian Li**Date:** November 26, 2009 1:11 PM

Hi everyone,

Although there will be no marking or demo today, I'll be available in lab 1A for my office hours from 4:30 to 8:30pm. See you there.

Cheers,
Jian

Reply
Forward

Subject: Group Report: Description of Your Design Tree?
Author: Jason Tsai

Topic: Technical Course Project Discussions
Date: November 24, 2009 11:06 AM

Hi,

I am not sure what we are supposed to do for the "Description of Your Design Tree". Does it mean we have to send the whole project as a zip file to Lesley?
Are we supposed to talk about the details of the entire folder in the report?

Thanks,
Jason

Reply
Forward

Subject: Re:Group Report: Description of Your Design Tree?

Topic: Technical Course Project Discussions

Author: Jian Li

Date: November 24, 2009 2:46 PM

Hi Jason,

Yes, as is stated in the handout, you should first clean all generated files (Project->Clean All Generated Files) before archiving your project with zip or other utilities. Normal designs are usually around 1 or 2 megabyte before compression. You don't have to talk about every file in the entire folder, but it would be nice to include a simple file list of *YOUR* design (software and hardware) with one line of illustration of purposes or functions of each file.

Another note is to check whether your system.xml file is getting too large (> 1megabyte) by opening it in a text editor and see if you have multiple identical peripheral library locations. This is because if you change your peripheral lib location in your design tree and do not modify the search path in project settings, EDK will keep appending the wrong path into system.xml, which results in a very large system.xml and a long project startup time.

Cheers,
Jian

Reply
Forward

Subject: Re:Group Report: Description of Your Design Tree?

Topic: Technical Course Project Discussions

Author: Jason Tsai

Date: November 24, 2009 4:30 PM

Thanks Jian

Reply
Forward

Subject: Question about the FIFO clk**Topic:** Technical Course Project Discussions**Author:** Piraj Fozoonmayeh**Date:** November 10, 2009 9:32 PM

Hi all,

I send the audio to my custom ip core via FSL (FSL_clk at sys_clk) , then this data is being stored in FIFO and read out at a later time. I have been providing the FIFO with the system clock, meaning that the read and write is happening at clock rise edge. the write_en of the FIFO is connected to the FSL_S_Exist, therefore whenever a data exist it will be written in the FIFO, but the issue is that I have the feeling that since the data is coming at 44.1k my fifo will write the same sample couple of times in itself. Do you guys think that I can use the FSL_S_Exist as the clk to my FIFO (since the data is coming at 44.1k)

Cheers,
Piraj

[Reply](#)[Forward](#)**Subject:** Re:Question about the FIFO clk**Topic:** Technical Course Project Discussions**Author:** Ryan Lynne**Date:** November 10, 2009 9:50 PM

Do you mean 44.1 kHz? As in a left and right sample every 44.1 kHz?

I used the FSL to interface with my audio controller but it is still not 100% as there is still some slight crackling in the audio.

I first made the FSL FIFO 8192 deep then made a function that fills the FIFO until it is full then stops, waits until the FIFO is "roughly" half empty and fills it the to max again. I say roughly because it is very hard to exactly know how fast it is being emptied.

I'm not sure if you can read and write to the FSL FIFO at the same time or about using the FSL_s_exists as a clock.

[Reply](#)[Forward](#)**Subject:** Re:Question about the FIFO clk**Topic:** Technical Course Project Discussions**Author:** Piraj Fozoonmayeh**Date:** November 10, 2009 9:58 PM

Hello,

I am not talking about FSL's FIFO, my core works fine there. I have a FIFO in my core, and since I have connected the system clock to the clk port of it, I have the feeling that the FIFO might write the sample couple of times.

(although the simulation is working good)

Cheers
Piraj

[Reply](#)[Forward](#)**Subject:** Re:Question about the FIFO clk**Topic:** Technical Course Project Discussions

Author: Lesley Shannon**Date:** November 16, 2009 12:34 AM

Hello

The write signal should not be connected to the fsl_exists signal. You use the fsl_exists signal to determine if there is any data in the fifo to read. You use the fsl_full signal to tell you when to stop writing. You definitely can't use an fsl_s_exists signal as the clk.

However, you can read and write from a FIFO at the same time - however, you have to be careful of the corner cases (when there is only one word left/one space left to store a word in the fifo).

Cheers

Lesley

[Reply](#)[Forward](#)**Subject:** Re:Question about the FIFO clk**Topic:** Technical Course Project Discussions**Author:** Piraj Fozoonmayeh**Date:** November 16, 2009 3:00 PM

Hi Lesley,

Thanks for the reply. I got it working.

Cheers,

Piraj

[Reply](#)[Forward](#)**Subject:** Interrupts not working properly after moving program from Bram to DDR...**Topic:** Technical Course Project Discussions**Author:** Ryan Lynne**Date:** November 10, 2009 9:28 PM

We ran out of room on the BRAM for our program so we used the linker script to move everything to the DDR and now the interrupts are not working properly. In particular the input from the keyboard using the UART doesn't work and the handler function is never reached. Any ideas?

[Reply](#)[Forward](#)**Subject:** Re:Interrupts not working properly after moving program from Bram to DDR...**Topic:** Technical Course Project Discussions**Author:** Mike Kubanski**Date:** November 11, 2009 12:21 AM

You could try finding out whether the microblaze is even receiving the interrupt, and then whether the XIntc driver is running the main interrupt handler. From what I have managed to find in the code, when an interrupt hits the microblaze, it calls the main interrupt handler set in its interrupt vector table (see microblaze_interrupt_handler.c in microblaze_0/libsrc/standalone.../src. The only interrupt vector registered should be the XIntc_DeviceInterruptHandler from the XIntc device driver if you are using one XIntc device.

I think you can run the software debugger and place break points at the `__interrupt_handler()` of the microblaze and at the `XIntc_DeviceInterruptHandler (xintc_l.c)` function. Thus if your interrupts are properly connected, the UART should trigger the high level interrupt handler, and you should hit

the breakpoint. If you get the breakpoint you know at least the interrupts are coming.

Next you can read the ISR and IER registers in the XIntc using xmd and see if your interrupt is enabled/triggered.

If it is, your handler might not be attached to XIntc properly (anymore?). If you look in XIntc_DeviceInterruptHandler in xint_l.c, if your interrupt was triggered it should call the handler you attached to XIntcs Handler table. Since you modified your linker script, you may want to check the initialization of XIntc and attachment of your handlers as maybe the xparameters might of changed?

If the microblaze handler never runs, then your interrupt is not hitting the XIntc controller, or the XIntc controller has interrupts disabled, or its not connected to the microblaze.

Hope this helps

Mike

Reply

Forward

Subject: Re:Interrupts not working properly after moving program from Bram to DDR...

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: November 14, 2009 10:33 AM

Strange problem? If you fix it let us know how. Thanks,

Reply

Forward

Subject: Re:Interrupts not working properly after moving program from Bram to DDR...

Topic: Technical Course Project Discussions

Author: Pranav Gupta

Date: November 14, 2009 7:07 PM

When switching to the DDR. Enable Caching on the microblaze, and then connect the DDR to the microblaze via the XCL (as well as the PLB). Caching requires use of BRAM, so you might want to reduce the ILMB and DLMB size used by the processor, else the design may not synthesize

Reply

Forward

Subject: Re:Interrupts not working properly after moving program from Bram to DDR...

Topic: Technical Course Project Discussions

Author: Ryan Lynne

Date: November 15, 2009 5:29 PM

What seems to have happened is that when we moved our entire program from the BRAMS on the FPGA to the DDR off the FPGA the program executed too slowly. This makes sense for our situation as the UART interrupt was lower priority than the AC97 interrupt which was still working.

To move your program to the DDR off chip, delete the old linker script, double click on it again and move everything possible in the drop down menus to the DDR ram. Then to solve the speed issue

make sure you enable the cache in the microblaze by doubling clicking on the microblaze module in XPS Platform View. The cache makes it run much faster!

-Ryan Lynne

Reply

Forward

Subject: How to make the interrupt controller see your interrupt signal...

Topic: Technical Course Project Discussions

Author: Ryan Lynne

Date: October 29, 2009 12:35 PM

For those making custom peripherals, with interrupt signals, you will have to add the following code to the peripherals .mpd file in order for the interrupt controller to see your interrupt signal.

```
./pcores/custom_peripheral/data/*****.mpd
```

```
PORT Peripheral_Interrupt = "", DIR = O, SIGIS = INTERRUPT, SENSITIVITY = LEVEL_HIGH
```

Thanks Tom for finding this code!

-Ryan Lynne

Reply

Forward

Subject: Re:How to make the interrupt controller see your interrupt signal...

Topic: Technical Course Project Discussions

Author: John Ogawa

Date: October 30, 2009 4:10 PM

Thank you. I was considering using interrupt for my custom peripheral. Saves me a lot of time in research.

John.

Reply

Forward

Subject: Re:How to make the interrupt controller see your interrupt signal...

Topic: Technical Course Project Discussions

Author: Ryan Lynne

Date: November 2, 2009 3:04 PM

No problem, here is the syntax for the various types:

```
SENSITIVITY = LEVEL_LOW  
SENSITIVITY = LEVEL_HIGH  
SENSITIVITY = EDGE_FALLING  
SENSITIVITY = EDGE_RISING
```

I Found this in the Platform Specification Format Reference Manual.

http://www.xilinx.com/support/documentation/sw_manuals/edk10_psf_rm.pdf

-Ryan Lynne

Reply

Forward

Subject: Re:How to make the interrupt controller see your interrupt signal...

Topic: Technical Course Project Discussions

Author: Jason Tsai

Date: November 6, 2009 8:47 PM

Hi Ryan,

Thanks for the information about the custom peripherals.

My partner has created a interrupt pin and had it show up in XPS.

I am wondering if I should write our own c codes to initialize the peripherals so that I could connect it properly to the interrupt controller.

Thanks,
Jason

Reply

Forward

Subject: Re:How to make the interrupt controller see your interrupt signal...

Topic: Technical Course Project Discussions

Author: Ryan Lynne

Date: November 9, 2009 3:56 PM

After you have added the interrupt signal to the Interrupt Controller (using XPS in the ports tab) you will have to use software to initialize and then service the interrupt.

You can use the lab3 as an example as it initializes the timer interrupt then sets a handler function to service the interrupt to blink the LED.

-Ryan Lynne

Reply

Forward

Subject: Re:How to make the interrupt controller see your interrupt signal...

Topic: Technical Course Project Discussions

Author: John Ogawa

Date: November 9, 2009 4:19 PM

The timer interrupt functions (disabling, initializing, setting handler) are provided for us in `\microblaze_0\include\xtmrctr.h`

But the interrupt functions do not exist for interrupt signals of user defined peripherals, so I have no idea how to use the interrupt in c code.

John.

[Reply](#)[Forward](#)

Subject: Re:How to make the interrupt controller see your interrupt signal...

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: November 10, 2009 7:04 AM

Hello

As Ryan said, the timer C code is an example. You have to write your own for your own peripheral. Unless the peripheral was included as part of XPS, there is no way that the designers could have written the corresponding software for the interrupt - they'd have no idea what the device is. Follow the standard steps required for initializing and utilizing interrupts in software (recall 151/215 and 351). If you are still having problems, please ask specific questions. They'll be easier to answer and may point you in the right direction.

Cheers

Lesley

[Reply](#)[Forward](#)

Subject: Can generate netlist but not bitstream

Topic: Technical Course Project Discussions

Author: John Ogawa

Date: October 28, 2009 6:05 PM

I made a VGA pcore, and added to my project. I get error from generating bitstream (netlist generation passes). This problem happens when I use falling clock edge for some processes and rising clock edge for other processes in VHDL. If I use only rising clock edge processes, then I do not get the error. Is it not possible to have both processes with falling edge and processes with rising edge?

Here is the detail of the error:

ERROR: 1 constraint not met.

PAR could not meet all timing constraints. A bitstream will not be generated.

To disable the PAR timing check:

1> Disable the "Treat timing closure failure as error" option from the Project Options dialog in XPS.

OR

2> Type following at the XPS prompt:

```
XPS% xset enable_par_timing_error 0
```

[Reply](#)[Forward](#)

Subject: Re:Can generate netlist but not bitstream

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 28, 2009 11:49 PM

Hi,

My suggestion is to stick with one edge. I assume that it is possible to use two in different processes but then getting into errors is more likely. Sorry i was no further help

Thanks,

Nik

Reply

Forward

Subject: Re:Can generate netlist but not bitstream

Topic: Technical Course Project Discussions

Author: John Ogawa

Date: October 29, 2009 4:14 AM

You're right, I'll stick with one edge. I thought I need to use both edges to solve the timing problem, but I realize now that the problem was due to something else.

John.

Reply

Forward

Subject: Re:Can generate netlist but not bitstream

Topic: Technical Course Project Discussions

Author: Jian Li

Date: October 29, 2009 10:50 AM

Hi John,

From what you've posted, it looks more of a timing issue of your design. You can definitely use both edges in different processes, as long as the timing makes sense, however, sticking with one sensitive edge would be easier.

You can either look for the PAR report for the spot that failed the timing constraints and fix it (change the logic, lower your frequency etc), or switch over to single edge sensitive.

Cheers,
Jian

Reply

Forward

Subject: Re:Can generate netlist but not bitstream

Topic: Technical Course Project Discussions

Author: John Ogawa

Date: October 29, 2009 11:43 AM

Thank you for the responses. I will stick to single edge sensitive processes.

John.

Reply

Forward

Subject: Re:Can generate netlist but not bitstream

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: October 29, 2009 10:38 PM

To be clear, in any given process, you can only use either the rising edge **or** the falling edge (you can't use both in a single process). However, you can use different edges in **different** processes if you want.

Cheers

Lesley

PS Just because you *can* do something, doesn't mean that you need to =)

Reply

Forward

Subject: Using extra bits of FSL

Topic: Technical Course Project Discussions

Author: Piraj Fozoonmayeh

Date: October 26, 2009 5:52 PM

Hi Jian,

is there any way that I can concatenate 2 integers, for eg ADC read has 18 bits and the FSL can take up to 32 bits, therefore I want to use the higher 16 bits to transfer some extra information to my custom core. (just to avoid an extra FSL)

1 way would be the adding the ADC value to 2^x $x > 18$

for eg if my extra information is 1 I can add my ADC value with 2^{19} . but I am not sure if this procedure will make my system slow.

Cheers,

Piraj

Reply

Forward

Subject: Re:Using extra bits of FSL

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: October 27, 2009 10:11 PM

Hello.

Remember, these are *not* integers. They are standard logic arrays (binary). '&' is the concatenation operator. Otherwise, don't add OR as long as the unused word is all zeroes it won't matter. However, concatenation is better.

Cheers

Lesley

Reply

Forward

Subject: Keep this warning in mind when editing your UCF Files

Topic: Technical Course Project Discussions

Author: Ryan Lynne

Date: October 26, 2009 3:44 PM

Do not assign the same net to two separate FPGA pins. XPS or ISE will only assign the net to one of the FPGA pins and will not give you an error.

For example, connecting the dip switch and the an LED to the same net:

```
NET "reset" LOC = "AC4"; ##LED0
NET "reset" IOSTANDARD = LVTTTL;
NET "reset" DRIVE = 12;
NET "reset" SLEW = SLOW;
```

```
NET "reset" LOC = "AD11"; ##dip1
NET "reset" IOSTANDARD = LVCMOS25;
```

This will not work and it will only connect "reset" to just the dip switch.

-Ryan Lynne

Reply

Forward

Subject: Re:Keep this warning in mind when editing your UCF Files

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: October 27, 2009 10:05 PM

It's more than that. You are defining reset as both an input and an output. You need to define a wire through. Otherwise, your reset signal defaults to whatever I/O port configuration you have in your top-level system.vhd file.

Cheers
Lesley

Reply

Forward

Subject: Drawing graphics

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 23, 2009 2:26 PM

Hi,

I was successful creating my background for my game, however, it takes to long for the background to get drawn. The limitation is the speed of microBlaze I believe. The longest functions to execute are trig functions. So here comes my question: Will it be faster for me to use dedicated HW Cores such as snoopy to do trig calculations for me? Will this make it faster then using c-math functions?

Nik

Reply

Forward

Subject: Re:Drawing graphics

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: October 24, 2009 12:39 PM

Why are you executing trig functions? Trig functions should be implemented using look up tables (concept, not technology) as they map really well to LUTs (technology, not concept). If you are going to do multiplication/division, be sure to include the hardware multiplier and divider. In the case of trig, you'd also need an FPU.

Although you might want to implement your own custom hw core (snoopy doesn't do anything like that - it's only a profiler), a look up table solution using BRAM is the most efficient solution.

Cheers
Lesley

Reply

Forward

Subject: Re:Drawing graphics

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 27, 2009 3:10 PM

I am executing trig functions to draw circle arcs on the monitor (It is one of my functions for drawing my background image of the "simon" GAME). The picture is nice, however the arcs are drawn by a ridiculously slow speed. I will try some of your advices and i will keep you updated:-)

Nik

Reply

Forward

Subject: Re:Drawing graphics

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: October 27, 2009 10:03 PM

Nikola,
These should be predrawn sprites that you load as need,
you shouldn't be drawing them dynamically.
Cheers
Lesley

Reply

Forward

Subject: Re:Drawing graphics

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 28, 2009 12:59 AM

Ok i will do that instead thanks is sounds easier,

Nik

Reply

Forward

Subject: Re:Drawing graphics

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 29, 2009 7:39 PM

Hi to display images on the TFT you can use the following code attached.

First load the image to DDR using dow command

```
dow -data image.bmp 0x9xxxxxxx
```

"store the image somewhere in the memory 0x9xxxxxxx (Please make sure you change the u32

DDR_BMP_Address = 0x90200000=> 0x9XXXXXXX TO)"

then run the FUNCTION attached (The code will do the necessary swapping of byts so they can get displayed on the screen TFT standard) the function should be called after the TFT is initialized at the following base address u32 baseaddrImageSavedDDR = 0x90000000;

Hi if you have any questions please post them here

Nik

Attachments: [BMP_DDR_Conversion.c](#)

Reply

Forward

Subject: Compact Flash Reader IO

Topic: Technical Course Project Discussions

Author: Sonca Teng

Date: October 18, 2009 3:21 PM

My upcoming milestone involves interfacing with the compact flash reader. It seems very few of the teams will be using it, so I thought I'd make a thread for the few of us who are to share research findings.

Leslie, I think you mentioned that you might be able to provide us with some helpful information and documentation regarding this, based on previous years?

Reply

Forward

Subject: Re:Compact Flash Reader IO

Topic: Technical Course Project Discussions

Author: Jian Li

Date: October 19, 2009 10:51 PM

Hi all,

I am posting the following based on the info shared by Eric Matthews and Aws Ismail when they set up their CF on XUPV2P.

1. Look up the docs on the XUPV2P user guide, for using system ACE controllers for non-volatile storage. Page 69-70. Note that you should format your CF card to the specification mentioned here.
2. The System ACE CompactFlash Solution Data sheet is worth reading too:
http://www.xilinx.com/support/documentation/data_sheets/ds080.pdf
3. You can include the SystemACE module from the system builder, or you can add it to your existing design manually and then connect the ports and modify the ucf file.
4. As for the software, look up the slideshow demo design from Lesley's course website. It is a bit old, but you can use the code. Pay attention to include the "xilfatfs" library as you'll need it to access fat format filesystem. Also, if you are using the same code in the slideshow demo, you'll probably need to set the stack and heap addresses as the same in the demo.

5. the slideshow demo uses the systemACE to load images from the CompactFlash into the DDR, and display them onto a VGA monitor with the XPSTFT core, which is a very useful reference for most of the display/memory related projects.

Cheers,
Jian

Reply

Forward

Subject: Re:Compact Flash Reader IO

Topic: Technical Course Project Discussions

Author: Sonca Teng

Date: November 4, 2009 1:33 PM

So after much frustration and wasted time, Pranav and I managed to get our CF cards formatted so that SysACE is happy.

Do **not** waste time trying to use the CF card formatting procedure outlined in the doc (using mkdosfs through Windows, etc). Instead, use gpart in Linux and simply format to FAT16. Done.

Everything else about getting the CF read/writing should be fairly straightforward.

Reply

Forward

Subject: interrupts - two types

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: October 17, 2009 3:08 PM

Hello everyone,
Remember that there are two types of interrupts: level and edge triggered. Futhermore, level triggered ones can be active high or active low, whereas edge triggered ones can look for rising/falling/both edge changes. When you choose a type of interrupt, make sure you think about the effects of this choice - particularly for the physical system. For example, mechanical contacts (buttons, etc) need debouncing. Be sure to give them time to settle.

Cheers
Lesley

Reply

Forward

Subject: Re:interrupts - two types

Topic: Technical Course Project Discussions

Author: Piraj Fozoonmayeh

Date: October 17, 2009 5:43 PM

Hi Lesley,
Yes I noticed the debouncing issue with the PBs. I reduced this debouncing by turning the GPIO interrupt off in the beginning of my interrupt sub routine, and turning it back on at the end, but I still receive the interrupt twice. I thought this issue will be solved as my interrupt subroutine gets bigger.

Regards,
Piraj

Reply
Forward

Subject: GPIO Interrupt from Push buttons
Author: Piraj Fozoonmayeh

Topic: Technical Course Project Discussions
Date: October 15, 2009 10:38 PM

Hi All,
I have made the interrupt to work with GPIO. but t how do I know which pin of the GPIO was in charge of that interrupt. for eg if you connect push buttons (up and down) to the GPIOs pin 0 and pin1, how do we know if the interrupt has come from Left or Right. Reading the values of the GPIO in the routine is not helpful, because by the time the interrupt routine is called, the value of the GPIO register for the push buttons are back to their original state.
Regards,
Piraj

Reply
Forward

Subject: Re:GPIO Interrupt from Push buttons
Author: Aminreza Ahari Kaleibar

Topic: Technical Course Project Discussions
Date: October 15, 2009 11:25 PM

Hi Piraj,

I think that two different interrupts should be connected to these two pins i.e. two different interrupts can be called as these pushbuttons return different values ,and so it is easy to distinguish which one has been pushed.

Sincerely,
Amin

Reply
Forward

Subject: Re:GPIO Interrupt from Push buttons
Author: Piraj Fozoonmayeh

Topic: Technical Course Project Discussions
Date: October 16, 2009 12:16 AM

Hi Amin,
We connect the GPIO interrupt to interrupt controller , and as far as I know GPIO has only 1 interrupt.
regards

Reply
Forward

Subject: Re:GPIO Interrupt from Push buttons
Author: Lesley Shannon

Topic: Technical Course Project Discussions
Date: October 17, 2009 3:04 PM

Unless you are clocking your design in the kilohertz or the interrupt is delayed by 10s-100s of milliseconds, there's no physical way that you are able to push a button for less than 10 ms (which means that you can't be done pushing the button before the handler runs =). What's more likely is

that you are experiencing a "bounce". When you push a button the mechanical contact will bounce before holding - meaning that depending on when you read the register value, you might get a zero or a 1. You should try reading in the GPIO register multiple times and look for changes to determine which button is pressed.

Cheers

Lesley

Reply

Forward

Subject: Outputting to a file from a test bed / test bench...

Topic: Technical Course Project Discussions

Author: Ryan Lynne

Date: October 15, 2009 8:43 PM

Since I wasted so much time on this I will share an example. If anyone has an input example feel free to add it.

```
LIBRARY ieee;
use IEEE.std_logic_textio.all;
use std.textio.all;
```

```
ARCHITECTURE behavior OF ac97_testbench IS
BEGIN
```

```
process (ac97_bit_clock, ac97_sync) is
variable s : line;
variable s2 : line;
variable cnt : integer := 0;
file output : text open write_mode is "C:/temp/lab6/output.txt";
begin
```

```
if rising_edge(clk) then
cnt := cnt + 1;
```

```
write(s, "Number of clock edges: ");
write(s, cnt);
writeline(output,s2);
end if;
```

```
end process;
```

```
END;
```

```
-----
-- Example output to file
-----
```

```
--Number of clock edges: 1
--Number of clock edges: 2
--Number of clock edges: 3
--Number of clock edges: 4
--Number of clock edges: 5
--Number of clock edges: 6
```

--Number of clock edges: 7
--Number of clock edges: 8
--Number of clock edges: 9
--Number of clock edges: 10

Attachments: [output_example.vhd](#)

Reply

Forward

Subject: Re:Outputting to a file from a test bed / test bench...

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: October 17, 2009 2:59 PM

Sorry guys. I teach this in my 350 class. For those of you that haven't taken my class, go to my 350 website and poke around the lab stuff. Also, I cover an example in one of my lectures (called testing I think). What Ryan's got here is good, but this other material might help. Also (for those of you that bought the HDL book I recommended), there are examples there.

Cheers
Lesley

Reply

Forward

Subject: DDR issues

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 14, 2009 5:36 PM

Hi,

I have made my video work and it is reading shared memory based in the DDR. So i get the square displayed that i want, however the screen has random pixels lightning up. In other words the DDR memory is changing in certain addresses. My screen is still showing the square white block, however some pixels are randomly showing up in the screen with random colors?

I am stuck on this for three days and i am unable to fix it. Dos anyone have any idea why is that so or is my DDR malfunctioning?

This error has noting to do with my milestone however the screen output is not as Cristal clear.
Thanks,

Nik

Reply

Forward

Subject: Re:DDR issues

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 15, 2009 2:36 PM

Hi,

I have tested if i can read and write to the DDR and all that is working however sometimes some

of the bits change (in random memory addresses). I can see this using the software debugger and the memory button? When i insert the base address of the DDR and keep scanning (while the processor is running) i can see some of the bits which i have previously initialized change? I have nothing else writing to the DDR?

So could this be do to the memory malfunctioning?

Nik

Reply

Forward

Subject: Re:DDR issues

Topic: Technical Course Project Discussions

Author: Jian Li

Date: October 15, 2009 3:02 PM

Hi Nik,

I think you can try your design on a different board, and see if the same happens.

Jian

Reply

Forward

Subject: Re:DDR issues

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 15, 2009 3:18 PM

Hi,

Thanks for you quick reply

I just did it actually and guess what, that was the problem since Saturday not the inverting of the pin hahah (I lost so much time on this). My DDR is malfunctioning (Not working properly). I would need to use another board for my demo. Thanks,

In addition i have contacted Fred and he das not have any extra DDR's.

So my question is if some other group is not using their DDR can i use it instead since i need it to save my video data on it?

Nik

Reply

Forward

Subject: Re:DDR issues

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 19, 2009 3:17 PM

One last post to resolve this thread.

I lied..... seems that even 256mb of ram is unstable in the new XPS 10.1 SP3 with the new memory controller.

However i did finally resolve my problem with the ethernet not working.... , again it was the memory.

That is now 3 different KVR266x64c25/256 boards i have tried in the new memory controller, and I have had 3 sets of results.

KVR266x64c25/512 does not work,with 10.1 SP3, BUT it will pass the inbuilt memory test from year 2005 , however that IP core is no longer supported.

The ethernet was not working because the memory randomly corrupted both the program & stack, this is despite the memory passing the memory tests.

I think perhaps the memory test needs changing, so that it writes to the whole DDR memory, then goes BACK to the start to verify the memory after a period of time.

So, I now have a fully working XAPP1026 for the XUPV2P board under XPS 10.1 SP3, and it only took 3 weeks.

Hurray for our side ;-)

Reply

Forward

Subject: Re:DDR issues

Author: Nikola Cucuk

Topic: Technical Course Project Discussions

Date: October 19, 2009 3:19 PM

However when i swapped the board with Stefan (This board is with Fred now) everything worked fine. I am unsure if it is the board or the DDR. I will run the golden configuration soon and let you know.

Nik

Reply

Forward

Subject: Re:DDR issues

Author: Nikola Cucuk

Topic: Technical Course Project Discussions

Date: October 20, 2009 1:45 PM

Hi,

Thanks for your assistance. My DDR issue is now fixed.

Thanks,

Nik

Reply

Forward

Subject: Re:DDR issues

Topic: Technical Course Project Discussions

Author: Pranav Gupta

Date: October 22, 2009 10:20 AM

Hi,

Jian and I noticed that the 'faulty memory' has the RAM ICs on both sides of the module(front and back). However the working memory has the RAM ICs only on the front side. I guess this somehow creates a problem when connecting to the FPGA, as the ports may have changed and the FPGA cannot access all locations on the DDR module. My board has the same problem and I will need to get my memory swapped as well.

Pranav

Reply

Forward

Subject: Re:DDR issues

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: October 23, 2009 10:08 AM

Hi all,

Thanks for the info. I've figured out the problem =) There are two different sets of boards. The ones with DDR on "one side" of the daughter card have 256MB of DDR and the other with chips on "both sides" have 512MB. Only the boards with 256MB of DDR were supposed to be distributed - the tutorial is designed to work with that configuration.

If the wizard allows you to choose between the two configurations, be sure you are picking the right one (otherwise you aren't driving all of the DDR pins - which is where some of the problems are coming from). However, I don't think the wizard supports the other configuration (512MB). Could anyone requiring DDR for their project with a board that has the larger DDR configuration please contact Jian? We'll figure out what needs to be done depending on the number of people with a problem.

Cheers

Lesley

Reply

Forward

Subject: Re:DDR issues

Topic: Technical Course Project Discussions

Author: Nikola Cucuk

Date: October 23, 2009 2:19 PM

That is funny, since when i was setting up the DDR it was recognized by the EDK as 256? What

ever as long as the issue has been solved. :-)

Reply

Forward

Subject: Re:DDR issues

Topic: Technical Course Project Discussions

Author: Farzad Abasi

Date: October 24, 2009 4:11 PM

Hi Lesley,

Me and my partner are also experiencing problems with our board. We ran the memory test on the 452 website with Jian on thursday night and it failed. We tried to ask Fred to swap our board but he wanted confirmation from you first. Also, we just looked in EDK and there doesn't appear to be a configuration for 512MB ddr (it just has a "custom" drop down menu for it). But I'm pretty sure these modules are 256MB because the sticker on the memory says 256. I took a look at the spec sheet from kingston's website:

(http://www.valueram.com/datasheets/KVR266X64C25_256.pdf)

and it says there may be other configurations. The spec sheet says:

"The components on this module include eight 32M x 8-bit (8M x 8-bit x 4) DDR266 SDRAM in TSOP packages" so maybe the two sided modules have sixteen 16M SDRAM TSOP packages?

Please let us know how to proceed. Thank you very much,
-Farzad

Reply

Forward

Subject: Re:DDR issues

Topic: Technical Course Project Discussions

Author: Lesley Shannon

Date: October 27, 2009 10:16 PM

Farzad,

I don't know your group number, but I assume that this has been addressed already. If not, please email me offline.

Cheers

Lesley

Reply

Forward

Subject: Examples in the EDK installation

Topic: Technical Course Project Discussions

Author: Jian Li

Date: October 14, 2009 2:51 PM

Hi all,

Just a quick remind: there are a lot of examples in the EDK installation folder \$EDK\hw\XilinxProcessorIPLib\pcores\, which would serve as good resource for references when you write your own IP core. The same applies for the software, you can look through the drivers in the "sw" subfolder as well.

Jian

[Reply](#)[Forward](#)**Subject:** Info for Milestone Demo on Thursday Oct. 15**Topic:** Technical Course Project Discussions**Author:** Jian Li**Date:** October 13, 2009 11:34 PM

Hello All,

The first Milestone demonstration is two days away. Your time slots are the same as for the lab test. If you haven't returned your original project proposal and revised milestones you will receive a ZERO for the demo as I won't know what you were supposed to do.

Here is the format for the demos.

- Show up and setup 10 minutes before your demo time. Be sure that your bitstreams are built and ready to be downloaded.

- You must demonstrate your milestone to receive marks (simulation results, video on screen, audible audio, flashing lights, etc). Telling me you did task "X" and showing me C code or VHDL will get you nothing.

- EACH of you MUST have a 1 PAGE MAX WRITTEN description of what your milestones for the week were (from your revised proposal), and what you actually accomplished. You will not necessarily lose marks if what you actually accomplished differs from your milestone so long as you can clearly explain and justify why this happened and show me an equivalent amount of work in another form.

-Marking Scheme

2 marks : Written description of milestone and accomplishments. Must be clear and concise. Reasonable grammar/spelling. Max 1 page long (1/2 page preferable). If this is not present, I will not know what I am marking for your demo. I WILL GIVE OUT ZEROS IF THIS IS NOT PRESENT AT THE DEMO.

4 marks : Demonstration of milestone. Each partners must be able to clearly and concisely tell me about their work. You are expected to be able to answer any questions about your work (how does it work, architecture details, what design choices did you make, what obstacles did you have to work around, etc). I may also request to see your source VHDL/C or other supporting documents.

6 marks total

Cheers,
Jian

[Reply](#)[Forward](#)**Subject:** Creating a testbench in ISE...**Topic:** Technical Course Project Discussions**Author:** Ryan Lynne**Date:** October 13, 2009 3:17 PM

Someone showed me how to quickly create a VHDL test bench template on the day of the lab test so I thought I would share:

ISE -> Project -> New Source -> Select "VHDL Test Bench and enter a name -> Next -> Select the VHDL file to simulate -> Next

This creates an excellent starting point.

Reply

Forward

Subject: Creating a peripheral on the bus FSL/PLB...

Topic: Technical Course Project Discussions

Author: Ryan Lynne

Date: October 13, 2009 2:30 AM

Here is a way to quickly setup all of the files for a user peripheral on the bus.

Hardware -> Create or Import Peripheral -> Next -> Create templates for a new peripheral -> To an XPS project -> Enter a name -> Next -> Choose bus FSL/PLB -> Next -> Follow intructions

Seems to work well for the FSL bus, haven't tried it for the PLB bus.

Reply

Forward

Subject: Re:Creating a peripheral on the bus FSL/PLB...

Topic: Technical Course Project Discussions

Author: Piraj Fozoonmayeh

Date: October 14, 2009 11:02 AM

great post. thanks

Reply

Forward

Subject: References for VGA controllers

Topic: Technical Course Project Discussions

Author: Pranav Gupta

Date: October 12, 2009 6:55 PM

Hi,

I found the following link, which I felt was a good reference for a VGA controller, along with a sample design written in VHDL. It is written for the Altera UP2 board

http://www.eecg.toronto.edu/~jayar/ece241_05F/vga_new/index.html

This next link is a more detailed description about the VGA standard

<http://martin.hinner.info/vga/vga.html>

Please post any more references for VGA designs with this thread

Cheers,
Pranav

Reply
Forward

Subject: Re:References for VGA controllers
Author: Nikola Cucuk

Topic: Technical Course Project Discussions
Date: October 12, 2009 8:02 PM

Yes try using the tft IP. I am trying to do it however i have issues connecting the pins in the .uce file. Since this IP dos not have VGA_COMP_SYNCH, and VGA_OUT_BLANK_Z. Anyways i am sure it works for DVI standard though. But it is staying same support

Reply
Forward

Subject: CF?
Author: Nikola Cucuk

Topic: Technical Course Project Discussions
Date: October 11, 2009 11:12 PM

Hi,

Do we have any extra CF's (compact flash units) that i can use for my project since that would simplify my project significantly and if not which models dos this board support?.

Thanks,

Nik

Reply
Forward

Subject: Re:CF?
Author: Lesley Shannon

Topic: Technical Course Project Discussions
Date: October 12, 2009 10:16 PM

Hello
Everyone has a CF slot built into the board. As to flash cards, I'm afraid you will have to provide your own. The school hasn't purchased any for this course.
Cheers
Lesley

Reply
Forward

Subject: How can I modify hdl of IP cores?
Author: Jason Tsai

Topic: Technical Course Project Discussions
Date: October 9, 2009 5:50 PM

I found an example EDK project which can display text images on the monitor. I want to modify the hdl code so that I can put game character images, but I do not know how. I think I need to create ISE project to work on that hdl code, but I do not know how to work on the hdl IP core from EDK to ISE then work back to EDK (if that is what I am supposed to do).

Could someone help?
Jason.

Reply
Forward

Subject: Re:How can I modify hdl of IP cores?
Author: Lesley Shannon

Topic: Technical Course Project Discussions
Date: October 9, 2009 8:57 PM

Hello everyone,

Okay, I'm not really sure I understand the question. Assuming that the core is not encrypted, then you can edit its HDL wherever you want using any text editor. When creating (editing) a module comprised of HDL files, you can design it wherever you want. I'm guessing you'll use a combination of ISE and modelsim as they provide HDL simulation capabilities (both waveform and file i/o). EDK has an import wizard you can use to import hdl files as a core into an edk project. However, I've already shown you the directory structure format (snoop is your template) and what other files you need .pao and .mpd. This is what the import wizard does for you.

As I stated initially, I didn't really understand the question. Hopefully, I've kind of covered what ever the major concerns are. If not, please post again to clarify.

Cheers
Lesley

Reply
Forward

Subject: AC97 Digital Controller Discussion...
Author: Ryan Lynne

Topic: Technical Course Project Discussions
Date: October 9, 2009 2:53 PM

I thought it may be useful to start a thread for those who are developing an AC97 Digital Controller. If you have questions or have figured out some key points post them here to help everyone out.

Wiki Entry:
<http://en.wikipedia.org/wiki/AC'97>

Intel Audio Codec 1997 Specs:
http://download.intel.com/support/motherboards/desktop/sb/ac97_r23.pdf

LM4550 AC 97 Chip Specs:
<http://www-mtl.mit.edu/Courses/6.111/labkit/datasheets/LM4550.pdf>

-Ryan Lynne

Reply
Forward

Subject: Re:AC97 Digital Controller Discussion...
Author: Scott Hsieh

Topic: Technical Course Project Discussions
Date: October 10, 2009 4:15 PM

i've searched around about AC97, apparently the AC97 core, lib and headers are not included in our veersion of XPS, so the ac97 interface etc have to be either find online or have to make our own

[Reply](#)[Forward](#)**Subject:** Re:AC97 Digital Controller Discussion...**Topic:** Technical Course Project Discussions**Author:** Nikola Cucuk**Date:** October 10, 2009 4:44 PM

I would assume this is done on purpose so we develop or use other internet resources to implement both audio and video. thanks,

nik

[Reply](#)[Forward](#)**Subject:** Re:AC97 Digital Controller Discussion...**Topic:** Technical Course Project Discussions**Author:** Ryan Lynne**Date:** October 11, 2009 12:56 PM

It probably costs additional \$\$ for the AC97 Controller IP core.

-Ryan Lynne

[Reply](#)[Forward](#)**Subject:** Re:AC97 Digital Controller Discussion...**Topic:** Technical Course Project Discussions**Author:** Ryan Lynne**Date:** October 11, 2009 1:06 PM

Basically it appears we have to make the hardware for the AC97 Controller in Verilog or VHDL. This controller has to be linked to one of the buses and the AC97 Codec (LM4550 chip), the link between the Controller and the Codec is referred to as the Audio Codec Link or AC Link. The AC Link is composed of the following signals: sync, sdata_out, sdata_in, bit_clk, and reset.

The AC Link Serial Interface Protocol can be found on page 18 of the LM4550 pdf.

-Ryan Lynne

Attachments: [webct_1.JPG](#)

[Reply](#)[Forward](#)**Subject:** Re:AC97 Digital Controller Discussion...**Topic:** Technical Course Project Discussions**Author:** Lesley Shannon**Date:** October 12, 2009 10:11 PM

You won't have a core that connects to the PLB, but be sure to look through the designs for one that connects to the OPB. You can always use a PLB to OPB bridge if you want.

Cheers

Lesley

Reply
Forward

Subject: Re:AC97 Digital Controller Discussion...
Author: Ryan Lynne

Topic: Technical Course Project Discussions
Date: October 17, 2009 11:51 PM

If your controller is not working check to make sure you are using an active high reset not an active low reset as stated in the LM4550 datasheet.

"The [LM4550] CODEC is held in a reset state until the AUDIO_RESET_Z signal is driven high by the FPGA overriding a pull-down resistor (R15)."

Reply
Forward

Subject: Re:AC97 Digital Controller Discussion...
Author: Lesley Shannon

Topic: Technical Course Project Discussions
Date: October 21, 2009 1:01 PM

I think Ryan said the opposite of what he meant. The device is in reset when your reset signal is low (called active low reset because the unit is in reset when the reset signal is low).
Cheers
Lesley

Reply
Forward

Subject: Xilinx FSLs
Author: Fatemeh Aezinia

Topic: Technical Course Project Discussions
Date: September 11, 2009 11:35 AM

Hi Jian,

It seems that the reference related to the MicroBlaze (Xilinx FSLs) is not available in this link:
http://www.ensc.sfu.ca/~lshannon/courses/ensc452/reading_material.html

Could you please tell me how I can get it?

Thanks a lot,
Fatemeh

Reply
Forward

Subject: Re:Xilinx FSLs
Author: Jian Li

Topic: Technical Course Project Discussions
Date: September 11, 2009 1:53 PM

Hi,

Just google "Xilinx FSL".

And you'll find plenty of doc/help/references within the EDK tools once you have access to them.

Jian

Reply

Forward

Subject: Dev Board?

Author: Kyle Balston

Topic: Technical Course Project Discussions

Date: September 8, 2009 10:32 AM

I was just wondering what the model of our dev board is.

Thanks,
Kyle.

Reply

Forward

Subject: Re:Dev Board?

Author: Jian Li

Topic: Technical Course Project Discussions

Date: September 8, 2009 3:29 PM

It's a XUPV2P, Xilinx University Program Virtex II Pro.

You can look it up online on either xilinx.com or digilentinc.com, both of which you will be visiting a lot for the course.

Jian

Reply

Forward

Subject: Re:Dev Board?

Author: Kyle Balston

Topic: Technical Course Project Discussions

Date: September 9, 2009 12:38 PM

Ok. Thanks!

Reply

Forward

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