Simon Fraser University
School of Engineering Science
ENSC452/894: Advanced Digital System Design
Fall 2009

Facts Sheet

Instructor:

Dr. Lesley Shannon E-mail: lshannon@ensc.sfu.ca Office: ASB 8819
Office Hours: Tuesdays10:30am-12:30pm and Thursdays 3:30-4:30pm

Teaching Assistants:

Jian Li E-mail: jla193@sfu.ca Office: ASB 8803.1
Office Hours: Wednesdays 1:30-2:30pm

Class:

Lecture: Tuesday 8:30am-10:30am, AQ 5018
Labs: Thursday 4:30pm-8:30pm, Lab 1a
Each lab group will have two individuals (unless specifically permitted by the instructor). It would be preferable to ***not*** have graduate and undergraduate lab pairings. You will be given a board used for the labs and your final project: ***You are responsible for the well being and proper care of this board!!***

The Course:

This is a course on the design of large digital systems. Digital systems lie at the heart of almost any electronic system including consumer devices, cell-phones, signal processing systems, computers, biomedical devices, etc. This course will provide the opportunity to design real digital systems containing significant amounts of hardware and software.

Most of the course will be focused on a design project, where you will have the opportunity to design a real system using state-of-the-art tools and technology.

Course Web Page:

The course web page is at http://www.ensc.sfu.ca/~lshannon/courses/ensc452/. Handouts will be posted. I will try to post lecture notes before each lecture so that you can print them out before class. We will be using WebCT, but only for the bulletin board postings. All other material can be found from the course web page.

Course Bulletin Board:

All students *must* regularly check the course bulletin board. All course related questions ***must*** be posted to the bulletin board. Postings are set to be anonymous (you can sign your name if you like for bonus marks). Announcements and hints regarding the labs and project will be posted here. I have also created class mailing lists so that last minute announcements can be sent when necessary.

Suggested References:

Timing Analysis:

High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Hall, Hall and McCall, Wiley. Chapter 8 is most directly relevant to the lectures. Chapter 9 gets more into setting up spreadsheets to do the computations. (Available online from Books 24x7.com)

Clock Domains and Synchronization:

Digital Systems Engineering, Dally and Poulton, Cambridge. Chapter 10 (Available at Bennett Library)

Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs, Clifford E. Cummings, SNUG-2001. (Available from the course web page)

Recommended HDL Reference:

Custom Courseware copies of Douglas J. Smith's HDL Chip Design: A Pracitical Guide for Designing, Synthesizing & Simulating ASICs and FPGAs Using VHDL or Verilog are recommended for this course.

Labs:

There is a weekly 4 hour lab component to the course. Initially these lab periods will be used to perform tutorials to learn about Xilinx's system software and hardware. After the marked lab demonstration, the remaining labs will be used to work on the final project. Students are required to follow the lab policies outlined by the School of Engineering Science along with those provided in the lab handouts. *Please read them carefully.*

Lab Demonstration:

Students are required to complete and present a lab demonstration for October 8th. Students will have to demonstrate that their design works and be able to answer questions about their design choices and the Xilinx tools (consider this a preliminary for Test 1). There are several lab tutorial modules that should be completed to help students prepare. See the Lab Demo Handout for further information.

Project Proposal:

Students will be required to submit a project proposal by ***no later than Friday 3:30pm, October 2nd*** in the course drop box. The proposal should consist of both a group and an individual component. This document will be used to evaluate the remainder of your lab work and the final project report and demonstration so it should be well thought out. Please see the Project Proposal Handout for further information.

Project Report:

Students will be required to submit the final project report by the beginning of class on Tuesday, December 1rst. The report will consist of both a group and an individual component. This document should reflect the final status of the project and the contributions of each lab partner. Please see the Project Report Handout for further information.

Project Presentation:

On November 27th, students will be required to present the final status of their project. The details of what should be included in this presentation will be provided later on in the course.

Exams and Tests:

While there is no final exam, two in-class tests have been scheduled:

Test 1: **October 20th** (Focus: material from the lab, including the tutorial modules)
Test 2: **November 24th** (Focus: material from lectures)

Mark Breakdown:

- Test 1 (Oct 20th) 20 %
- Test 2 (Nov 24th) 20 %
- Lab Demonstration 5 %
- Project Lab Work 12 %
- Final Project Demonstration 8 %
- Project Proposal 15 %
  - Group Mark 6 %
  - Individual Mark 9 %
- Project Report 20 %
  - Group Mark 8 %
  - Individual Mark 12 %
- Class Participation ***Bonus*** 5 %

Class Participation:

Finally, it is important in this class that people work together. In a design team everyone needs to contribute to the group. That means speaking up when there's a problem or when you see a solution. Although the Bulletin Board will not be marked, good "citizenship" demonstrated through in class participation, in-lab cooperation, and asking and answering each others questions on the bulletin board will be rewarded with a maximum of a ***5% bonus*** on a student's final mark.

*****Important Notes***: While I promote team work and helping each other, code copying and plagiarism will ***NOT*** be tolerated. Any individual found copying code from other class members or the web will receive an automatic ***0*** on the ***entire*** lab component. Similarly, anyone found copying during quizzes, midterms, or the final will receive a ***0*** for the ***entire*** testing component. Any code copying or plagiarism will result in an automatic ***0*** for the class participation bonus.

Please take note of the disclaimer posted to the bulletin board regarding improper usage.