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March 11, 2013

Dr. Andrew Rawicz
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Simon Fraser University
Burnaby, BC V5A 1S6

Re: ENSC 440 Design Specifications for Automated Attendance System

Dear Dr. Rawicz,

Attached to this letter is our team's design specification for an automated attendance system, regarding our 440 engineering science class. The project aims to design and implement a system that will take students attendance at university through automatic identification check and facial recognition.

This document outlines all the necessary information and specifications of our proposed Automated Attendance System and all its sub-components. The design specification described is this document is to provide an in-depth look into the design process required to meet the basic functional requirements for a proof-of –concept model. We will occasionally discuss design improvements, but these iterations will not be implemented I this stage of development.

Our company, Secure Com Systems consists of five talented engineers. Omar Khlif, Tahani Trigui, Oldooz Pooyanfar, Hongxin Dai, and Dong Geun Shin are all fourth-year engineering students majoring in computer, electronics and systems engineering. We will be delighted to hear from you in order to further discuss our functional specification. If you have any question or concern about our product, please contact me via email at okhlif@sfu.ca.

Sincerely,

Omar Khlif

Chief Executive Officer

Enclosure: *Design Specifications for Automated Attendance System*

Design specification for

Automated Attendance System

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Executive Summary

At Secure Com Solutions, the goal is to help educational institutes improve the learning curve of students by taking attendance. This device makes taking attendance less time consuming and more accurate. While it helps the instructors keep track of the attendance, it also helps them check the students' attendance records during exams. The growing numbers of students entering the higher educational institutes is another factor for employing a device that will reduce the amount of work for the instructors and professors.

The device employs the RFID reader's functionality to securely check for each students' unique ID. After the unique number is taken it will be compared to the student list in class, and the students picture will be accessed. Then using the real-time picture taken after recovering the RFID number, it will be compared to the picture associated to the RFID number from the data base.

This document will outline the design and implementation process of the design. The members of Secure Com Solutions employ their skills in hardware and software design to design and implements both hardware and software of the device.

- RFID reader/tag - used to check the students' identity and providing the program with an associated picture with their number - the RFID system will be designed such that it follows all the safety regulations

- Camera and Image processing - after the RFID associating the number with a picture this program will double check their identity

The document will also explain the testing that will be done for each sections of the design separately so that. The testing will assure that each subsystem is designed and implemented to be compatible with the desired output. This results in integration of the components with minimum effort and higher efficiency.

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Glossary

SCS –	Secure Com Solutions
RFID –	Radio Frequency identification
The system –	The SCS automated attendance system under development
ID number –	An identification of a particular student, each student has a unique number
ISO –	International Organization of Standardization
USB –	Universal Serial Bus
GUI –	Graphical User Interface
DC current –	unidirectional flow of electric charge
AC current –	alternating current is the flow of electric charge periodically reverses direction
PIC microcontroller –	Peripheral Interface Controller, a small computer on a single integrated circuit. Low cost, extensive collection of applications and serial programming
PCB –	Printed Circuit Board
HID –	HID global, a manufacture of secure identity solutions.
SFU –	Simon Fraser University
FSK –	Frequency Shift-Key
Envelope detector –	An electronic circuit that takes a high-frequency signal as input and provides an output which is the envelope of the original signal
MPLAB –	Integrated Development Environment (IDE) is a free, integrated toolset for the development of embedded applications on Microchip's PIC
PIC kit –	A family of programmers for PIC microcontrollers made by Microchip Technology. They are used to program and debug microcontrollers

OSCCON –	Oscillator Control Register
MVS –	Microsoft visual studio Is an integrated development environment (IDE) from Microsoft. It is used to develop console and graphical user interface applications along with Windows Forms applications
Mock-up –	Mock-up is a prototype if it provides at least part of the functionality of a system
openCV –	(Open Source Computer Vision Library) is a library of programming functions mainly aimed at real-time computer vision, developed by Intel
MySQL	World's most used open source relational database management system

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1 Introduction

The Automated Attendance System can automatically capture student's attendance based on the RFID and face recognition technologies. The system consists of a camera, an RFID reader and tags, and a software solution. The camera will capture the image of the users when they pass the RFID card by the reader. The RFID reader will collect the information from the tag, digitizes it, and transmits it to the computer. The software gets the student information associated with the RFID tag, checks whether the student is enrolled in the class and compares the student's photo with the image captured by the camera. The design specification describes the technical details for the design of each component of the automated attendance system.

1.1 Scope

This document expands on our thinking behind our design choices and will outline the hardware and software design blocks of the attendance system. The design specification includes and discusses all the requirements for a proof-of-concept system which are labeled "A" in the functional specification. At the end of the specification, a series of test plans of the system and its units are provided in order to evaluate the function of our prototype.

1.2 Intended Audience

The design specification document will be used by all members of the Secure Com Solution team throughout the development of the Automated Attendance System development. This document will be used to ensure that all the design functions conform to the goal of the product. During testing the engineers of Secure Com Solutions will use this document to implement the test plan and to approve the correct behaviour of the system.

2 System specification

The automated attendance system high level overview is modeled as shown in figure 1 below.

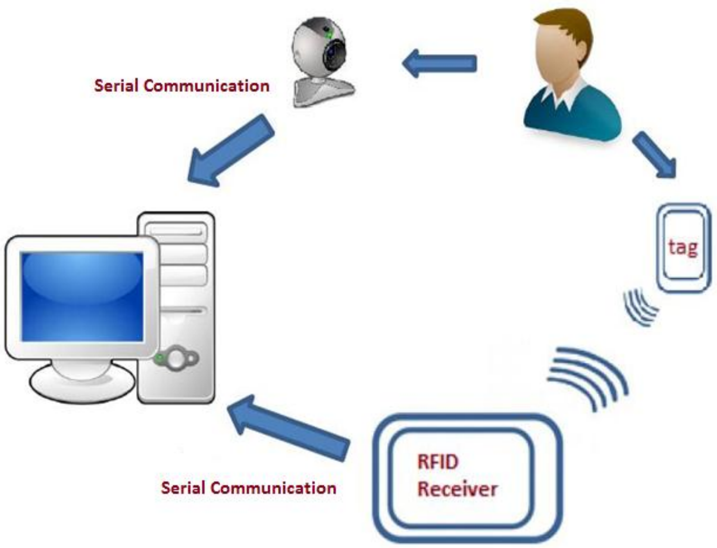

FIGURE 1 TOP LEVEL BLOCK DIAGRAM

The product design consists of three main sub-systems: The RFID reader, the camera and a software program. Due to time and budget constraints, the project will not be in its compact and ready to market form. All three parts will be separate but connected through USB cables. A computer will be used instead of a microprocessor and a web camera will serve instead of an integrated camera.

All students will have to scan their personal RFID tags. The unique ID is associated with the student account saved on the database. For the scan to be completed, the RFID reader will continuously transmits a 125 KHz carrier signal to power the passive RFID tag. After receiving the information from the tag, the receiver digitizes it and transmits it to the computer through a USB cable. The software solution will be responsible for extracting information related to the tag from the database. A picture of the student will appear on the screen. After scanning his or her card, the student will have to stand directly in front of the camera with a clear background (i.e.: no interference from any other person).

The software program will be an executable file that will be launched by the user. Due to time constraint, the picture will not be captured automatically after reading an RFID tag. A bottom will be displayed on the screen to allow the user to take a picture. The captured picture will be saved on the database and displayed on the screen. The picture associated with the student saved on the database will be compared to the one captured by the camera. Image processing techniques will be used for comparison purpose. The user will be notified if an incompatibility occurs. The user will have the choice to either decline if the system fails or to proceed if the pictures do not actually match.

3 Overall system design

This section of the document provides a general overview of our Attendance system entire design. Further description and specification of each component are outlined in details in their respective sections

3.1 Hardware

Secure Com Solutions will design and implement the RFID reader circuit. We designed our own circuit for simplicity purpose and to make the product customized to our needs. It is also more affordable for the purpose of this project. Mainly the RFID system consists of two main units:

1) The Reader
    a. Transmitter
    b. Receiver
2) The Passive tags

The Reader component is the main frame of the RFID system. The transmitter will generate low frequency (125 kHz) signal constantly using the antenna [1]. The antenna will also detect the signal from any tags present in its field. It will then filter and decode the signal and sent the unique ID to the host computer.
For the purpose of the project since we only need to identify the students based on their unique ID card a simple passive tag is sufficient. Also these tags are powered by the transmitted signal from the Reader, so the distance to the reader is limited to a small range [1] and this also provides for one of a requirement of the design functionalities for this project. The host computer is provided with the ID number of the tag from the reader. The computer will then use this number and compare it to all the ID numbers of the students registered in the class. The figure below is the block diagram of the RFID system overview.

3.2 Software

The software part of the system consists of three major parts:

1) Camera
2) Application
    a. User Interface
    b. A customized code based on OpenCV source code for face detection and face recognition
3) Database

The main part is the application which will interact with both the camera and the database. The login page will be displayed as soon as the user launches the application. After logging in the user will be asked to enter the class and the event information. The student will be asked to get a photo as soon as he scans his RFID tag. A rectangle will be displayed in the console of the camera indicating face detection. The captured image will get preprocessed first by converting the color image to greyscale then histogram equalization will be applied to standardize the brightness and contrast. The pre-processing stage is essential for accurate results. After this stage, the database will get accessed for face recognition. The captured image will be compared to the images saved on the database. The database that will be used is MySQL.

4 Hardware Design

4.1 RFID reader

4.1.1 RFID Transmitter

RFID transmitter provides the RF signal which will trigger the passive tag in the range to extract its stored information. This unit encompasses four major subsystems: Power Supply, Clock generator, Power Amplifier, and the Antenna.
The following figure shows the block diagram of the Transmitter.

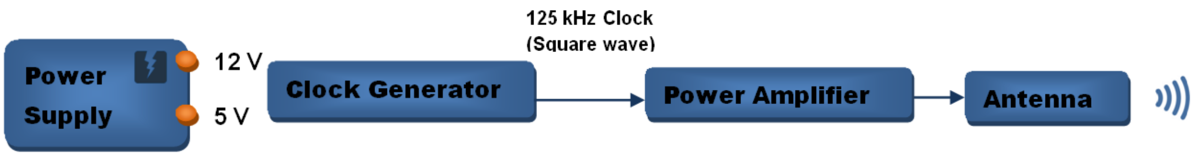

FIGURE 2 THE TRANSMITTER BLOCK DIAGRAM

Power supply

The Power Supply provides the power to derive the whole reader unit. The unit will require a 5 volts DC voltage for the receiver circuit (discussed later on) and a 12 volts DC voltage for the clock generator and the amplification stage. Hence the power supply was designed so that it will use two regulators to provide the required power for the circuit. This is sufficient for the design since the circuit has low power requirement and can easily be designed so that it portable. Figure 3 below shows the design of the Power Supply circuit.

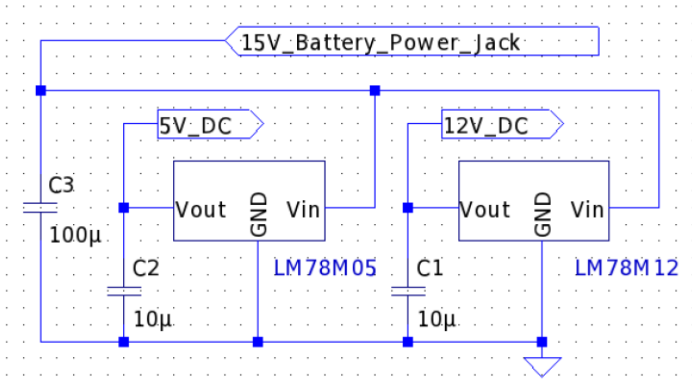

FIGURE 3 POWER SUPPLY CIRCUIT

Clock generator

Since the PIC16F88 has an internal 125 kHz clock, at first it was attempted to use this clock for generating the clock. This could have minimized the circuitry and the costs. But unfortunately it was creating bugs with using the same clock for the receiver decoder program. Hence the circuit that will generate the low level 125 kHz square wave is as shown in figure 4. The generated signal will be a square wave that will later be converted to a sine wave. To make the design more affordable a 555 timer was used to generate the signal. The design will follow an astable multivibrator circuit design to produce a 50% duty cycle 125 kHz square ware. The following calculations show how the capacitor and resistor values were calculated.

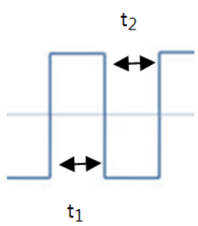

FIGURE 4 THE SQUARE WAVE SIGNAL

Following the astable mulivibrator formula [2] the period of each half wave is:

$$t = \ln(2) \times RC \qquad (1)$$

Hence in circuit shown in figure 5,

$$t_1 = t_2 = \ln(2) \times R_1 C_1 \qquad (2)$$

$$T = t_1 + t_2 = 2\ln(2) \times R_1 C_1 = \frac{1}{f} \qquad (3)$$

Choosing a 1nF capacitor, it follows that,

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$$R_1 = \frac{8\times10^{-6}}{1.368\times1\times10^{-9}} = 5.77\ k\Omega \qquad (4)$$

R_2 is a pull-up resistor; the purpose of this resistor is to ensure that the digital output voltage level at OUT pin closely approximates VCC. R_1 needs to be at least 10 times of R_2, so it was chosen to be 100 Ω. The C_2 is a bypass capacitor on the unused voltage control output. It was chosen to be 100 nF for convenience of the design.

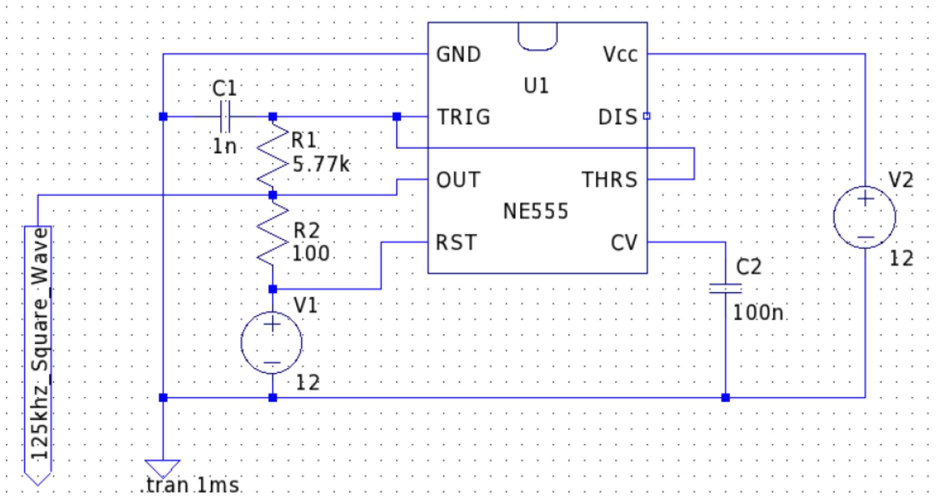

FIGURE 5 CARRIER FREQUENCY CLOCK GENERATOR

Power amplifier and antenna

The last component of the transmitter is the power amplifier and the antenna. First the square wave signal generated from the clock will be converted to sin wave using an RL circuit. The next stage includes a power amplifier.

As by the FCC regulations Part 15 of Title 47 for a 125 kHz signal the signal level needs to be at 64 dB A/m at 10m[3]. Since the distance we require is within centimeters the power amplifier is designed so that it will amplify the sinusoid signal within the regulation limits. The circuit below, figure 6, shows the full design using PNP and NPN transistors that will amplify the signal [2].

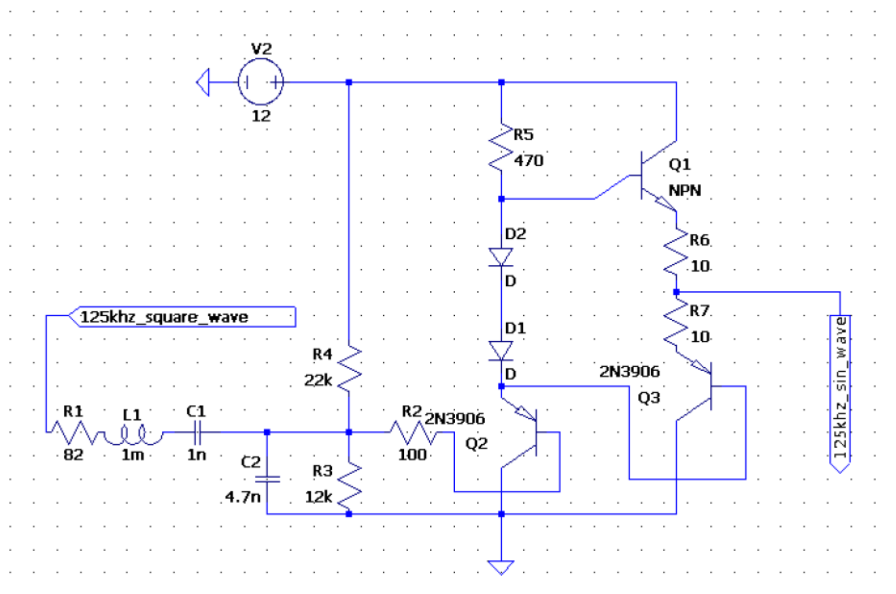

FIGURE 6 SCHEMATIC OF POWER AMPLIFIER AND ANTENNA

Resonant Antenna Design

The RFID passive tags require induced AC voltage to power up. The antenna circuit that will induce this voltage to the tag is of great importance in the antenna design. For this purpose the series LC circuit was chosen to accomplish the resonant frequency. The following equation was used to calculate the inductance needed from the antenna [4].

$$f_0 = \frac{1}{2\pi\sqrt{LC}}, \qquad (5)$$

f_0 is the resonant frequency, L is the inductance, C is the capacitance.
To achieve the 125 kHz resonance frequency, using a capacitance value of C = 1nF.

TABLE 1 LC CIRCUIT CHARACTERISTIC

Capacitance	1nF
Inductance	1.62mH
Frequency	**125kHz**

The reason for choosing these values highlighted in table1 is first achieving smaller values of inductance would require more copper wire and also it will reduce the accuracy. Hence the 1nF capacitance was chosen to attenuate the value of the inductance.

To design the antenna size and shape to achieve the desired inductance the following was considered. The calculation for the inductance of the coil is subject to the different shape of coil such as circular, rectangular, square with single or multi-layer. The rectangular shaped antenna coil was chosen since it will be compatible with the shape of the PCB. This will make casing the final design much easier as well. The following equation shows the inductance of the multilayer rectangular loop coil using the values of the Capacitor and the dimensions of the PCB.

$$L = \frac{0.0276(CN)^2}{1.908C+9b+10h} \tag{6}$$

N is the number of turns, x is the width of coil, y is the length of coil, b is the width of cross section, h is the height (coil build up) of cross section, and C = x + y + 2h [1].

TABLE 2 PCB BOARD AND COIL CHARACTERISTIC

Width (x)	3.5 cm
Length (y)	13 cm
Height (h)	1 cm
Width Cross (b)	0.5 cm
Number of turns	**92**

4.1.2 RFID Receiver

For the purpose of this project it was decided to use the HID lab cards provided by SFU for engineering labs. The information on these cards is stored in FSK format, which the design of the receiver will depend on. The ‘0’s and ‘1’s of the ID number are represented by two different frequencies.

TABLE 3 ‘0’&’1’ FREQUENCY REPRESENTATION

‘0’	12.5kHz	$\frac{f_c}{10}$
‘1’	15.625kHz	$\frac{f_c}{8}$

f_c is the carrier frequency of 125 kHz [1][4]. To recover the data the detected signal from the antenna will go through three stages.

The filtered data will be fed to a microcontroller for decoding. The final step is to transfer the data to the computer for further processing. The following Block diagram shows these stages.

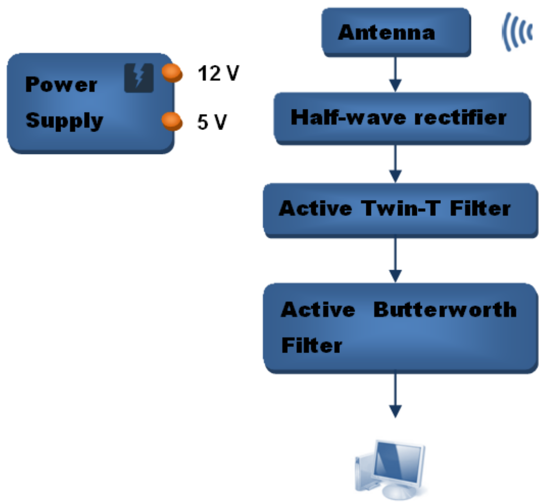

FIGURE 7 BLOCK DIAGRAM OF THE RECEIVER

The half-wave rectifier

As shown in figure 8 C_1 is grounded, this will cause resonant frequency (125kHz) of the signal received through the antenna to be filtered. The half-wave capacitor-filtered rectifier circuit is used to drop the negative part of the received signal. D_1 is used to detect the peak voltage of the signal and the RC filter circuit is to detect the signal envelop. The values for this section are chosen to be R_1=390kΩ and C_2=2.2nF so that the RF filter detects the correct frequency [1].

Active twin-T filter

The rectified signal is then fed to a band-pass filter to drop any frequency other than the range that has the information (10-20 kHz). This is achieved by the Active Twin-T filters as shown in figure 8. This filter also sets the signal's gain at unity [1][4].

The last stage that the signal goes though before the microcontroller, is an Active Low-Pass Butterworth filter. This filter will then amplify all lower frequencies and drop 125 kHz frequency [4].

Butterworth Filter

The filtered signal will be outputted to the PIC16F88 microcontroller. The microcontroller will

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then decode the signal and provide the computer with the student information transmitted from their RFID tag.

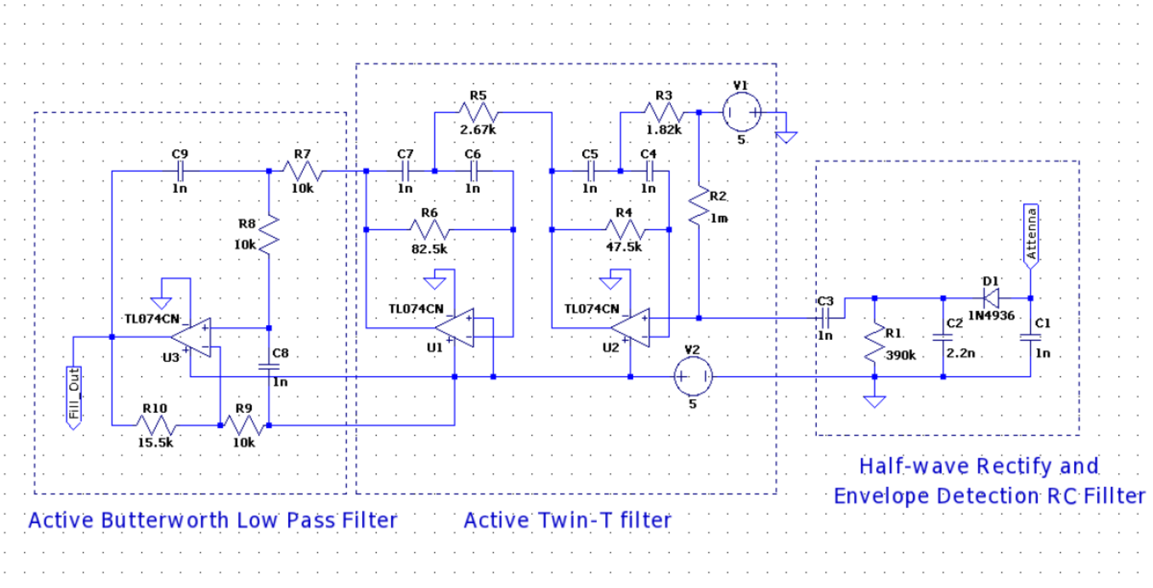


FIGURE 8 ENVELOPE DETECTOR AND FILTERS

Microcontroller

The PIC16F88 microcontroller is used to perform data decoding. It was chosen since it has all the functionalities required without being excessive for the design. It was also very cheap. It was programmed using a “Mini USB PIC Programmer”. The software used for programming is MPLAB and PIC kit 2, since they are compatible with the hardware. It is programmed in Assembly.

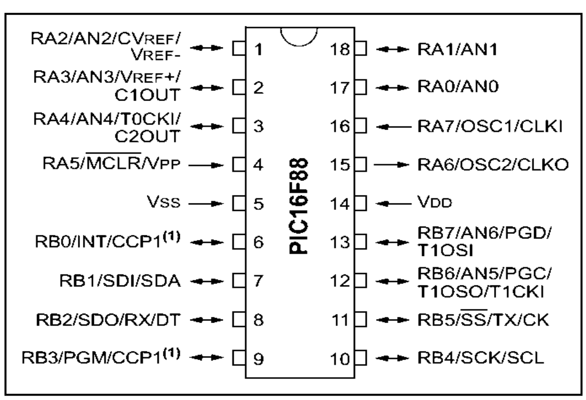


FIGURE 9 PIC16F88 CONFIGURATION [6]

The functionality of the microcontroller is to decode the received FSK modulated data, and then out putting the ‘0’s and ‘1’s to the computer through an RS-232 serial interface for later processing.

The internal RC oscillator can be configured to use the 125 kHz frequency by setting the bits in register 4-2 of the microcontroller (OSCCON) [6]. Port 18 is used as the analog input port, and port one for the comparator input. The microcontroller also has an internal comparator that will compare the analog input to the reference voltage (Register 9-1: CCP1CON), in other words it will convert the analog signal to a digital signal.

The HID data format has a header bit that specifies the beginning of the ID and a finish bit that specifies the end of the information bits. It has 26 bits, from which bit 2-9 represent the company code (in this case SFU) and bits 10-24 represent the unique user ID [7]. This will give us 255 possible facility codes and 65,535 possible card codes which will be more than enough for any Educational institute.

4.2 RFID tag

Choosing the Tag was the simplest, Secure Com Solutions decided to use the SFU Engineering Labs ID cards to minimize the costs. As mentioned the formatting of the cards’ information is 26 bit unique ID number (section 3.2.2.d) which serves well with the reader design.

5 Software Design

5.1 Face detection

The method used for face detection is Haar Cascade. The features used are based on Haar wavelets. The actual rectangles used are Haarlike features.

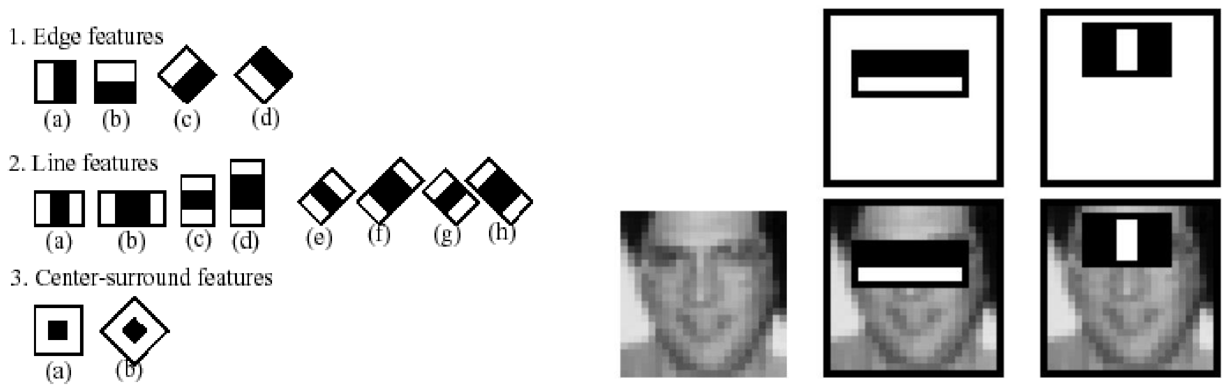


FIGURE 10 HAAR FEATURES

The concept is to choose a scale of the feature typically 24x24 pixel window. Slide the window across the image. Calculate the difference of the average of the area under the white region and the average of the area under the black region. If the difference is above some threshold then the particular feature matches the data underneath it.

Summing pixel values, calculating the average and computing the difference for every feature is expensive and time consuming.

The solution to this problem is “Integral image” or “summed data table” which is created in a single pass across the image.

This method works by adding the pixel values. The integral value of a pixel is the sum of all the pixel values above it and to its left starting at the top left corner of the image

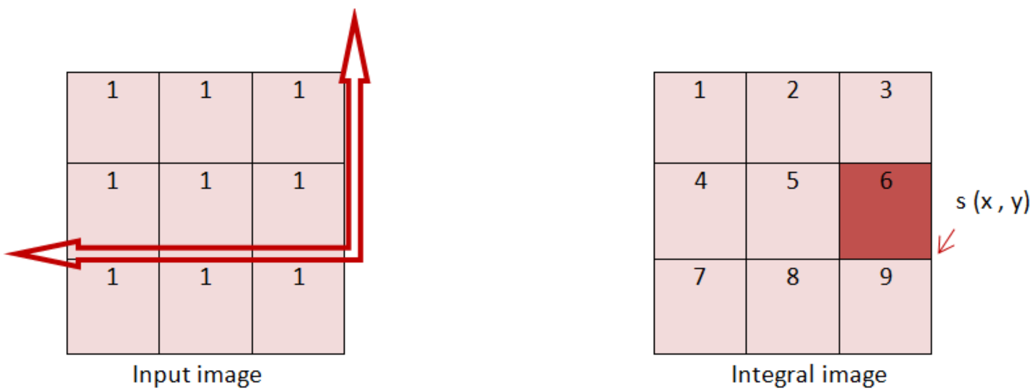
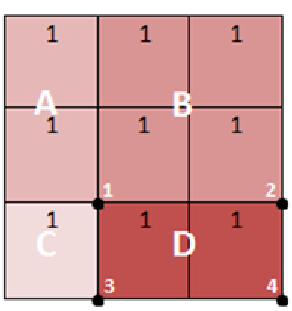


FIGURE 11 INPUT-INTEGRAL IMAGE ILLUSTRATION

Integral image allows for the calculation of sum of all pixels inside any given rectangle using only the four values at the corners of the rectangle as shown in figure 12.



D = 1 + 4 –(2+3)
= A+ (A+B+C+D) - (A+C+A+B)
= D

FIGURE 12 INTEGRAL IMAGE CALCULATION

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To select the specific Haar feature to use, an to set threshold levels AdaBoost method is used. Adaboost is a mchine learning algorithm which helps in finding only the best features among all the 160,000+ featurs. A weighted combination of the selected features is used to evaluate and decide whether any given window has a face. AdaBoost tries out multiple weak classifiers in each round and combining the best weak classifiers to create a strong classifier.

Figure 13 shows how a series of AdaBoost classifiers construct a filter chain.

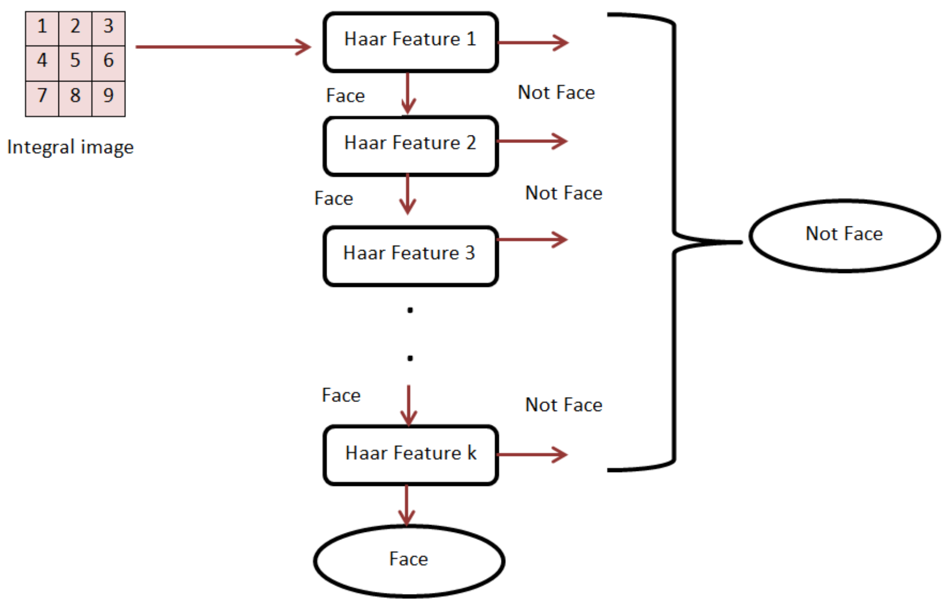

FIGURE 13 FACE DETECTION ADABOOST FILTER

5.2 Face recognition

The most common and simple method for facial recognition is Eigen face based face recognition. Eigen face consists of two phases: learning and recognition. During the learning phase, one or more face images of each person are provided. The set of images is called the training images. In the recognition phase, the name of the person associated with the training image that is closest to the new image is returned.

The set of Eigen faces is generated using a mathematical process called principle component analysis.

The face recognition process is as follows:

An example of a training set of M images is showed in the figure 14. All the images must have the same size (NxN).The images are converted into vectors.

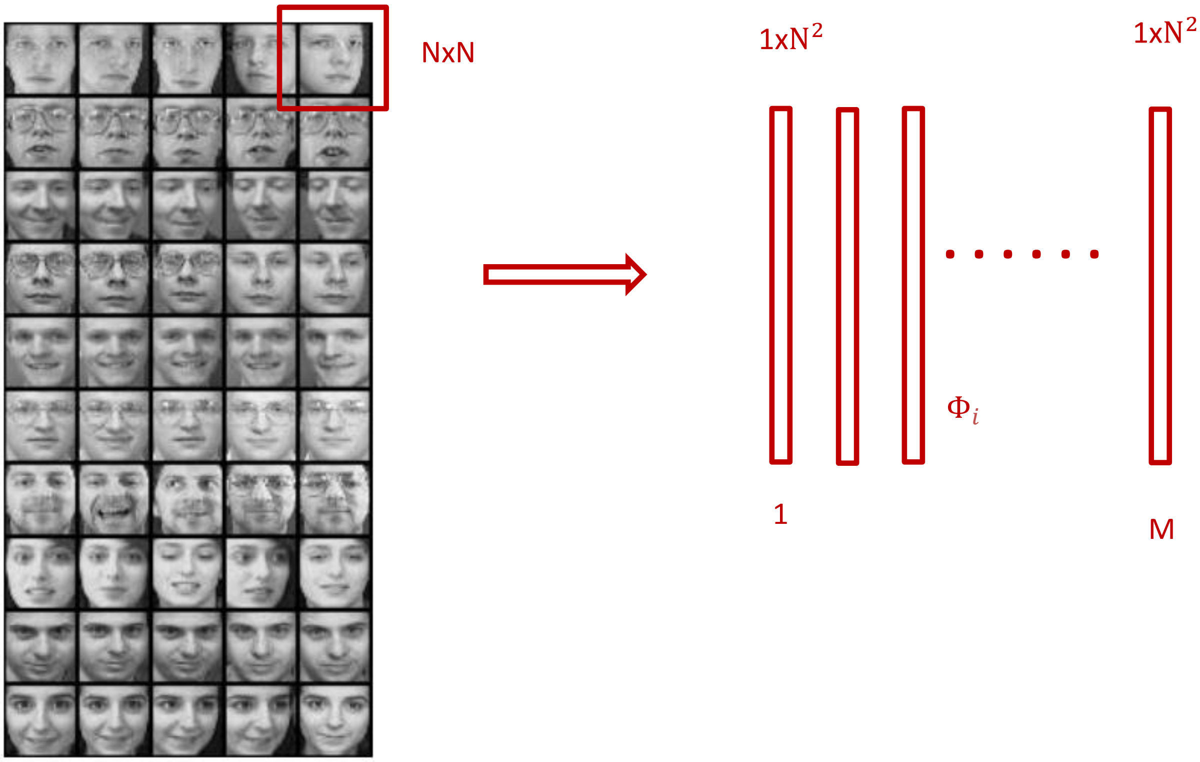

FIGURE 14 TRAINING IMAGES

Next the face vectors are normalized by removing all common features that all images share. The common face vector ψ is calculated as shown by equation (7).

$$\psi = \frac{1}{M} \sum_{i=1}^{M} \Gamma_i \qquad (7)$$

FIGURE 15 MEAN EIGEN FACE

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Normalized face vectors are obtained by subtracting the average face ψ from each face vector

$$\Phi_i = \Gamma_i - \psi \quad (8)$$

FIGURE 16 EIGEN FACES

To calculate the eigenvectors, the covariance matrix C needs to be derived.

$$C = \frac{1}{M} \sum_{i=1}^{M} \Phi_i \Phi_i^T = AxA^T \qquad \text{where } A = [\ \Phi_1, \Phi_2, \ldots, \Phi_M\ ] \quad (9)$$

Since A is N^2x M, C will be of N^2x N^2 dimension.

Example:

N = 50 => N^2 = 2500

C will contain 2500 eigenvectors each 2500 x 1 dimension.

This huge number might cause the system to run very slowly or might cause a memory problem. To reduce dimensionality principle component analysis (PCA) is used. Eigenvectors are calculated from the covariance with reduced dimensionality.

$$C' = A^T x\ A \quad (10)$$

C′ represents the lower dimension subset of C.

The next step in training the recognizer is to select the K best Eigen faces such that K < M and the K Eigen faces can represent the whole training set.

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The selected K Eigen faces must be in the original dimensions. A mapping needs to be done to get back to the original domain after calculating the eigenvectors ν_i corresponding to the K eigenfaces.

$$\mu_i = A \times \nu_i \quad (11)$$

μ_i is the corresponding eigenvector in the original dimentionality.

By this method we did not only save computation and memory usage but also reduce the effect of noise since only the K most important Eigen faces have been selected.

Once we have the Eigen faces, we can represent each image in the training image set by a linear combination of the Eigen faces added to the average face as shown in figure 17.

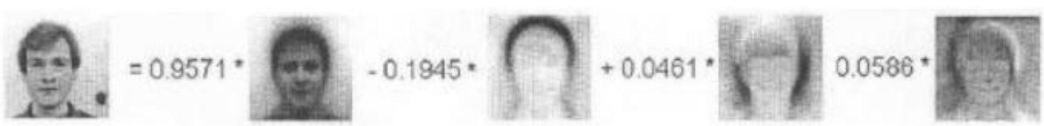

FIGURE 17 FACE RECONSTRUCTION

$$\widehat{\Phi_i} = \sum_{j=1}^{K} \omega_j \ \mu_j + \Phi_i \quad (12)$$

The coefficients shown in figure 17 represent the weights ω_j associated with each Eigen face. The weight is the contribution of each Eigen face to represent a particular image in the training set images.

The weight vector can be represented as follows: $\Omega = \begin{bmatrix} \omega_1 \\ \omega_2 \\ \cdots \\ \omega_k \end{bmatrix}$

At this point the recogniser is trained and ready to recognize new faces. An unknown input face is then introduced. The image goes through the same processing stage to map the image to the Eigen space.

The flowchart below represents the overall recognition algorithm; the process phase is also applied for training set but not illustrated in the flowchart.

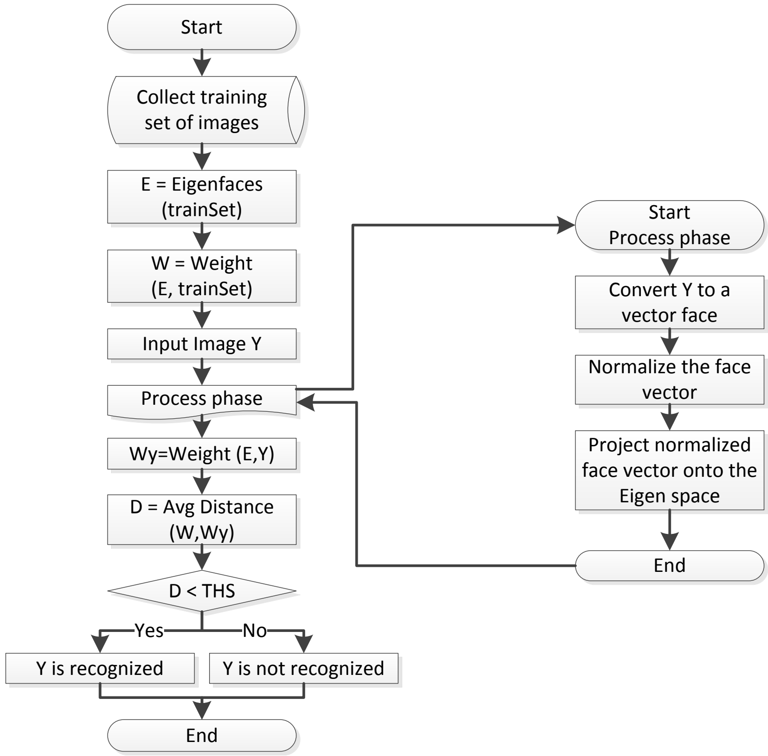

FIGURE 18 FACE RECOGNITION FLOWCHART

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6 User interface

6.1 Hardware

An LED will serve as indicator of the status of the RFID reader. The following table summarize the different LED status

TABLE 4 RFID READER INTERFACE

LED status	Reader status
Red	The reader is idle, nothing detected
Flashing red	The reader is processing a card
Green	Card successfully processed
Flashing red & green	Card unsuccessfully processed

6.2 Software

Our main image processing application is implemented in MVS 2010 so we decided to design the GUI with Windows Form Application tool available via MVS 2010. The final project will be built into an executable format.

Figure 19 shows a mock-up screen of the login pages. These mock-ups are for illustration purpose only but do not represent the final GUI design.

FIGURE 19 MOCK-UP SCREEN

The design is intended to be simple to be able to later upgrade the solution to portable devices.

Depending on the need, the next screen would be different.
For Example, in a final exam case, the student photo and information will be displayed as soon

as students scan their ID. For a simple attendance case, we will confirm that the student is enrolled in the class.

7 System test plan

The main idea behind the test plan consists of testing the individual parts separately on the first stage for a unit test. Then merge all modules together step by step for a final test. Therefore all modules functionality is validated through a unit test and the system functionality is verified through a final test.

7.1 RFID reader

To verify that each part of the circuit meets the specified requirements, we use electronic test equipment as voltmeters, oscilloscopes...

1. Power supply
   - The 5V DC output should be 4.8V to 5.2V
   - The 12V DC output should be 11.5 V to 12.5 V
2. clock generator
   - The output should be 125 kHz square wave with 12 V DC Vcc input
3. Power Amplifier and Antenna
   - The output should be 125 kHz sinusoid wave with 125 kHz square wave input
4. The inductance of the Resonant Antenna Design circuit should be 1.62mH

We will fine-tune the circuit until we see the highest resonant voltage form our carrier frequency.
The reader's size should not exceed 15cm x 10cm; as defined in requirement specification [R26-B].

After we assure that the circuit behaves as specified in theory, we will try to detect the tag and transfer information associated with it to the computer.

- Given the distance constraint to assure no interference from other tags, the RFID reader needs to be tested with different distances. Based on our requirement specification [R23-B], the reader should read the tag within 10 cm.
- Another tag will to be introduced at the same time. The RFID reader needs to detect only one tag at a time.

- Once the detection stage is done, the transfer stage will be tested.
  A USB port will be connected to the circuit. Using a USB cable, data will be transferred to the computer. The number read should match the unique number associated with the tag.
- We also will test the read time. Based on our requirement specification [R21-A], the reader needs to read the data in less than a 0.5s. We will test the read time with putting the tag in 2cm, 4cm, 6cm, and 10cm with 5 times for each position. We will test the accuracy of the system. We will put the tag in different range, put two tags in the range and the two tags with fixed distance, or put another electronic device within the range. Around 5 to 10 different tags will be tested.

7.2 Software system and image processing

The purpose of this module is to receive the incoming information, retrieve data from the database and compare two pictures. To be efficient the image processing will be implemented and tested in parallel with the other software parts. Once every part is working, the integration phase will be done and testing will be conducted.

1. Face detection:
   - The algorithm will be tested to detect the face on pre-loaded images and an image taken with a webcam.
   - Different people will take part of the tests and different position & lighting condition will make the test cases.
   - The algorithm will handle one face per picture as discussed in our requirement specification [R41-A]
2. Face recognition
   - Face recognition is related to the previous module. Once the face is detected the system will try and identify the person.
   - A pre-loaded picture will be stored in the computer and the algorithm should be able to identify the person.
   - Different persons will take part of the test and this iteration is repeated to identify different persons.
3. The software solution – Database and information retrieval
   - A database will be created and filled by some random information for testing purpose. The first testing step after that is to make sure that the connection between the program and the database is secure and reliable.
   - Once the connection is made, a random number with the same format as the tag number will be used to access the database.

- The second step will be to store an image in the database and to retrieve it using the same number.

4. The software solution – Add image processing
    - After retrieving information, a person will try to be identified. A wrong person and the real person will take part of the test.

As soon as we assure that the system is working properly, the GUI will be taking care of. All feedback messages will be displayed to the user on the screen.

7.3 System test plan

As a final test, all parts software and hardware will be combined and extensively tested. The information received form the RFID reader will be used to access the database and the picture captured by the camera will be saved. Once reading information from both the RFID reader and the database is guaranteed to be working properly, reading from the camera will be tested. An alternation between reading the tag information and capturing a photo needs to be respected.

Multiple scenarios will be experienced to ensure that the algorithm works properly and meets the requirements.

- Student scans the RFID tag , then gets a picture from the camera
- Student scans the RFID tag and another person scans another RFID tag
- Student scans the RFID tag , then gets a picture from the camera and another person gets a picture without scanning the tag
- Student scans the RFID tag and another person gets a picture from the camera
- More than one person scan their tags at the same time

In all the above scenarios the system should detect the acceptable from the unacceptable scenario and give feedback to the user. Once everything is working properly, system improvement and optimization will be taken into consideration.

8 Conclusion

In design document, we clearly and concisely described the design specifications of our automated attendance system. Furthermore, these design choices will help Secure Com Solutions' engineers to fulfill the A requirement in the functional specifications, resulting in a prototype device.

Through the design specification, we provide clear goals toward the completion of each requirement.

The proof of concept device is well under development and we are confident that the final product will be complete by April 25 as initially planned.

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