ELECTRAUDIO

March 13th, 2014

Dr. Andrew Rawicz
School of Engineering Science
Simon Fraser University
8888 University Drive
Burnaby, British Columbia
V5A 1S6

Re: ENSC 440 Design Specification for SoundSocket, an Innovative Audio Transmission Solution

Dear Dr. Rawicz,

The enclosed document contains the design specification for SoundSocket, a novel product that uses power line communication to transmit audio signals. The objective is to create a device that will provide quality audio transmission utilizing existing power lines, effectively eliminating the need to set up alternative wiring schemes or rely on wireless communication.

The design specification provides the necessary information and specifications for the SoundSocket system and all of its components. It contains a detailed discussion of the justification for the design decisions that were made to meet the required functional specifications. The system test plan and future design considerations are presented. This document will be utilized by our team to aid in the development of the product and efficiently implement a proof-of-concept model for demonstration.

Electraudio was founded by five innovative and dedicated senior engineering students: Josh Ancill, Andy Cheng, Daman Dhillon, Kim Izmaylov, and Laura Wiggins. If there are any questions or concerns regarding the proposal, please feel free to contact us via email at kvi@sfu.ca.

Sincerely,

Kim Izmaylov
Electraudio

Enclosure: *Design Specification for SoundSocket Power Line Audio System*

Design Specification for **SoundSocket** Power Line Audio System

Josh Ancill
Andy Cheng
Daman Dhillon
Kim Izmaylov
Laura Wiggins

1 Abstract

This document provides the design specifications for Electraudio's Sound Socket powerline audio transmission system. The four different modules are presented and discussed in detail: the Audio Processing, the OFDM, the RF and the Isolation/Coupling module. Audio Processing module, consisting of a Nios II processor and VHDL-generated hardware, receives analog audio and converts it to a suitable digital format. The OFDM module is VHDL-generated hardware that uses OFDM to modulate the digital data onto sub-carriers. The RF module receives these sub-carriers and modulates them onto a 6MHz carrier. The Isolation and Coupling module receives the RF-modulated signal and couples it to the mains power lines while protecting the circuitry from 60Hz power signal. The same process applies backwards on the receiving side which allows analog audio to be recovered from an outlet on the same mains power lines. This document also describes a test plan to be applied to test the functionality of the individual modules as well as the system as a whole. It is written in a manner intended for an individual with background in electronics and programming.

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Glossary

The definitions given here are given according to the context they are used in and are intended for clarity. They may differ slightly or be incomplete compared to lengthy official definitions.

60Hz power signal	120V RMS (B.C. Hydro) signal from the mains power lines
ADC	Analog to digital converter
CODEC	Coder and Decoder
DAC	Digital to analog converter
Data signal	Signal containing useful data (as opposed to power)
DFT	Discrete Fourier Transform
DSB	Double side band (referring to modulation technique)
FDM	Frequency Division Multiplexing
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
Galvanic Isolation	Isolation of circuit elements to prevent direct current flow and separate “ground” references
ICI	Inter-channel interference
IFFT	Inverse Fast Fourier Transform
ISI	Inter-symbol interference
ISR	Interrupt Service Routine
LED	Light Emitting Diode
Line-level	A signal power level standard; typical output power for use with ear phones.
Loop back test	Reading the input signal and outputting it (with no change to the
LSB	Least Significant Byte
Mains power lines	General purpose 120V household power line
	signal) to test the basic functionality of internal modules
MSB	Most Significant Byte
OFDM	Orthogonal Frequency Division Multiplexing
Overvoltage	Voltage levels that exceed the allowable voltage levels on a circuit line/node.
PAPR	Peak to Average Power Ratio
PIO	Parallel Input/Output
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
Reactance	Component of impedance corresponding to capacitors and inductors
SDRAM	Synchronous Dynamic RAM (type of Random Access Memory
Vss	Supply Voltage (typically for buffers and op-amps)

2 Introduction

SoundSocket, an innovative product from Electraudio, is an audio system which utilizes the concept of power line communication to transmit an audio signal, avoiding the need to rely on wireless technology or external wiring and the cumbersome setup associated with it. With SoundSocket, the user simply plugs the transmitter unit into a wall outlet and may utilize another outlet as both the audio and power source for the receiver unit. SoundSocket is a robust and reliable product that delivers CD quality audio.

2.1 Scope

This document describes the design requirements and specifications that must be met by the product. It contains detailed information pertaining to the specific design choices that were necessary to ensure that the prototype meets the specified proof-of-concept requirements. Unless specified otherwise, the design specifications apply to the proof-of-concept only. Each component of the overall SoundSocket system is discussed and justifications for the various design requirements are given. A system test plan is outlined, and it provides the template against which the product performance will be evaluated.

2.2 Intended Audience

This documentation is intended for use by all Electraudio members throughout the product development process, and it can be utilized as a guideline for the implementation of the proof-of-concept model. The test plan included in this document will be used as a guide to evaluate the performance of the proof-of-concept model.

2.3 Background

Today, more and more companies are using wireless technologies to reinvent existing products so as to empower them with portability. Conversely, the number of devices on the allowed frequency spectrums (2.4/5GHz) of home devices has increased tremendously [1]. This has a large and noticeable impact on performance in areas saturated with wireless devices, which one can sometimes easily notice in public WiFi networks or at home when a family member is streaming a high definition video, just to pull a few examples. Electraudio's SoundSocket Power Line Sound System provides a smart and elegant solution by providing an audio streaming or transmitting device which offers the portability of a wireless counterpart, and the stability and performance of a wired device by using the existing power lines in a building to transmit audio.

3 System Overview

SoundSocket is comprised of multiple independent modules which will be interconnected to form the complete prototype device. The prototype will be built out of four major modules, the first of which, the audio processing module is implemented on the DE2-70 FPGA board. The second major module is the OFDM modem with the necessary DA/AD converters also implemented on the DE2-70. The third module is the RF modulator which will take the baseband signal generated by the OFDM module and modulate it on a carrier to be transmitted. The final module is the isolation and coupling circuit which acts as the interface to/from the mains and also protects the SoundSocket from the dangerous high voltages. Figure 1 shows the hardware modules and the connections between them.

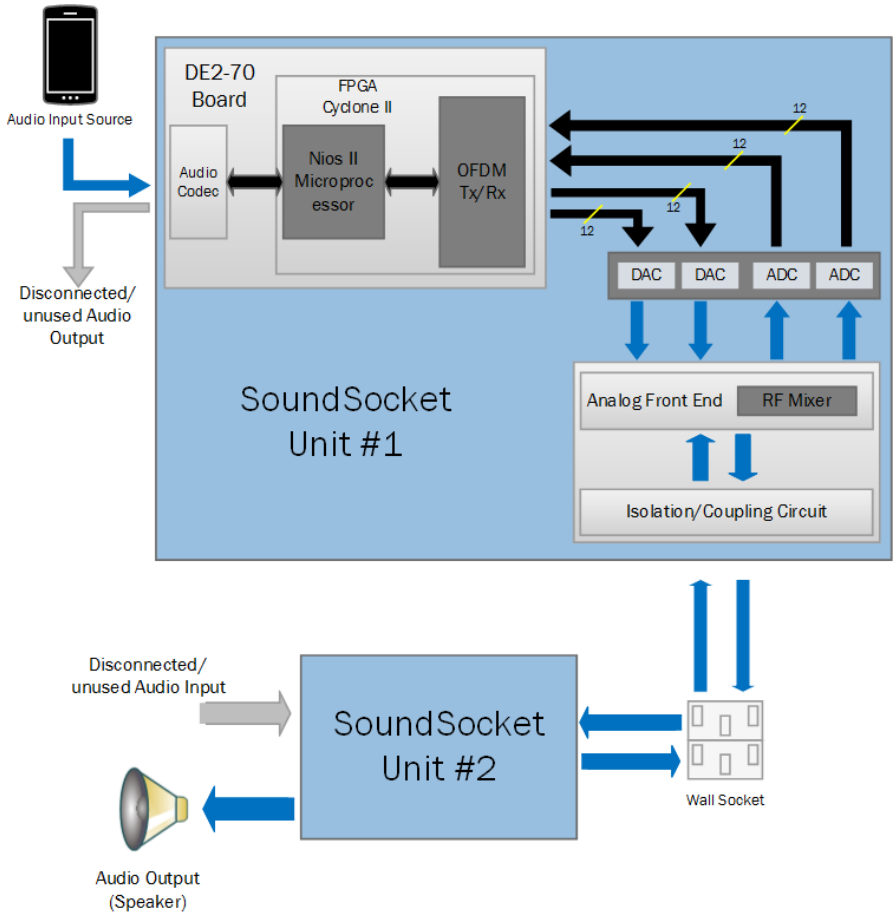

Figure 1: System diagram and interconnections

4 Audio Processing Module

4.1 Background

In the SoundSocket transmitter, the audio processing module is responsible for reading the data in from the audio source, processing and packetizing the data, and passing the data to the OFDM module on transmitter side. On the receiver side, the module will receive data from the OFDM Module, unpack and process the data, and pass it to the audio output source. The audio processing module is implemented using an Altera DE2-70 development and education board. The decision to utilize this board was based on a number of considerations including the specific hardware that is required, the ease of obtaining and working with the board, and the cost of the board. The DE2-70 board contains the peripherals that are necessary to implement the audio processing module, and there is already a familiarity with this board and its functioning because it has been used in previous courses. Financially it is a logical choice due to its availability from the ESSEF parts library at no cost. The module utilizes the cyclone II FPGA to implement a Nios II system and the VHDL circuitry to communicate with the peripherals on the board. The audio processing module is comprised of three sub modules: The Audio CODEC Sub-Module, the Nios II Sub-Module, and the Serialization Sub-Module.

4.2 Audio CODEC Sub-Module

The Audio CODEC Sub-Module is responsible for formatting and passing data between the Audio CODEC Sub-Module and the Nios II Processor Sub-Module.

4.2.1 SoundSocket Transmitter

The input audio signal is applied to the line-in jack on the board and must be passed through an analog to digital converter to enable the digital signal processing to occur. The Wolfson WM8731 audio CODEC is a low power stereo CODEC with 24-bit sigma delta ADCs and DACs [2]. The CODEC is initialized using an I^2C protocol. VHDL is utilized to design the circuitry implemented on the FPGA that takes the data from the CODEC and passes it to the Nios II Processor Sub-Module. A serial receiver is used to obtain the stereo audio data from the ADC. The data is received as a 32 bit left justified signal, and the relevant 16 bits of audio are extracted and passed to the Nios II Processor Sub-Module for processing.

4.2.2 SoundSocket Receiver

VHDL is utilized to design the circuitry implemented on the FPGA that takes the data from the Nios II Processor Sub-Module and passes is to the CODEC. The audio signal is received from the Nios II Processor Sub-Module as a 16 bit signal. The signal is then formatted into a 32 bit left justified signal by concatenating zeroes to the end of the input signal. Next, the data is passed to the serial transmitter which generates a serial signal to send to the DAC which generates the output audio signal that travels through the line-out jack on the board.

4.3 Nios II Processor Sub-Module

The Nios II Processor Sub-Module is a soft-core 32-bit embedded processor designed specifically for the Altera family of FPGAs, and it is implemented entirely in the programmable logic and memory blocks of the FPGA [3]. The Nios II has a Harvard architecture and a RISC instruction set architecture [3]. Utilizing a soft processor core provides the ability to design a custom system and tailor it to the desired

specification by adding the required components to the system. The Nios II Processor Sub-Module is comprised of a Nios II processor, on-chip memory, an SDRAM controller, and multiple parallel input and output ports.

4.3.1 SoundSocket Transmitter

This part of the audio processing module is responsible for reading 32 bits of audio data from the two 16 bit channels coming from the Audio CODEC Sub-Module. Data is read at clock speed of 50 MHz. Every time the data arrives from Audio CODEC Sub-Module, an ISR (interrupt service routine) is launched to process the data. The ISR concatenates two 4-bit headers and the two 16-bit channels of audio data, resulting in a 40-bit output which is fed to the serialization module.

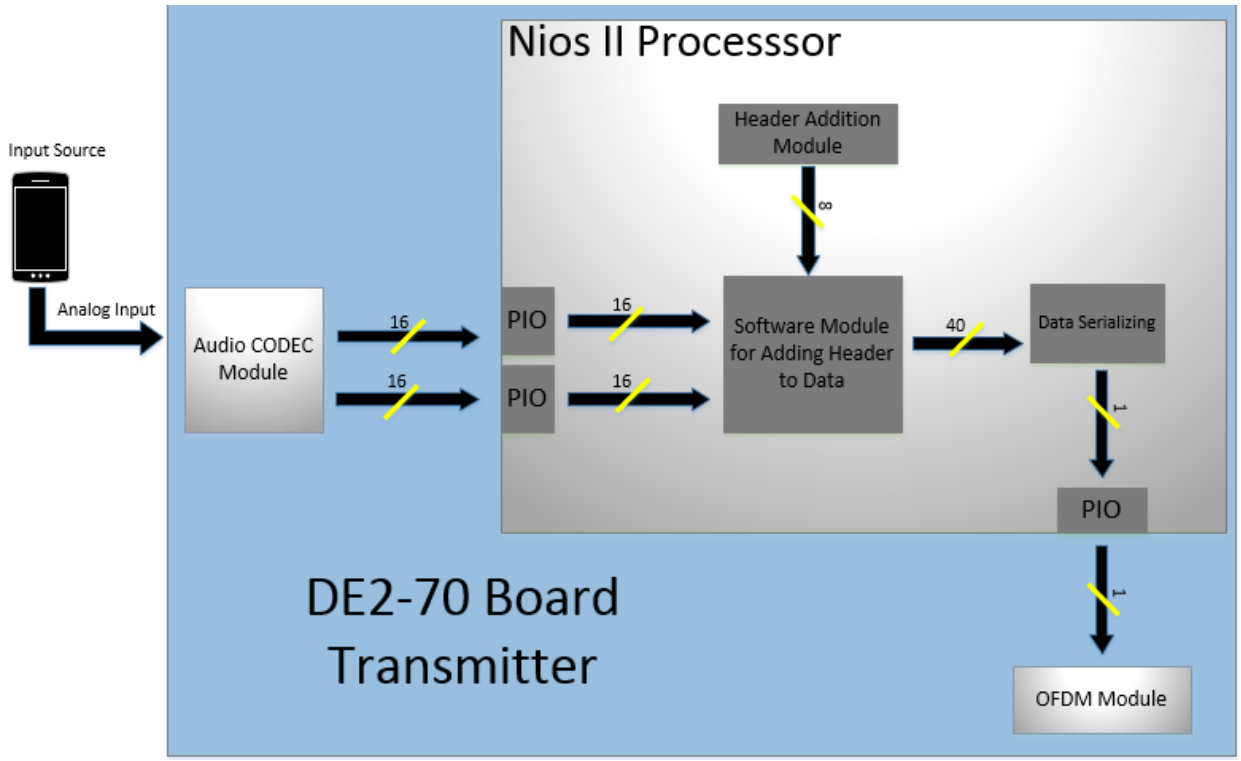

Figure 2: Nios II Processor Sub-Module in Transmitter

4.3.2 SoundSocket Receiver

The receiver has the same structure for the Nios II Processor Sub-Module, but it works in the reverse order. It receives the 40-bit data from the serialization module, detaches both of the 4-bit headers that were present to dictate the cannel, and separates the two 16-bit audio channels. The switches on the DE2-70 board are utilized to select the desired channel to be output. Table 1 provides the switch input values that must be specified to control which channel should be output. The switches on the DE2-70 board are utilized to select the desired channel based on the header data.

Table 1: Header Code to output Specific Channels at Reciever

CHANNEL NUMBER	SWITCH PATTERN
Channel 1	0001
Channel 2	0010
Channel 1 & Channel 2	0011

Following figure explain NiosII Processor Sub-Module in Receiver.

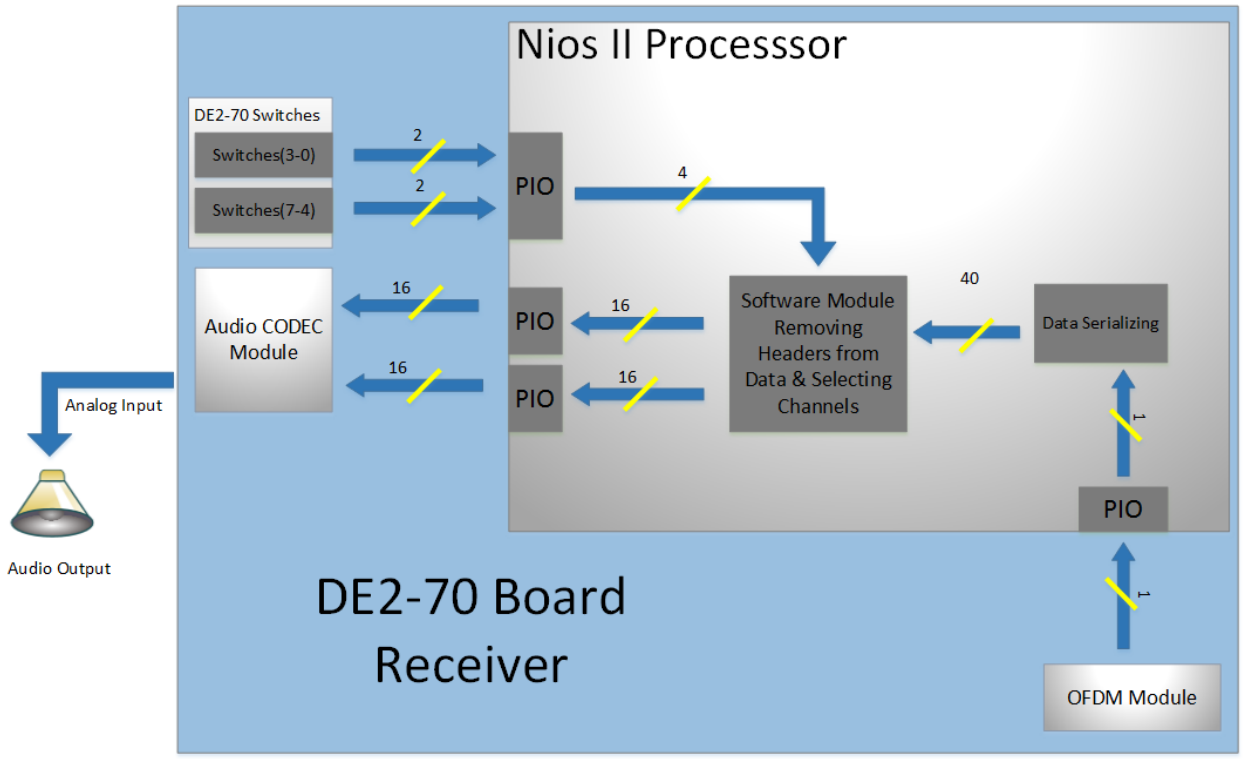

Figure 3: NiosII Processor Sub-Module in Receiver

4.3.3 Serialization Module

In the SoundSocket transmitter, the serialization module receives a 40-bit signal from the Nios II processor, and it produces a serial bit stream that is passed to the OFDM module. In the SoundSocket receiver, the serialization module receives the 40-bit serial signal from the OFDM module and creates a 40-bit parallel signal that is passed to the Nios II Processor Sub-Module.

The specific design of the serialization module is still under consideration. One option would be to include the serialization module in the Nios II Processor Sub-Module. In this option, the serialization would be implemented in a C language program running on the processor. Another possible option would be to design a VHDL circuit to implement the serialization module which would involve the creation of a serial transmitter and receiver.

5 OFDM Transmit and Receive Module

5.1 Background

In our transmitter and receiver devices, we will have two modules which utilize an Orthogonal Frequency Division Multiplexing (OFDM) transmit and receive block respectively. First off, OFDM is based on FDM. Essentially, FDM divides the entire bandwidth available into multiple sub-channels, which can carry streams of data completely independent of other sub-channels. This allows a device to fully utilize the available bandwidth.

OFDM on the other hand further reduces the bandwidth by overlapping signals in such a way that when any given signal at a frequency is being analyzed, all the others are at “zero”. This is described as having orthogonally.

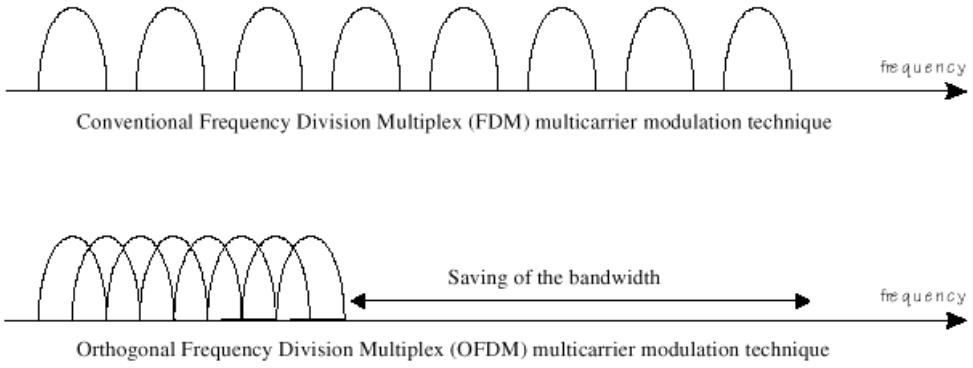

Figure 4: Bandwidth advantages of OFDM over traditional FDM methods

However, there are several other advantages to using OFDM versus single carrier modulation techniques:

1. Efficient use of the spectrum (due to channel overlap)
2. Resilient against Inter-Symbol Interference
3. Resilient against Inter-Channel Interference
4. Uses Fast Fourier Transform to generate orthogonal channels
5. Not as sensitive towards time synchronization errors

Given that we are building our prototype off of the DE2-70 FPGA development board, we have limited bandwidth due to hardware limitations. Therefore, bandwidth efficiency is definitely one of the main desirable attributes of OFDM. Similarly, the inherent robustness in error correction is important as our product aims to provide CD quality audio output at the receiver. Also, the fact that FFT and IFFT

algorithms can be used to generate orthogonal sub channels greatly simplifies the design by reducing the need of multiple I/Q-modulators and demodulators, as will be discussed in the implementation.

Despite the advantages, there are some aspects of OFDM, which, if not handled correctly can result in poor signal transmission. For one, this modulation scheme is highly susceptible to offsets in frequency and phase. This causes the signals to no longer be orthogonal to each other. Therefore it is absolutely critical that the receiver is able to calculate the offset as accurate as possible to prevent any severe loss of orthogonality and the introduction of ICI. Secondly, OFDM produces signals with a relatively high peak-to-average-power ratio (PAPR). This causes problems mainly for the receiver as the peak signals can get cut off if the hardware is incapable of handling a high enough PAPR.

OFDM is actually comprised of a separate modulation and multiplexing scheme, respectively: Quadrature Amplitude Modulation (QAM) and the Discrete Fourier Transform (DFT). QAM is both an analog and digital modulation scheme, but in the case of SoundSocket, we are interested purely in its digital capabilities. Basically, it uses two carrier waves which are out of phase by 90 degrees to describe a unique "symbol" which is a combination of binary bits. The in-phase carrier is denoted by having an amplitude I(t), whereas the out of phase carrier, or quadrature component is denoted by having amplitude Q(t) as shown in the relation below.

$$s(t) = I(t)cos(2\pi f_0 t) - Q(t)sin(2\pi f_0 t)$$

(Cosine and Sine pair are 90 degrees out of phase)

In our design, we chose to use a 4-QAM modulator. 4-QAM maps two bits of data to a unique symbol (a dot on the plot), for a total of 4 symbols (00, 01, 11, 10) as can be seen in Figure 5 below. One can infer from the diagram that you can simply shift the phase 90 degrees to get the next symbol. This is in fact a special case of Quadrature Phase Shift Keying (QPSK).

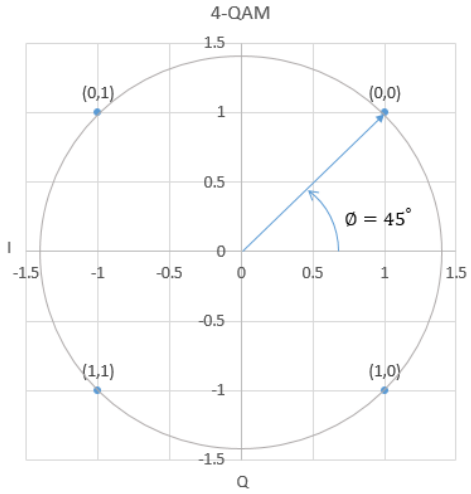

Figure 5: Constellation pattern for 4-QAM modulation

5.2 System Overview

Figure 6 below depicts the overall system diagram of a transmitter and receiver with a bit stream.

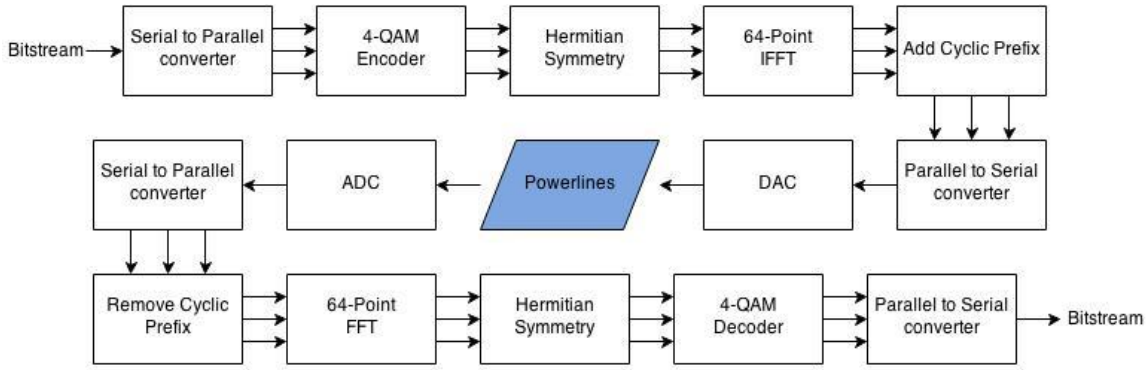

Figure 6: Block Diagram of OFDM Transmitter/Receiver

5.2.1 Transmitter Overview

Looking at the transmitter side only, we step through the process of taking in m-bits where we use m = 62-bits of serial data bits to transmission over the power lines in one OFDM symbol. Figure 7 describes the details regarding traversal of the bits through the various OFDM sub-blocks.

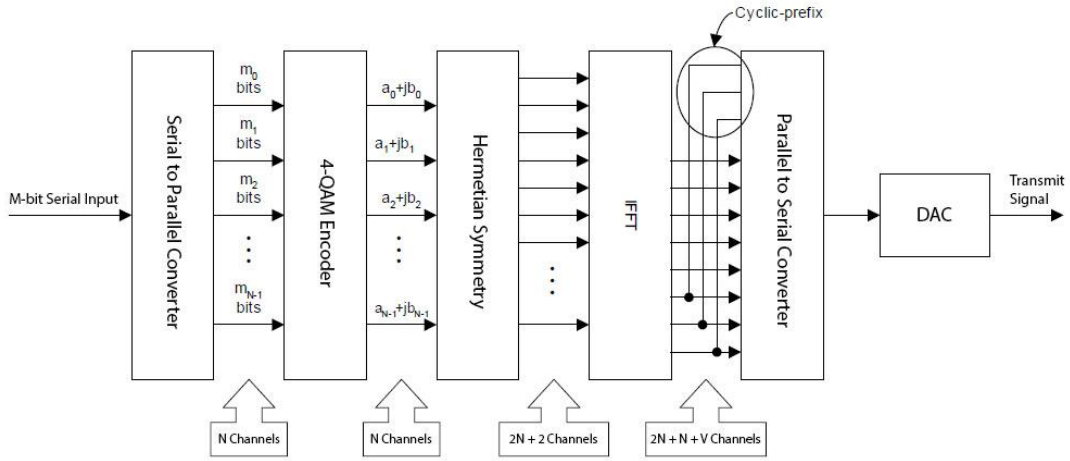

Figure 7: Transmitter Data path [4]

5.2.1.1 Serial to Parallel Convertor Block

First, the incoming bitstream containing the audio data is converted into a parallel data format, reads in 62 bits and passes them along to the QAM block.

5.2.1.2 4-QAM Block

The 4-QAM block takes in 31 channels of bit pairs and maps them into symbols of the form $a + jb$. One bit from the pair is mapped to the real component and the other to the imaginary component. These components represent sine and cosines (which translate to the real and imaginary form a+jb in frequency domain).

5.2.1.3 Hermitian Symmetry Block

This block takes in the in-phase and quadrature (real and imaginary) components of the resulting 4-QAM symbols and maps them all only to the even components (h_0, h_2…h_{n-1}) for n=64. Later, this will allow the IFFT block to only transmit the real/in-phase component of the symbol and still be able to recover the original bit stream.

5.2.1.4 64-Point IFFT Block

The IFFT block is based on a Radix-4 64-point algorithm. Radix-4 means that it splits the IFFT calculations in 4 sub-sequences rather than all at once. A Radix-4 block calculates 16 bits of input at a time as shown in the diagram, which is why we need 4 passes by shifting the input 16 points after each sub-sequence to calculate the IFFT of the entire 64-point input. The resulting output however is going to be 4-based digit reversed, as shown in the butterfly diagram in Figure 8.

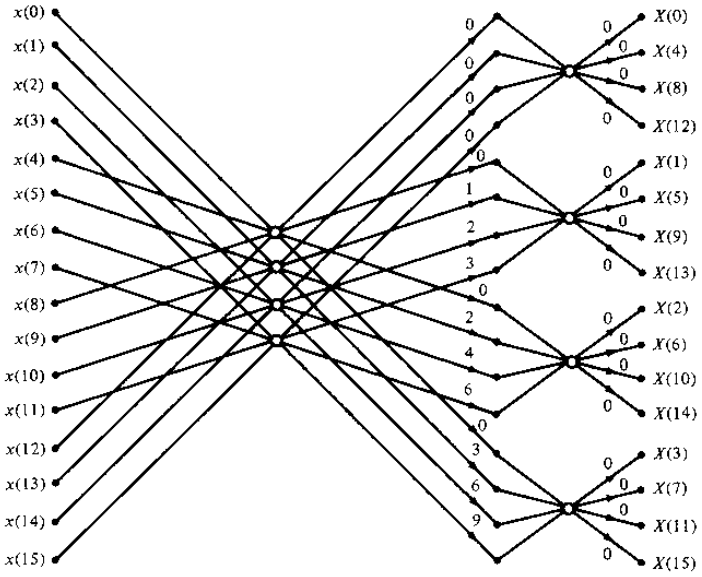

Figure 8: Butterfly Diagram of Radix 4 FFT

5.2.1.5 Parallel to Serial Converter

The parallel to serial converter, reads out from memory the output of the IFFT reading the first few entries again at the end to implement the cyclic prefix.

5.2.1.6 Digital to Analog Convertor

The DAC/ADC boards are an external peripheral and they connect to the DE2-70 board via the extension header pins, controlled through a set of data in/out, read/write and status flags.

5.2.2 Receiver Overview

The receiver is exactly the same as the transmitter model but reversed. After being converted into a digital signal by the Analog to Digital board, the serial data will be parallelized, but have the cyclic prefix removed before feeding it into the FFT block (to reverse the IFFT). This is followed by the Hermitian Symmetry operation, then the 4-QAM decoder and finally serialized into the original bit stream.

The clock frequency we have selected for the OFDM modem is 8 MHz which gives us a maximum data rate of 2 Mbit/s as the design allows the input to be processed in 4 clock cycles/bit.

6 RF module

6.1 Background

Typically in data transmission signals are sent at radio frequencies (RF) instead of baseband. This is done to reduce interference often found at lower frequencies and to decrease the difficulty of transmitting data signals over a large distance.

6.2 Theory

The method of RF modulation we intend to use is called Quadrature-Amplitude Modulation (QAM) which combines two DSB signals together with a 90° phase between then making them orthogonal to each other. This is accomplished by multiplying a carrier signal with one of the message signals, and multiplying a 90° phase shifted carrier with the other message signal and then adding the two results together as shown in the Figure 9 below. The two message signals are the I (real) component and Q (imaginary) component of the OFDM baseband signal.

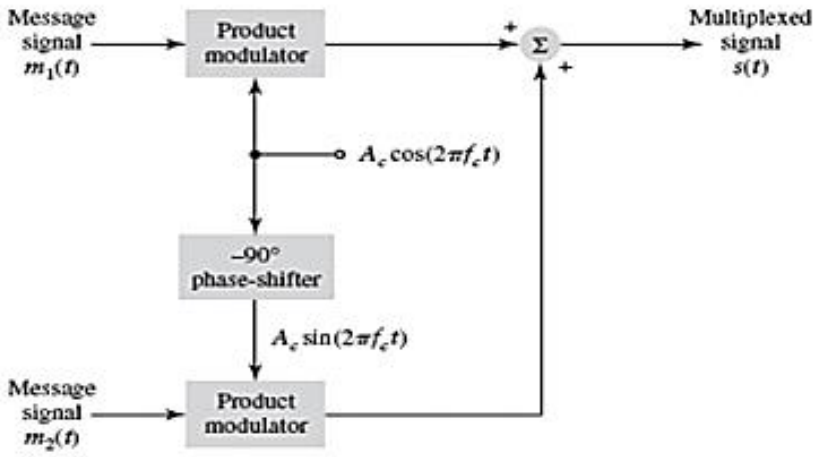

Figure 9: Block diagram of Quadrature-Amplitude Modulation

6.3 Use in SoundSocket

In the SoundSocket product, OFDM modulation is used to create a baseband signal with a bandwidth which starts from DC and extends to 4 MHz. We are in the process of determining how necessary the RF module will be for the correct functionality of SoundSocket. It is possible that we will not need to use RF modulation at all, however as this is currently still unknown we have a plan for including it if necessary. We plan to implement this with the frequency multipliers that are included with the ASLK Pro lab experiment board. Note that the Isolation and Coupling module assumes the use of RF modulation (as it is more challenging).

7 Isolation and coupling module

7.1 Background

One of the key features of our product is transmission of audio via the power lines (mains). If idealized and simplified, the power lines are no different from a pair of long copper cables. If that was the case, then transmission would be as trivial as transmission over a wire. However, there are 2 main issues that are to be overcome in a real world situation: **effective impedance** of the cables and the 110V **60Hz power signal**.

7.1.1 Effective impedance

Depending on the location of the power outlets used for transmission, the effective length of the cable will change the parasitic reactance as well as total resistance. In addition to that, the number and character of household devices plugged in into the outlets on the same mains might affect the input impedance of the power outlet. Thus, the total impedance of the line will fluctuate slightly and the transmitter-receiver pair has to be capable of communicating over a channel of fluctuating impedance.

7.1.2 60Hz power signal

In case of wired transmission, the medium is usually dedicated to the signal it's designed to carry. However, in the case of power line communications, the transmission medium inherently carries a 60Hz 110V signal which it was designed for. The task is to *couple* the data to the power line and *isolate* the SoundSocket signal path from the 60Hz power signal, thus the name "Isolation and coupling module". In the case of 60Hz power signal leaking on to the SoundSocket signal path, the equipment will be damaged immediately, creating a hazardous situation.

7.2 Sub-modules

The isolation/coupling circuit will be described as 2 separate sub-modules: **Transmitter** and **Receiver**. In the final product these modules will be combined, sharing most of the signal path. Due to this, most components that belong to the transmitter sub-module are duplicated in the receiver sub-module description. The combined transceiver block diagram will be shown later in the section. Some components in our design are potentially redundant, providing extra isolation and safety.

7.2.1 Transmitter

The block diagram of the circuitry is shown below in Figure 10.

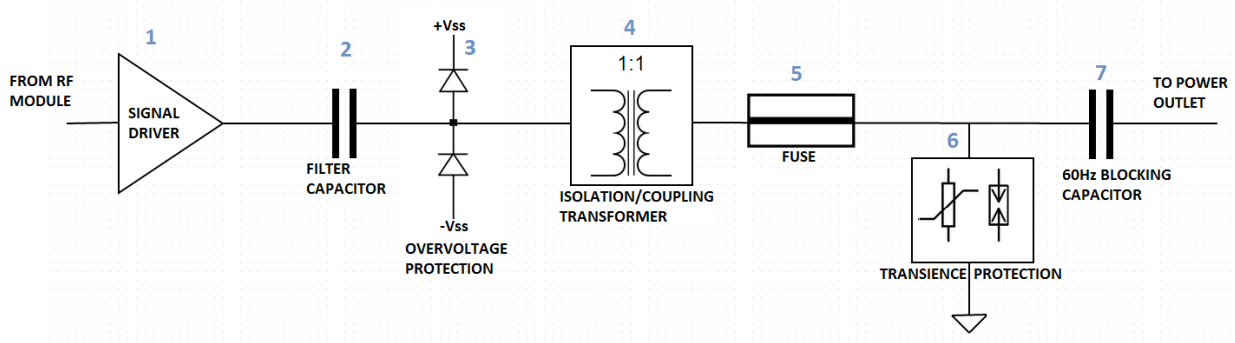

Figure 10: Circuit block diagram of the transmitter sub-module; part of isolation and coupling module

Referring to the figure above, the signal driver (1) provides a high impedance input for the RF module. Essentially it is a buffer preventing RF module from being loaded and providing a low-impedance data signal for next stages. The 600V rated filter capacitor (2) serves as a DC and low-frequency block. Also, in the case of accidental leakage of the 60Hz power signal, the cap will block the power signal, protecting the signal driver. Note that in theory, the 60Hz power signal will not appear anywhere to the left of the blocking capacitor (7). However, to increase the safety of the product some redundancy is implemented. The overvoltage protection (3) will drive any unwanted signal exceeding +/- Vss volts into the power supply; this is likely to be more useful in receiver module discussed next. The isolation/coupling transformer (4) provides galvanic isolation of RF and other modules from being directly connected to the mains. It also couples the data signal from the signal driver to the lines leading to mains line. The fuse (5) will break the circuit in case of accidental high current from high voltage spikes that can bypass the capacitor (7) due to high frequency (these can be caused by lightning strikes for example). This is backed up by the transience protection (6) which will short any high voltage spikes. As mentioned before, the 600V rated blocking capacitor (7) blocks the 60HZ power signal from entering the circuitry. This is the key element in blocking the 60Hz power signal. To sum up, the high frequency data signal driven by the signal driver (1) will bypass the filter cap (2) and overvoltage protection (3), get coupled through the transformer (4), bypass the protection elements (5)(6) and enter the power lines through the capacitor (7).

7.2.2 Receiver

The block diagram of the receiver circuitry is shown below.

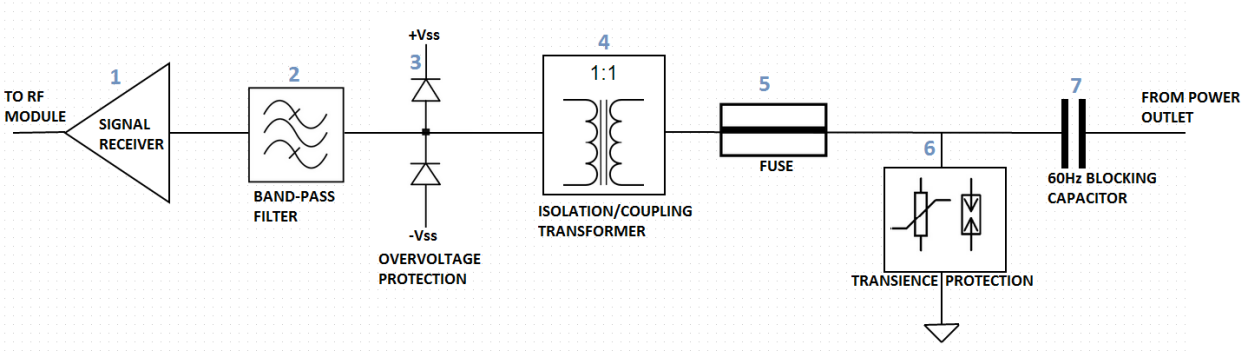

Figure 11: Circuit block diagram of the receiver sub-module; part of isolation and coupling module

The only elements of this receiver sub-module that are different from the transmitter are the signal receiver (1) and a band-pass filter (2). Other elements serve exactly the same purpose as in the case of the transmitter. The data signal will be superimposed onto the 60Hz power signal coming from the power outlet. The capacitor (7) will stop the 60Hz power signal from travelling further, but the high-frequency data signal component will flow through it. The transience protection (6) and the fuse (5) add protection from high frequency voltage spikes as well as accidental 60Hz power signal leak. The transformer (4) will once again provide galvanic isolation and transfer the data signal further down the line. In case there are voltages higher than what the receiver (6) can handle, the overvoltage protection diodes will steer them away from next stage. This protects against any overvoltages that won't get filtered out by previous stages due to high frequency and relatively low amplitude. These are unlikely to happen as there is no immediate reason for those to appear on the lines. The band pass filter (2) is optional and might be used to attenuate any unnecessary frequency components that have made it through all the previous elements. Finally, the signal receiver (1) is there to provide high input impedance, necessary amplification and drive a low impedance data signal to the RF module.

7.2.3 Transceiver

Below is a diagram with the transmitter and receiver are combined into one module; data signal path is shared:

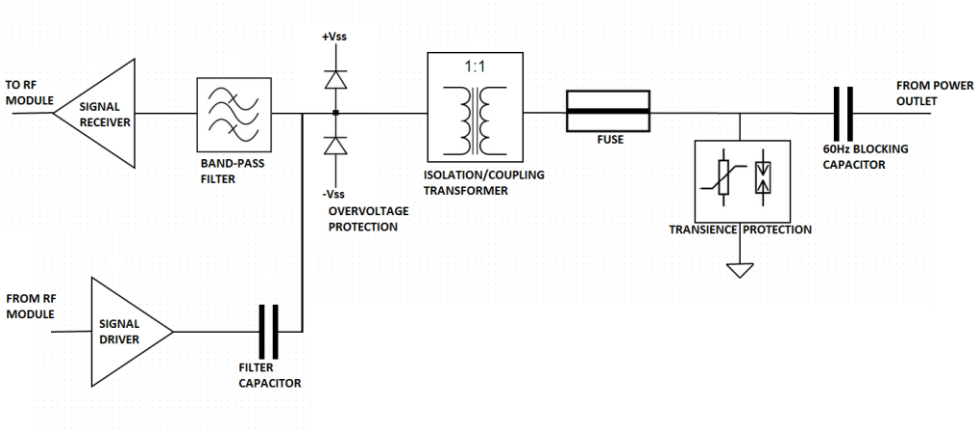

Figure 12: Circuit block diagram of the isolation and coupling module; the Transceiver

8 System Test Plan

Each of the individual sub-modules of Audio Processing Module will initially be tested separately. After the individual sub-modules have been integrated to produce the overall system, the operation of the system will be tested and verified.

8.1 Audio Processing Module

To verify that the audio processing module is functioning correctly, the following tests with sub-modules will be performed:

1) To verify that the Audio CODEC Sub-Module is functioning correctly, perform a loopback test in the VHDL circuitry and input an audio signal to check that the signal passes correctly into and out of the module.
2) To verify that the Audio CODEC Sub-Module and the Nios II module are properly connected, perform a software loopback test and input an audio signal to check that the signal passes into and out of the Nios II module correctly.
3) To verify that the OFDM module is correctly communicating with the Nios II module and receiving correct header information and data, connecting the LEDs on the receiver board to display the header bits received by receiver. First receiver have to extract them from incoming bit stream from OFDM Module on receiver and then amp them to corresponding LEDs on the board.
4) Output bit rate of Audio Processing Module should not be faster than 2 Megabits/second. This test is performed via output the bitrate speed on 7-segment display on DE2-70 Board.

8.2 Loop-Back Tests

To perform Loop-Back Test in context with Audio Codec Module, data read into input variable is passed directly to output variables in order to confirm proper functionality of Audio CODEC Sub-Module of Audio Processing Module.

To perform this test in context with NiosII Processor, data read in input variable of Audio CODEC Sub-Modules is passed to input variables of NiosII Processor Sub-Module and vice versa. This confirm the proper functionality of NiosII processor (excluding packetizing of data)

8.3 Test Plan for the OFDM Transmitter/Receiver

To verify the functionality of the OFDM Transmitter/Receiver, the following is to be verified:

1) The input signal going into the transmitter matches the output signal coming out of the receiver in simulation using ModelSim.
2) The input signal going into the transmitter matches the output signal from the receiver to an acceptable degree (within n% bit error rate) of the original signal in the hardware prototype.
3) The DAC converts digital signals to analog signals
4) The ADC converts analog signals to digital signals

8.4 RF modulation module

To verify that the RF modulation module is functioning properly, the test outlined below will be performed with input sinusoids ranging from 2 to 10MHz. These numbers are the boundary frequencies in case RF modulator is used.

1) Test basic frequency modulation with 6 MHz carrier and simple sinusoidal message signal at various frequencies and then demodulate and recovery original message signal
2) Repeat previous test except using the outputs of the OFDM DA converter as the message signal.
3) Demodulate OFDM signal down to baseband and connect it to the OFDM AD converter to recover original data.

8.5 Isolation and coupling module

To verify that the isolation and coupling module is functioning properly, the test outlined below will be performed with input sinusoids ranging from 2 to 10MHz. These numbers are the boundary frequencies in case RF modulator is used.

1) Initial transmission is to be tested as follows:
    a. The input signal is driven into the signal driver. The sub-test is passed if the input signal appears on the output (a loop-back test).
    b. Without removing the input signal, a mock-up 60Hz power signal at 20V peak-to-peak is supplied instead of the mains power. The sub-test is passed if the output is not affected.
2) Full transmission is to be tested with test 1.b performed with real mains power connected instead of the mock-up signal.
3) If necessary and possible, use an electrostatic discharge gun to simulate a high-voltage spike on the mains power lines. The test will be passed if the spike does not appear on the driver/receiver buffers and does not damage them. Due to lack of expertise and equipment, this test isn't planned.

8.6 Overall Sound Socket test plan

To verify the functionality of the SoundSocket, the following tests are to be performed:

1) A line-level audio source is to be connected to the SoundSocket unit. This unit will be connected directly to another SoundSocket over an extension cable. This sub-test is passed if audio is transmitted and played through the speaker on the receiver side. Absence of audible distortion is important.
2) Repeat sub-test a. above, but with a mock-up 60Hz 20V peak-to-peak power signal present on the extension cable.
3) To meet the Medium Priority requirement [R24-B] of the Functional Specification (transmission through real power lines), the sub-test a. is to be repeated over a real B.C. Hydro mains power lines.

9 Conclusion

The proposed design specifications are aimed to meet mostly the High Priority Proof-of-Concept functional specifications described in the Functional Specification. The design of each individual module is described with moderate level of details. As the implementation and testing is still under way, some design decisions are not finalized. However, we don't expect these to alter the functionality dramatically. The test plans included in this document will be used to test the functionality of individual modules, as well as the functionality of the whole system.

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