Amorphous Silicon Active Pixel Sensor Readout Circuit for Digital Imaging

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***Abstract*—The most widely used architecture in large-area amorphous silicon (a-Si) flat panel imagers is a passive pixel sensor (PPS), which consists of a detector and a readout switch. While the PPS has the advantage of being compact and amenable toward high-resolution imaging, reading small PPS output signals requires external column charge amplifiers that produce additional noise and reduce the minimum readable sensor input signal. This work presents a current-mediated amorphous silicon active pixel readout circuit that performs on-pixel amplification of noise-vulnerable sensor input signals to minimize the effect of external readout noise sources associated with "off-chip" charge amplifiers. Results indicate excellent small-signal linearity along with a high, and programmable, charge gain. In addition, the active pixel circuit shows immunity to shift in threshold voltage that is characteristic of a-Si devices. Preliminary circuit noise results and analysis appear promising for its use in noise-sensitive, large-area, medical diagnostic imaging applications such as digital fluoroscopy.**

***Index Terms*—Active pixel sensor (APS), amorphous silicon (a-Si), digital fluoroscopy, integrated pixel amplifier, medical imaging.**

I. Introduction

Amorphous silicon (a-Si) active matrix flat panel imagers (AMFPIs) have gained considerable significance in large-area flat panel digital imaging applications [1], in view of their large-area readout capability. The pixel, forming the fundamental unit of the imager, consists of a detector and readout circuit to efficiently transfer the collected electrons to external readout electronics for data acquisition. The pixel architecture most widely used is based on the passive pixel sensor (PPS) [1]. An example is the amorphous selenium (a-Se)-based photoconductor detection scheme where the readout circuit consists of a storage capacitor and a thin-film transistor (TFT) readout switch [2]. The storage capacitor accumulates signal charge during the integration period and transfers the collected charge to an external charge amplifier via the TFT switch during readout. While the PPS architecture has the advantage of being compact and thus amenable to high-resolution imaging, reading the small output signal of the PPS for low-input-signal, large-area applications (e.g., fluoroscopy [2]) is extremely challenging and requires costly, high-performance, and sometimes custom-made charge amplifiers [3]. More importantly, if external noise sources (e.g., charge amplifier noise) are comparable to the input, there is a significant reduction in pixel dynamic range. This paper reports an integrated pixel amplifier circuit using a-Si TFTs based on the CMOS active pixel sensor (APS) technology [4]. The APS performs *in situ* signal amplification providing higher immunity to external noise, hence preserving the dynamic range. The current-mediated APS readout circuit was previously presented as a short note [5]. This paper constitutes a comprehensive version providing additional details on its operation, design, and performance pertinent to gain, noise, and a-Si metastability.

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II. Operation

Unlike a conventional PPS, which has one TFT switch, there are three TFTs in the APS pixel architecture. This could undermine the fill factor if conventional methods of placing the sensor and TFTs are used [3]. Therefore, in an effort to optimize the fill factor, the TFTs may be embedded underneath the sensor to provide high-fill-factor imaging systems [1], [2].

Central to the APS illustrated in Fig. 1 is a source-follower circuit, which produces a current output (C-APS) to drive an external charge amplifier. Here, the APS array architecture is assumed to be column-parallel, i.e., one charge amplifier per column so that an entire row can be read out simultaneously. The C-APS operates in three modes.

- Reset mode: the RESET TFT switch is pulsed ON and C_{PIX} charges up to Q_P through the TFTs ON-resistance. C_{PIX} is usually dominated by the detector (e.g., a-Se photoconductor [2] or a-Si photodiode [3] detection layer) capacitance.
- Integration mode: after reset, the RESET and READ TFT switches are turned OFF. During the integration period T_{INT}, the input signal $h\nu$ generates photocarriers discharging C_{PIX} by ΔQ_P and decreases the potential on C_{PIX} by a small-signal voltage ΔV_G.
- Readout mode: after integration, the READ TFT switch is turned ON for a sampling time T_S, which connects the APS pixel to the charge amplifier and an output voltage V_{OUT} is developed across C_{FB} proportional to T_S.

Operating the READ and RESET TFTs in the linear region reduces the effect of inter-pixel threshold voltage (V_T) nonuniformities. Although the saturated AMP TFT causes the C-APS to suffer from FPN, using CMOS-like off-chip double sampling

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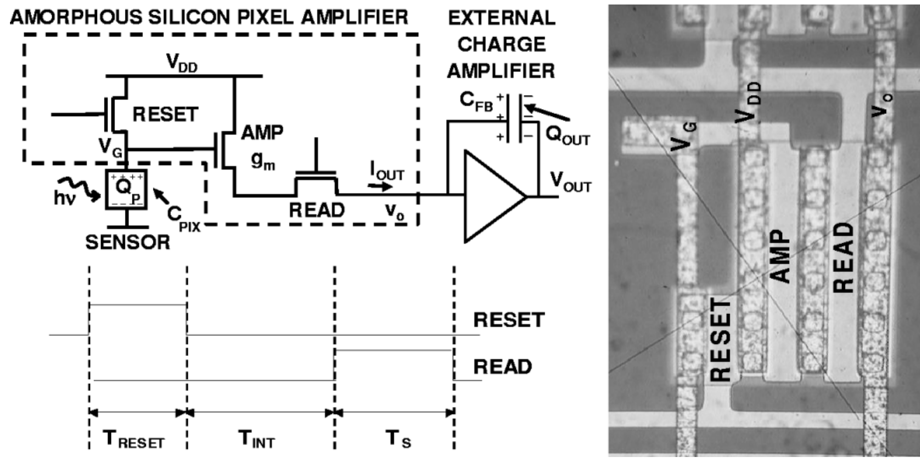


Fig. 1. Current-mode active pixel schematic, readout timing diagram, and a-Si circuit micrograph [5].

[4] and offset and gain correction techniques can alleviate the problem.

III. Gain

A. Theory

When photons are incident on the detector, electron–hole pairs are created leading to a change in the charge at the integration node. The change, due to a sensor input, in the charge detection node bias voltage (V_G) at the gate of the AMP TFT occurs as described in [5]

$$\Delta V_G = \frac{\Delta Q_P}{C_{\mathrm{PIX}}} \tag{1}$$

where ΔQ_P is the change in the input signal charge of the sensor on C_{PIX} due to incoming X-rays and ΔV_G is the corresponding change in the integration node bias voltage. In a typical diagnostic medical imaging fluoroscopic array, using the above equation with $C_{\mathrm{PIX}} = 1$ pF and medical imaging data from [2] (where the minimum and maximum input signals for diagnostic fluoroscopy are 1000 and 100 000 electrons, respectively), a maximum ΔV_G of 16 mV for fluoroscopy can appear at the integration node.

The linearity of the C-APS architecture was previously discussed in [5] where the current-mode APS readout circuit was found to be linear during small-signal circuit operation. The small-signal condition [5] on the maximum allowable voltage swing (ΔV_G) at the C-APS integration node is repeated below for convenience as

$$\Delta V_G \ll 2(V_G - V_T). \tag{2}$$

Thus, for a $V_G = 12$ V and a $V_T = 2$ V, the pixel's output is linear for voltage swings as high as $\Delta V_G = 2$ V (which is more than sufficient for digital fluoroscopy).

During small-signal operation, the change in the amplifier's output current with respect to a small change in gate voltage ΔV_G is

$$\Delta I_{\mathrm{OUT}} = g_m \cdot \Delta V_G \tag{3}$$

where g_m is the transconductance of the AMP and READ TFT composite circuit and ΔV_G represents the small-signal voltage at the gate of the AMP TFT. The transconductance of the composite circuit may be obtained by observing that I_{OUT} is the bias drain current in both transistors. A simplistic MOS Level 1 model is used here to obtain insight although more exact results are obtained via simulation using a previously developed a-Si TFT model [6], [7]. Assuming that the READ TFT operates in the ohmic region with a constant resistance, $R_{\mathrm{ON_READ}}$, equating the I_{OUT} of the AMP and READ TFT yields (4) and (5), shown at the bottom of the page, where K_{AMP} is some constant relating the effective mobility (μ_{EFF}), gate capacity (C_G) and aspect ratio of the TFT ($K = \mu_{\mathrm{EFF}} C_G W/L$ in the c-Si MOSFET Level 1 model). Based on (4) and (5), $R_{\mathrm{ON_READ}}$ must be minimized and $K_{\mathrm{AMP}}(V_G - V_T)$ must be maximized to achieve high g_m. However, care must be taken to ensure that

$$I_{\mathrm{OUT}} = \frac{1 + 2R_{\mathrm{ON_READ}} K_{\mathrm{AMP}}(V_G - V_T) - \sqrt{1 + 4R_{\mathrm{ON_READ}} K_{\mathrm{AMP}}(V_G - V_T)}}{2R_{\mathrm{ON_READ}}^2 K_{\mathrm{AMP}}} \tag{4}$$

$$g_m = \frac{dI_{\mathrm{OUT}}}{dV_G} = \frac{1}{R_{\mathrm{ON_READ}}}\left[1 - \frac{1}{\sqrt{1 + 4R_{\mathrm{ON_READ}} K_{\mathrm{AMP}}(V_G - V_T)}}\right] \tag{5}$$

$I_{\rm OUT}$ does not saturate the charge amplifier. Thus, charge amplifier saturation at high APS biases limits the maximum achievable g_m. Using (1) and (3), the charge gain [8] G_i stemming from the drain current modulation is

$$G_i = \left|\frac{\Delta Q_{\rm OUT}}{\Delta Q_P}\right| = \frac{(\Delta I_{\rm OUT} \cdot T_S)}{\Delta Q_P} = \frac{(\Delta I_{\rm OUT} \cdot T_S)}{\Delta V_G C_{\rm PIX}} = \frac{(g_m \cdot T_S)}{C_{\rm PIX}}. \quad (6)$$

The charge gain amplifies the input signal, making it resilient to external noise sources. The corresponding voltage gain can be calculated using (3) and assuming a constant $\Delta I_{\rm OUT}$. Then, $\Delta V_{\rm OUT}$ for the charge integrating circuit in Fig. 1 can be written as

$$\Delta V_{\rm OUT} = -\frac{1}{C_{\rm FB}}\int_0^{T_S} \Delta I_{\rm OUT} dt = \frac{\Delta I_{\rm OUT} T_S}{C_{\rm FB}} = \frac{(g_m \Delta V_G) T_S}{C_{\rm FB}}. \quad (7)$$

Using (6) and (7), the charge gain G_i can now be related in terms of voltage gain $A_V (= \Delta V_{\rm OUT}/\Delta V_G)$ as

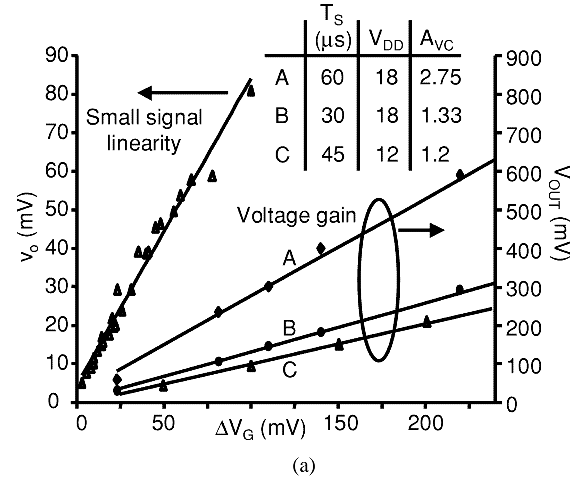
$$G_i = A_V \cdot \left(\frac{C_{\rm FB}}{C_{\rm PIX}}\right). \quad (8)$$

B. Measurements and Discussion

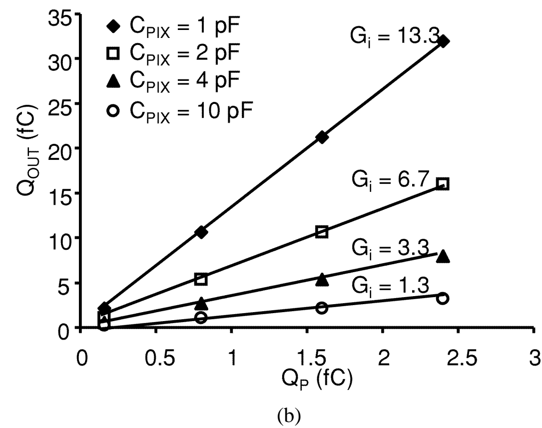
The APS test pixel, consisting of an integrated a-Si amplifier circuit in a $250 \times 250\ \mu{\rm m}^2$ pixel area, was fabricated in-house and is shown in Fig. 1. The small-signal linearity is within 5% of the theoretical value and is shown in Fig. 2(a). For the linearity measurement, the charge integrator shown in Fig. 1 was disconnected from the APS readout circuit and the small-signal output voltage (v_o) was measured. In addition, small-signal voltage gain (A_V) measurements were performed on the APS test circuit using the charge amplifier of Fig. 1 (a Burr–Brown IVC102 model), $V_{\rm RD} = 20$ V, $V_G = V_{\rm DD}$, and $C_{\rm FB} = 10$ pF for various READ pulsewidths T_S and supply voltages $V_{\rm DD}$. The results are also shown in Fig. 2(a).

Theoretical voltage gain A_V (based on (7) where $A_V = \Delta V_{\rm OUT}/\Delta V_G$) and experimental results in Fig. 2(a) agree reasonably well with a maximum discrepancy of about 10%. The verified theoretical model of (7) was extended to predict charge gain in Fig. 2(b) using (8) for different values of $C_{\rm PIX}$, $C_{\rm FB} = 10$ pF and $A_V = 1.33$ [for $T_S = 30\ \mu$s in Fig. 2(a)]. Theoretically, using a low-capacitance sensor (i.e., small $C_{\rm PIX}$) provides a higher charge gain, which minimizes the effect of external noise. In addition, minimizing $C_{\rm PIX}$ will also reduce the reset time constant (which comprises mainly of the RESET TFT ON-resistance and $C_{\rm PIX}$), hence reducing image lag [9]. Like other current-mode circuits [8], the C-APS, operating at a maximum of 30 kHz (for diagnostic fluoroscopy), is susceptible to sampling clock jitter. However, off-chip low-jitter clocks using crystal oscillators can alleviate this problem.

The advantage of the current-mediated APS over PPS pixels in diagnostic medical X-ray imaging applications lies in amplifying the sensor input signal electrons via the charge gain G_i.



(a)



(b)

Fig. 2. (a) Small-signal linearity and voltage gain (A_V) measurements. (b) Theoretical charge gain (G_i) for different pixel capacitances $(C_{\rm PIX})$ extracted from voltage gain measurements.

More significantly, the pixel (because of its circuit gain) offers *potentially reduced* patient X-ray doses for all diagnostic medical imaging modalities, hence improving the safety standards associated with current X-ray imaging practices. In contrast to a voltage-mediated a-Si APS [10], the main benefits of the current-mediated architecture lie in both gain and speed:

- Gain: the source-follower TFT in the voltage-mediated APS directly translates the voltage from the integration node to the output node at the external resistance with a gain <1. In contrast, the C-APS architecture gives both a voltage and a charge gain where the charge gain is instrumental is combating noise.
- Speed: the relative ON-resistances of a-Si TFTs are quite large (in MΩ). Coupled together with large-array column line capacitances ($C_{\rm LINE}$ is typically 50–100 pF) at the output node that must be charged and discharged repeatedly, the rise and fall times become prohibitively large, making the voltage-mediated architecture unsuitable for real-time applications. In contrast, the current-mediated APS is directly coupled to the virtual ground input of a charge integrator (effectively shunting $C_{\rm LINE}$ to ground). Here, the charging up of the charge amplifier feedback capacitance $(C_{\rm FB})$ depends on the slew rate of the amplifier.

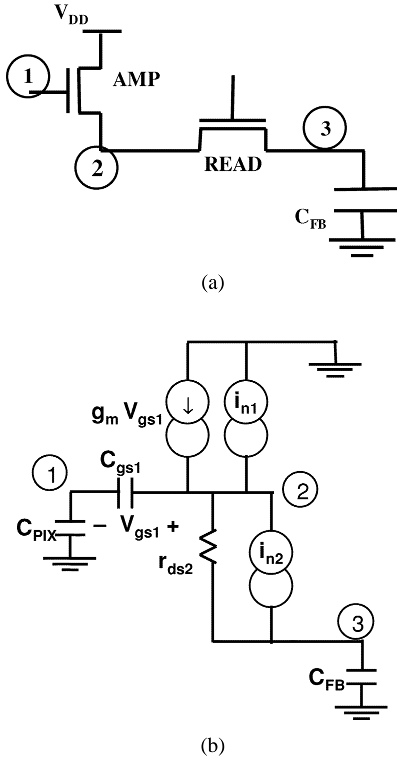


Fig. 3. (a) APS circuit during readout. (b) Small-signal equivalent with included current noise sources.

IV. Noise Performance

A. Thermal and Flicker Noise

During readout, the circuit of Fig. 1(a) reduces to a source-follower stage with source degeneration as shown in Fig. 3(a) where the READ TFT switch ON-resistance provides the degeneration in the AMP TFT's source. Modifying the small-signal model to include independent noise sources, the equivalent circuit is shown in Fig. 3(b) where the noise is sampled on the column charge amplifier capacitance C_{FB}. Here, C_{PIX} is the sum of capacitances between the detector node and ground and C_{gs1} is the gate–source parasitic capacitance of the AMP TFT. In steady state, the AMP TFT operates in saturation while the READ TFT operates in the linear mode. Hence, the READ TFT switch is represented by its ON-resistance $r_{ds2} = (1/g_{ds2})$. The TFT switch ON-resistance may be approximated as $r_{ds2} = dI_{DS(\mathrm{lin})}/dV_{DS} \sim [K(V_G - V_T)]^{-1}$. In Fig. 3(a), i_{n1} represents the noise current from the AMP TFT while i_{n2} represents the noise current from the READ TFT.

A nodal analysis in the frequency domain $(s = j\omega)$ of the equivalent circuit of Fig. 3(b) yields the noise voltage at the output V_3, defined in (9) at the bottom of the page. Equation (9) can be simplified by assuming $C_{\mathrm{FB}} \gg C_{\mathrm{PIX}} \gg C_{gs1}$ and that $s \ll g_{m1}/C_{gs1}$ (i.e., the operating frequency is far from the pole of the parasitic C_{gs1}) to yield

$$V_3 = \frac{i_{n1}.R_{eq1} + i_{n2}.r_{ds2}}{1 + j\left(\frac{w}{w_{eq}}\right)},$$
$$R_{eq1} = \left[g_{m1}.\frac{C_{\mathrm{PIX}}}{C_{\mathrm{PIX}} + C_{gs1}}\right]^{-1}$$
$$w_{eq} = \left[\frac{1}{C_{\mathrm{FB}}}.\frac{g_{ds2}.g_{m1}}{g_{ds2} + g_{m1}}\right]. \quad (10)$$

From (10), the spectral density of the noise S_{v3} at the output may be expressed as

$$S_{v3} = \frac{S_{in1}.R_{eq1}^2 + S_{in2}.r_{ds2}^2}{1 + \left(\frac{w}{w_{eq}}\right)^2} \quad (11)$$

where $\omega_{eq} = 2\pi f_{eq}$ represents the bandwidth of the APS circuit, R_{eq1} is related to the transconductance of the AMP TFT, and r_{ds2} is the ON-resistance of the READ TFT switch. The noise variance at the output σ_3^2 can be computed using thermal and flicker noise expressions suitable for a-Si TFTs. For thermal noise, we have

$$\sigma_3^2(\mathrm{th}) = (\mathrm{f_{eq}})\left(\frac{\pi}{2}\right) \cdot \left(\mathrm{R_{eq1}^2 \cdot a_{th1} + r_{ds2}^2 \cdot a_{th2}}\right) \quad (12)$$

where $a_{\mathrm{th1}} = (2/3).4kT.g_{ml}$, $a_{\mathrm{th2}} = 4kT.g_{ds2}$, f_{eq} is the circuit bandwidth, and $(\pi/2)(f_{eq})$ is the classic noise bandwidth of a first-order low-pass filtering circuit.

For flicker noise, we have

$$\sigma_3^2(fl) = \left(R_{eq1}^2.a_{fl1} + r_{ds2}^2.a_{fl2}\right)\int_{f_{\mathrm{OBS}}=1/T_{\mathrm{OBS}}}^{\infty} \frac{1}{f\left(1+\frac{f^2}{f_{eq}^2}\right)} df$$
$$= \left(R_{eq1}^2.a_{fl1} + r_{ds2}^2.a_{fl2}\right)\left(\frac{1}{2}\right)\ln\left(1 + \frac{f_{eq}^2}{f_{\mathrm{OBS}}^2}\right) \quad (13)$$

where a_{fl1} and a_{fl2} are flicker noise coefficients of the saturated AMP and linear READ TFTs, respectively, and T_{OBS} is the time of observation of the flicker noise [11]. Here, expressions for a-Si:H TFT flicker noise coefficients are given as [12], [13]

$$a_{fl1} = \frac{\alpha_{\mathrm{sat}}.q.\mu_{\mathrm{EFF}}^2.C_G.\left(\frac{W}{L}\right)^2}{2(W.L)}.(V_G - V_T)^3$$
$$a_{fl2} = \frac{\alpha_{\mathrm{lin}}.q.\mu_{\mathrm{EFF}}^2.C_G.\left(\frac{W}{L}\right)^2}{(W.L)}.(V_G - V_T).V_{DS}^2. \quad (14)$$

However, when the APS is used in imaging applications, the READ TFT is pulsed, causing the flicker noise performance to change. Here, double sampling is essential to perform offset and

$$V_3 = \frac{g_{ds2}.i_{n1}(C_{\mathrm{PIX}} + C_{gs1}) + i_{n2}(g_{m1}.C_{\mathrm{PIX}} + s.C_{\mathrm{PIX}}.C_{gs1})}{g_{m1}.g_{ds2}.C_{\mathrm{PIX}} + s(g_{m1}.C_{\mathrm{PIX}}.C_{\mathrm{FB}} + C_{\mathrm{PIX}}.C_{gs1}.g_{ds2} + C_{\mathrm{PIX}}.g_{ds2}.C_{\mathrm{FB}} + C_{gs1}.g_{ds2}.C_{\mathrm{FB}}) + s^2(C_{\mathrm{PIX}}.C_{gs1}.C_{\mathrm{FB}})} \quad (9)$$

gain corrections for proper operation of the APS. With double sampling, the effect of V_T nonuniformities as well as any dc components including low-frequency flicker noise [14] is mitigated. However, the thermal noise components from the AMP and READ TFTs, the reset noise, and the amplifier noise are all increased since they are uncorrelated sources. Using S_{v3} and noting that the thermal white noise sources are uncorrelated here, the output thermal noise with double sampling is

$$\sigma_3^2(th) = \pi f_{eq}. \left(R_{eq1}^2 \cdot a_{\text{th1}} + r_{ds2}^2 \cdot a_{\text{th2}}\right), \tag{15}$$

Similarly, using previously derived results [14], the output flicker noise with double sampling becomes

$$\sigma_3^2(fl) = 2.I. \left(R_{eq1}^2 \cdot a_{fl1} + r_{ds2}^2 \cdot a_{fl2}\right) \tag{16}$$

Here, as detailed in [14], I is an integral that accounts for the bandpass filtering effect of double sampling on flicker noise

$$I(x_{eq}) = \int_0^{\infty} \frac{1-\cos x}{x\left(1+\left(\frac{x^2}{x_{eq}^2}\right)\right)}.dx \tag{17}$$

where $x_{eq} = 2.\pi.f_{eq}.\tau_f$ and τ_f is the time between the pixel output and reset output samples. For small τ_f, the $I(x_{eq})$ function resembles a bandpass filter that eliminates low-frequency and dc noise.

In the case where the output is not subject to double sampling, the contributions of the uncorrelated noise sources are that of the unsampled case. The output thermal noise without double sampling is written as in (12). Similarly, the output flicker noise for a single pulse reduces to (13). In this case, however, the observation time (T_{OBS}) is defined as the pulse width of the READ TFT sampling signal [11], [14]. For a real-time, 1000×1000 pixel, fluoroscopic array (based on a column-parallel architecture) operating at a frame rate of 30 Hz, the READ TFT for each pixel is clocked at 33 μs. Hence, T_{OBS} is 33 μs and, thus, the lower limit of integration $f_{\text{OBS}}(=1/T_{\text{OBS}})$ in (13) becomes 30 kHz.

B. Reset Noise

The thermal noise of the RESET TFT ON-resistance is low-pass filtered by the pixel capacitance C_{PIX} and stored on C_{PIX} during reset. Although it is possible to approximate this noise as $\sigma_{\text{reset}}^2 = kT/C_{\text{PIX}}$, it is more accurate to include the effect of the feedback AMP TFT parasitic capacitance C_{gs1}. Then the effective capacitance at the detection node becomes [14]

$$C_{\text{eff}} = C_{\text{PIX}} + (1 - A_{V0}).C_{\text{gsl}} \tag{18}$$

where A_{V0} is the dc gain of the AMP TFT buffer. Therefore, the reset noise becomes

$$\sigma_{\text{reset}}^2 = \frac{kT}{C_{\text{eff}}}. \tag{19}$$

Referring to Fig. 3(b), the dc gain $A_{V0} = V_2/V_1$ can be accurately estimated by including the AMP TFT ON-resistance in saturation as $r_{ds1} = 1/(\lambda I_{DS})$

$$\frac{V_2}{V_1} = A_{V0} = \frac{1}{\left(1 + \frac{1}{g_{m1}.r_{ds1}}\right)}. \tag{20}$$

In addition, if double sampling is implemented, the reset noise variance doubles to give $\sigma_{\text{reset}}^2 = 2kT/C_{\text{eff}}$.

C. Charge Amplifier Noise

The amplifier noise can be modeled as having a fixed noise component σ_{amp0} in addition to an input-capacitance-dependent component [15]

$$\sigma_{\text{amp}} = \sigma_{\text{amp0}} + \delta C_d. \tag{21}$$

Here δ is a constant determined by the design properties of the charge amplifier (e.g., input FET noise) and C_d is the external capacitance loading the amplifier input node. This includes the parasitic capacitances on the data line such as the C_{GS} of all of the READ TFTs in the column as well as the overlap capacitance of data and gate lines. A typical value for the amplifier noise is about 1700 electrons [2], [16] where the base noise $\sigma_{\text{amp0}} =$ 275 electrons, $C_d = 95$ pF, and $\delta = 15$ area is assumed [2]. With double sampling, the noise variances doubles and, thus, the rms noise increases to 2400 electrons.

D. Total Output Noise and Input Referred Noise

Since the various APS noise sources are uncorrelated, the noise on C_{FB} after double sampling becomes

$$\sigma_{\text{out}}(\text{tot})^2 = \left(A_V^2 \sigma_{V_{\text{reset}}}^2\right) + \sigma_{v3}^2(th) + \sigma_{v3}^2(fl) + \sigma_{\text{amp}}^2 \tag{22}$$

where A_V is the voltage gain of the current-mediated APS connected to the charge integrator and was determined in Section IV-C. Note that, since the reset noise occurs at the same node as the signal, the charge gain increases both the reset noise in addition to the sensor input. $\sigma_{\text{out}}(\text{tot})^2$ can be referred back to the input of the APS at the gate of the AMP TFT to give $\sigma_{\text{input}}(\text{tot})$ as

$$\sigma_{\text{input}}(\text{tot}) = \frac{\sqrt{\sigma_{\text{out}}(\text{tot})^2}}{A_V}. \tag{23}$$

For the purposes of charge gain, it is beneficial to examine the noise from the standpoint of number of electrons. From (22) and (23), noise equivalent output electrons $\text{NEQ}(\text{output})$ and noise equivalent input electrons $\text{NEQ}(\text{input})$ can be determined. Here, q denotes the electron charge

$$\text{NEQ}(\text{output}) = \frac{\sqrt{\sigma_{\text{out}}(\text{tot})^2}.C_{\text{FB}}}{q} \tag{24}$$

$$\text{NEQ}(\text{input}) = \frac{\sqrt{\sigma_{\text{out}}(\text{tot})^2}.C_{\text{PIX}}}{A_V.q} = \frac{\sqrt{\sigma_{\text{out}}(\text{tot})^2}.C_{\text{FB}}}{G_i.q}. \tag{25}$$

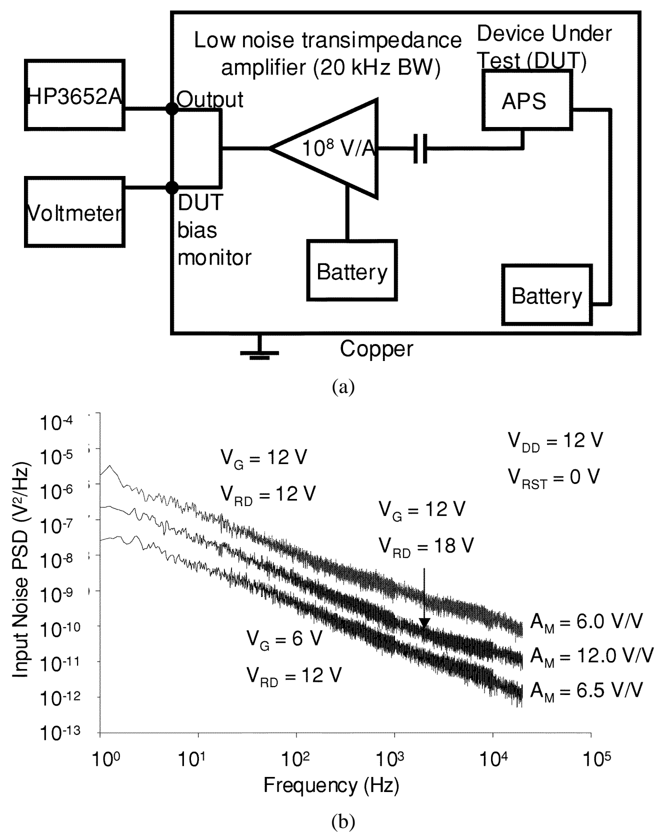


Fig. 4. (a) APS readout circuit noise measurement setup. (b) Input noise PSD (in V^2/Hz) for selected bias voltages.

E. Measurements and Discussion

Current-noise-power spectrum (S_{ID} in A^2/Hz) measurements were previously presented in [18] for a-Si TFTs fabricated at the University of Waterloo using an in-house fully wet-etched 260 °C process. The results concluded that the a-Si flicker noise current PSD measurements were consistent with previous findings [12], [13]. Specifically, it appeared that the fabricated a-Si TFTs followed Hooge's theory regarding bulk mobility fluctuations as the cause of $1/f$ noise. In addition, the thermal noise was in good agreement when fitted to the crystalline silicon MOSFET I_{DS} equation (a simple and heuristic model for predicting the channel thermal resistance in a-Si TFTs) at large V_{GS} biases, but less accurate as the TFT approaches saturation, thus requiring a more accurate model for the TFT ON-resistance. This result also concurs with previous findings [13].

The APS noise measurements were carried out for the fabricated test a-Si APS device shown in Fig. 1. V_G, V_{DD}, and V_{RD} (the READ TFT bias) were all provided by high-amp-hour dc batteries while an ac-coupled Perkin-Elmer 5182 transimpedance amplifier was used to amplify the noise signal to levels readable by the HP 3562 A spectrum analyzer. The RESET TFT gate was grounded during this measurement. The ac gain of the amplifier was set at 10^8 for a bandwidth of 20 kHz. The noise measurement setup is depicted in Fig. 4(a). All noise power curves were reconstructed from narrow-band measurements averaged at least 25–50 times and higher for low frequencies. The system noise was at least one order of magnitude lower (at high frequencies) than the APS output noise and was subtracted from each measured power spectrum. For each measurement, acquisition began a half hour after application of the bias voltages to allow the APS bias current I_{OUT} and the noise to stabilize.

To extract input noise voltage PSD (V^2/Hz), the system (i.e., APS readout circuit plus the transimpedance amplifier) voltage gain had to be measured over all frequencies of interest for each biasing arrangement. Then, the measured gain was used to adjust the output noise voltage PSD to obtain the input noise PSD at the gate of AMP TFT. Fig. 4(b) shows the input noise PSD for a few APS biasing arrangements where it is noted that the input noise voltage PSD increases with increasing AMP TFT bias (V_G) but decreases with increasing READ TFT bias (V_{RD}). This follows directly from the noise voltage PSD expressions for the Hooge theory of flicker noise where the flicker noise voltage PSD is directly proportional to TFT gate voltage in the saturation region but inversely proportional to the TFT gate voltage in the linear region. The measured data appear to be in good agreement with the theory. The values of the Hooge coefficients used here are extracted from previous data [18], whereby $\alpha_{sat} \sim 0.02$ for TFTs in saturation and $\alpha_{lin} \sim 0.008$ for TFTs operating in linear. Also, the mid-band gain (A_M) increases for increasing V_{RD} (read as a decrease in r_{ds2}), which follows from (5) relating g_m (and hence gain) to r_{ds2} in Section IV-D.

Integrating the area under the noise curves retrieves the input referred rms noise voltage for the APS. The lower limit of the integration, as mentioned previously, is usually determined from the frame rate of the imager. From Fig. 4(b), it is evident that the noise of the APS is dominated by flicker noise of the AMP and READ TFTs. However, when the APS is used in imaging applications, the READ TFT is pulsed, causing the flicker noise performance to change. In addition, for APS circuits used in digital imaging, double sampling, used to perform offset and gain corrections for proper operation of the APS, mitigates the effect of V_T nonuniformities as well as any dc components including low-frequency flicker noise. Using the theory presented previously in this section, the results of an APS noise analysis with double sampling are presented in Table I and appear promising for diagnostic medical imaging (particularly for real time fluoroscopy where the minimum signal is only 1000 electrons).

The noise and gain analyses so far indicate that a decreasing C_{PIX} provides the dual benefits of decreased noise and an increase in charge gain. However, using conventional co-planar pixel architectures where the sensor and TFTs are placed side by side gives rise to a tradeoff between noise performance, charge gain, and fill factor. For a small C_{PIX}, the reset noise decreases, and the charge gain increases but the fill factor shrinks since the sensor area must be reduced to get a smaller C_{PIX}. However, for the a-Si APS circuit, it is desirable to maintain a high fill factor while shrinking C_{PIX}.

Embedding the TFTs underneath the sensor in a fully overlapped pixel architecture [1], [17] allows the pixel to achieve a near 100% fill factor. A small C_{PIX} in addition to a high fill factor can be achieved by using a thick, continuous layer sensor [2] such as an a-Se photoconductor for detecting X-rays. In digital fluoroscopy ($250 \times 250\ \mu m^2$ pixels), the a-Se photoconductor thickness ranges from 0.5 to 1 mm which gives

TABLE I
PREDICTED APS NOISE (IN ELECTRONS) FOR VARIOUS NOISE SOURCES AT THE OUTPUT AND THE TOTAL INPUT REFERRED NOISE. HERE, C_{PIX} OF 1 pF AND 2 pF ARE USED TO CALCULATE THE CHARGE GAIN G_i. THE NOISE RESULTS ARE EXTRACTED FOR THE FABRICATED APS READOUT CIRCUIT USING THE THEORY PRESENTED IN THE PAPER WITH THE MEASURED GAIN AND NOISE VALUES

Noise at output	NEQ (electrons) (C_{PIX} = 1 pF)	NEQ (electrons) (C_{PIX} = 2 pF)
Thermal	1691	1649
Flicker	2363	2257
Reset	7508	5329
Amplifier	2400	2400
Total Noise (output)	8401	6478
Charge Gain (G_i)	13.3	6.65
Total Noise (input)	631	974

$C_{\mathrm{sensor}} < 10$ fF. Since C_{PIX} can become very small due to the decrease in C_{sensor}, an additional physical storage capacitor is usually designed into the pixel at the integration node to prevent the node voltage from rising excessively due to the increased dynamic range because large voltages at the integration node can cause problems ranging from output nonlinearity to TFT breakdown [2].

Embedding the TFTs underneath the sensor also provides a second benefit by making a large portion of the pixel area available for additional TFT circuitry or larger TFTs. Since the charge gain (G_i) partly depends on g_m (which is a direct function of the size of the input stage AMP TFT of the APS), the additional area available in a fully overlapped architecture can be used to achieve much larger TFTs and hence g_m. Note that, in addition to increasing g_m and decreasing C_{PIX}, G_i can also be made higher by increasing T_S, the sampling time of the READ TFT as shown in (6).

V. METASTABILITY

The threshold voltage (V_T) of an a-Si TFT shifts under prolonged gate bias stress, and TFTs show different threshold voltage shift behavior under positive and negative gate bias stress. This anomalous behavior is attributed to two main mechanisms: 1) charge trapping and 2) defect state creation [19]. In addition, a-Si:H TFTs exhibit different behavior for pulsed positive and negative stress voltages [20], [21]. The V_T shift (ΔV_T) due to positive pulse bias stress is almost independent of frequency of operation but, for negative pulse bias stress, the ΔV_T decreases in magnitude with increasing frequency [20]. In general, smaller duty cycles induce less ΔV_T since the effective stress time is decreased. This allows the created defect states to relax and/or charges can detrap during the "OFF" cycles [21].

For the APS pixel, there are three TFTs of concern: READ, AMP, and RESET and their ΔV_T performance depends largely on the application of the APS. If medical imaging is chosen as an example, a large factor aiding the APS stability here is the reduced TFT duty cycle for diagnostic medical imaging applications. For example, in a 1000×1000 pixel real-time fluoroscopic imager, the TFTs are clocked 33 μs every 33 ms (i.e., a duty cycle of 0.1%).

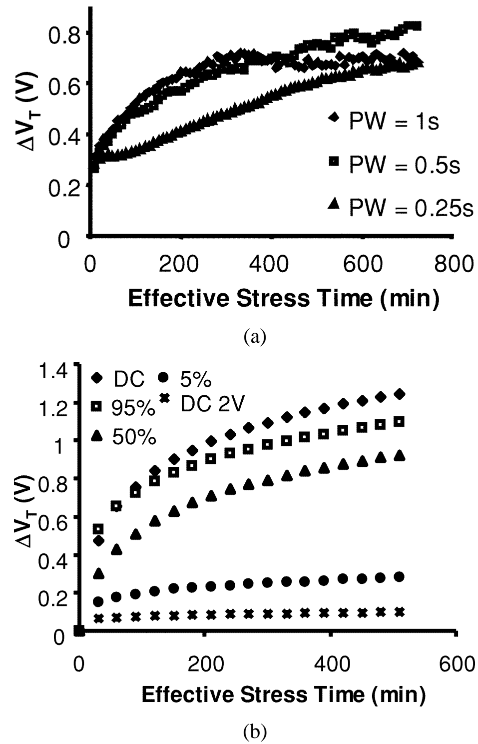


Fig. 5. (a) ΔV_T for a TFT $(W/L = 230/23)$ with a bipolar bias stress voltage of $+20$ V/-20 V. The duty cycle is 50% and various pulse widths (PW) are applied, (b) ΔV_T for a TFT $(W/L = 60/25)$ with a bias stress voltage of $+15$ V at 30 Hz for various duty cycles. The ΔV_T for an applied DC stress voltage of 2 V to the same TFT is also shown.

One method [20] of preserving the V_T in TFTs is by application of bipolar clocking voltages. Since a positive pulse serves to increase the ΔV_T and a large negative pulse can reverse this shift, applying negative pulses to the TFT during the OFF cycle can minimize the ΔV_T. To illustrate this effect, Fig. 5(a) shows the ΔV_T stabilizing for a bipolar pulse. However, an additional constraint for medical imaging applications is the low TFT leakage current requirement. For the RESET TFT, it is essential to prevent any excessive TFT leakage that can corrupt the signal accumulating at the AMP TFT gate. For the READ TFT, since READ TFTs in an array column are all connected to a single column charge amplifier (up to 1000 column pixels in digital fluoroscopy), their leakage currents are added. If comparable, this aggregate READ TFT leakage current can corrupt the small output signal of the APS pixel being read out. Therefore, the magnitude of the TFT negative voltage in the OFF state must be limited to satisfy the low leakage current requirement. As illustrated in Fig. 5(b), reducing the duty cycle can severely reduce the ΔV_T and thus, for the APS READ and RESET switch TFTs, bipolar clocking pulses to provide a small switch resistance in the TFT ON state (for high g_m) and a small leakage current in the TFT OFF state can be designed to give a constant V_T. However, for the saturated AMP TFT, a positive bias of approximately $V_{\mathrm{GS}} < V_T$ ($\sim$ 2 V) exists across the AMP TFT

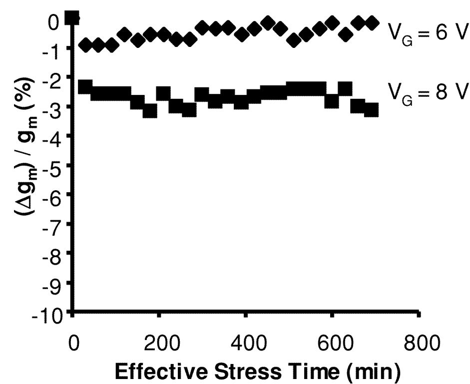


Fig. 6. $\Delta g_m/g_m$ (in percent) for the APS readout circuit. Here, $V_{\rm RD} = 12$ V and $V_{\rm DD} = V_G$ for both measurements. The RESET TFT gate was grounded for the duration of the measurement.

during the pixel OFF state. Fortunately, due to its small positive value, the 2 V bias has limited effect on the positive ΔV_T as illustrated in Fig. 5(b). Details of the ΔV_T measurement were presented previously in [22].

To illustrate the effect of any ΔV_T on the APS readout circuit (comprising of the AMP and READ TFTs), measurements were carried out on the fabricated a-Si APS pixel for different bias voltages. The READ TFT was biased at $+12$ V in the ON state for low ON resistance (r_{ds2}), -5 V in the OFF state since that voltage gives the lowest leakage current value for the fabricated TFTs and with a duty cycle of 10% at a frequency of 30 Hz. The results in Fig. 6 indicate that the composite circuit transconductance, g_m, defined in (5), which is directly related to the APS charge gain, does not vary beyond some initial drop for the bias voltages used. This is a direct consequence of choosing appropriate bias and clocking voltages and the READ TFT switch acting as a feedback source resistor for the AMP TFT, stabilizing g_m for small changes in V_T.

VI. Conclusion

This paper presents a current-mode on-pixel a-Si amplifier for higher immunity to external noise sources associated with the charge amplifier and data line in an imaging array. Measurements show excellent linearity and high gain where the charge gain can be made programmable by appropriate selection of bias voltage and sampling time. In addition, the circuit possesses an inherent immunity to small shifts in the threshold voltage of the TFTs, which are induced by the intrinsic material defects associated with the amorphous silicon and amorphous silicon nitride films in the TFT. Also, the noise performance of the APS readout circuit appears promising for noise-vulnerable digital imaging applications such as fluoroscopy.

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