Drain-Bias Dependence of Threshold Voltage Stability of Amorphous Silicon TFTs

Karim S. Karim, Arokia Nathan, Michael Hack, and William I. Milne

Abstract—Amorphous silicon (a-Si:H) thin-film transistors (TFTs) used in emerging, nonswitch applications such as analog amplifiers or active loads, often have a bias at the drain terminal in addition to the gate that can alter their threshold voltage ($V_{TH}$) stability performance. At small gate stress voltages ($0 \leq V_{GST} \leq 15$ V) where the defect state creation instability mechanism is dominant, the presence of a bias at the TFT drain decreases the overall shift in $V_{TH}(\Delta V_{TH})$ compared to the $\Delta V_{TH}$ in the absence of a drain bias. The measured shift in $V_{TH}$ appears to agree with the defect pool model that the $\Delta V_{TH}$ is proportional to the number of induced carriers in the a-Si:H channel.

Index Terms—Amorphous silicon, thin-film transistor (TFT), threshold voltage, metastability.

Unlike crystalline silicon transistors, a-Si:H TFTs exhibit bias-induced metastability phenomena that can have adverse effects on circuit performance if the circuit is improperly designed or operated. Metastability concerns become particularly important when the TFT is used as an analog device. In contrast to traditional applications (e.g., in LCDs) where the TFT is used as a switch, analog applications can require the device to withstand prolonged voltages at both the drain and gate terminals. This research focuses on developing an understanding of circuit performance when dc-bias voltages are applied simultaneously at the TFT drain and gate terminals.

The two widely accepted mechanisms for threshold voltage ($V_{TH}$) instability in a-Si:H TFTs are defect state creation and charge trapping. Defect creation dominates at lower positive bias voltages (e.g., $<25$ V) while charge trapping in the gate insulator becomes significant at higher gate voltages [1]–[3]. The latter occurs primarily in plasma-enhanced chemical vapor deposition (PECVD) a-Si:N$_x$ gate insulator TFTs where the high density of defects in the insulator can trap charge when the TFT gate undergoes bias stress [1], [2]. The point at which charge trapping overtakes defect state creation has been shown to be a function of the gate nitride stoichiometry [2] and usually occurs at larger voltages for nitrogen-rich gate dielectrics [4]. Low power requirements in emerging analog applications of a-Si:H TFT technology (e.g., active pixel sensor (APS) x-ray imager [5] and organic light emitting diode (OLED) display [6]) underscore the drive toward reducing circuit supply voltages to a level where defect state creation becomes the dominant $\Delta V_{TH}$ mechanism.

In contrast, defect creation in the a-Si:H layer or at the a-Si:H/a-Si:N$_x$ interface due to a prolonged gate bias has been reported to have some similarities to light-induced defect creation [7] where the density of deep-state defects increases. When a positive bias is applied to the gate of an a-Si:H TFT, electrons accumulate and form a channel at the a-Si:N$_x$/a-Si:H interface where they predominantly reside in conduction band tail states [8]. These tail states have been identified as weak silicon–silicon bonds which, when occupied by electrons, can break to form silicon dangling bonds (deep-state defects) [9], [10]. Deep-state defect creation forms the basis of the defect pool model [11], where the rate of defect creation is a function of the barrier to defect formation, the number of electrons in the tail states, and the density of the weak bond sites.

It has been proposed that deep-state defect creation is characterized by a power law time dependence and is strongly affected by temperature [4]. Charge trapping, on the other hand, has a logarithmic time dependence and is weakly dependent on temperature. Then, for the defect state creation mechanism in a uniform a-Si:H TFT channel, $\Delta V_{TH}$ can be expressed as [4], [9]

$$\Delta V_{TH}(t) = A(V_{GST}-V_{TH})^\beta$$

where $A$ and $\beta$ are temperature-dependent parameters, $V_{GST}$ is the gate bias stress voltage, $V_{TH}$ is the $V_{TH}$ of the TFT before bias stress is applied, and $t$ is the bias stress time duration.

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The a-Si:H TFTs used for this experiment are of the inverted staggered, bottom gate design (W/L = 0)/25, 250-nm a-Si:Nx gate insulator, 50-nm a-Si:H semiconductor) with a passivating a-Si:Nx layer on top of the a-Si:H channel layer [12]. The samples were annealed at 180 °C for 3 h and cooled for 3 h before each bias stress measurement. The annealing and cooling procedure was verified to restore both, TFT transfer characteristics (I_D–V_G) and V_T, to within 5% of their original pre-stress values.

To evaluate the effect of constant bias stress on TFT characteristics, I_D–V_G curves need to be measured periodically during the stress experiment. However, since the TFT is sensitive to bias stress during the I_D–V_G measurements,

1) fast measurements;
2) a small number of measured points per I_D–V_G curve;
3) reducing the total number of I_D–V_G curves per bias stress test

are all necessary to minimize the impact of monitoring TFT I_D–V_G characteristics on the overall bias stress experiment. All I_D–V_G curves were measured at V_D = 0.5 V using the fast electrometer setting on Keithley 236 SMUs. It took less than 30 s to interrupt the constant bias stress experiment and plot an entire I_D–V_G curve (for 0 < V_G < 4 V with a step size of 0.2 V). I_D–V_G data was measured at periodic intervals (every 30 min for Fig. 1 and 90 min for Fig. 2.) and V_T extraction was performed (as shown in Fig. 1) when the entire bias stress experiment completed (usually lasting 8–12 h).

For initial experiments, the TFTs were stressed with a bias on the gate terminal and the drain and source terminals were kept grounded. The results presented in Fig. 1 (where ΔV_T was extracted at V_D = 0.5 V) appear to corroborate the defect pool model, i.e., (1) where a linear relationship is observed between ΔV_T and (V_ES–V_T) and ΔV_T has a power dependence on bias stress time (β ≈ 0.3). The ΔV_T results shown in Fig. 2 are for TFTs where a bias voltage is applied to both the TFT gate and drain terminals. Here, to achieve greater experimental accuracy, the total number of I_D–V_G curve measurements in the bias stress experiment was reduced by collecting I_D–V_G curve data at longer 90-min intervals. The results in Fig. 2 support the dominance of the defect creation mechanism in TFTs with nitrogen-rich gate dielectrics [12] (as are the TFTs in this study) and for small stress voltages (<15 V).

Unlike the linear mode of TFT operation where a uniform channel exists in the a-Si:H layer, the presence of an increasing bias on the TFT drain terminal increases the lateral electric field and decreases the carrier concentration in the channel near the drain. Around V_DS = V_GS–V_T, the TFT enters the saturation mode of operation beyond which the carrier concentration in the channel remains approximately constant. Investigations into the dependence of ΔV_T on V_GS and V_GD show that the ΔV_T for a TFT entering saturation is smaller than that in the linear mode at the same gate bias voltage (see Fig. 2). Driving the TFT deeper into saturation (i.e., V_DS > V_GS–V_T or as V_GD < V_T) appeared to have little effect on ΔV_T. This can be seen in Fig. 2 where the TFT drain voltage is increased from V_DS = 15 V to 30 V (i.e., V_GD is changed from 0 to –15 V) while the gate bias is maintained at 15 V. If the defect pool model is considered (where ΔV_T is proportional to the number of carriers in the conduction band tail states), the decrease in TFT channel charge in saturation may help explain the smaller ΔV_T as compared to that in the linear region. Further, since once the TFT is saturated, there is no significant change in the concentration of channel charge as the TFT is driven further into saturation, the change in ΔV_T is negligible. Since ΔV_T appears to vary with the induced channel charge, simple MOS equations for channel charge are employed to develop a rudimentary ΔV_T model for a TFT operating under gate and drain bias voltages. For a given V_GS, the maximum number of carriers in the TFT channel occurs in the linear mode and assuming a uniform channel where V_GS = V_GD, the channel charge is given as

\[ Q_{CG} = C_G \cdot W \cdot L \cdot (V_{GS} - V_T) \]  

(2)

where C_G is the TFT gate capacitance per unit area, W the transistor width, and L the transistor length. Alternately, when a bias is applied at both drain and gate terminals, the charge stored on the gate can be expressed as [13]

\[ Q_G = \frac{2}{3} C_G W L \left( \frac{V_{GS} - V_T}{V_{DS}} \right)^3 \left( \frac{V_{GD} - V_T}{V_{DS}} \right)^3 \left( \frac{V_{GD} - V_T}{V_{DS}} \right)^2 \]  

(3)

Equation (3) reduces to (2) in the limit when V_GD → V_GS, which signifies the transistor entering the linear region. On the other hand, as V_GD → V_T (i.e., the transistor enters the saturation region), (3) reduces to 2/3 of the expression shown in (2). The relationship between normalized channel charge and ΔV_T was determined to be linear with a maximum discrepancy of around 10% as shown in Fig. 3 where the ΔV_T data from Fig. 2 was replotted.

Fig. 2. Dependence of ΔV_T on V_GS and V_GD. The value extracted for β is 0.3. The solid lines represent the model shown in (4).
Following the observed dependencies of $\Delta V_T$ on TFT bias, (1) can be suitably modified to include the effect of drain voltage by determining the ratio of the channel charge for given $V_{GD}$ and $V_{GS}$ bias values to that in the linear mode of operation

$$\Delta V_T(t) = \left( \frac{Q_G}{Q_{GO}} \right) A (V_{GS} - V_{T1})^\beta.$$  

Here, $Q_{GO}$ is defined in (2), $Q_G$ in (3), $V_{ST}$ has been replaced by $V_{GS}, V_{T1}$ by $V_T$, and again, $A$ and $\beta$ are temperature dependent parameters. Since $\Delta V_T$ is proportional to the normalized channel charge, the maximum (in linear mode) and minimum (in saturation mode) values for channel charge set the upper and lower limits of $\Delta V_T$ at a given $V_{GS}$. The developed $\Delta V_T$ model in (4) can be used to predict the stability performance of a-Si:H analog circuits for a variety of emerging a-Si:H TFT applications.

References


