Electrostatic Self-Assembly of Raised Surface Micromachined Structures for Optics

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ABSTRACT

This thesis critically analyses current surface micromachining processes. As the only readily available commercial process, special emphasis is placed on the MUMPs process, which is provided by Cronos. Using a wide array of devices, this thesis looks closely at design issues that affect functional yield and reliability.

Following the general look at surface micromachining, the knowledge is applied to a number of structures that are important for micro-optic systems. Large systems require that the individual components be highly engineered, so this thesis begins the task by carefully evaluating the implementation of simple designs.

Device-specific theory is then developed for micro-optic devices. Theory for the ideal operation and characteristics of these devices is provided. This thesis also outlines where, because of fabrication process limitations, devices depart from ideal operation. Both analytical and numerical tools are used to model these optical components.

A novel method of assembling surface micromachined components is presented. The assembly process uses electrostatic forces to create a series of attractions amongst the components. The component requirements and process steps are detailed along with the necessary theory.

As an example of the self-assembly method, a design for a 2x2 fibre-optic switch is presented. The design contains a number of features not possible with conventional surface micromachining and assembly methods.

DEDICATION

The thesis is dedicated to all those who travelled before me, who travel with me, and hopefully will travel behind me.

ACKNOWLEDGEMENTS

First and foremost, I'd like to acknowledge the support and advice of Dr. Ash M. Parameswaran, my supervisor. Extremely approachable, he was always available when I needed help. He is a great teacher, supervisor, and person.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1
INTRODUCTION

Microfabrication, as its name suggests, is the field of manufacturing microscopic devices. The most widely known field of microfabrication is microelectronics, which is the field of manufacturing microscopic electronic devices and systems. Although less well known, other fields of microfabrication have many important applications. In particular, the field of micromachining is currently a topic of much research interest.

Commercial successes in micromachining are still few. However, there are a number of large markets where micromachined components are strong players [1]. Examples included inertial sensors and inkjet print heads. More importantly, the number of emerging markets is quite large, and includes displays, data storage, chemical microanalysis, biological microanalysis, medical diagnostics, and drug delivery.

Common acronyms for microfabrication include micro-systems-technology

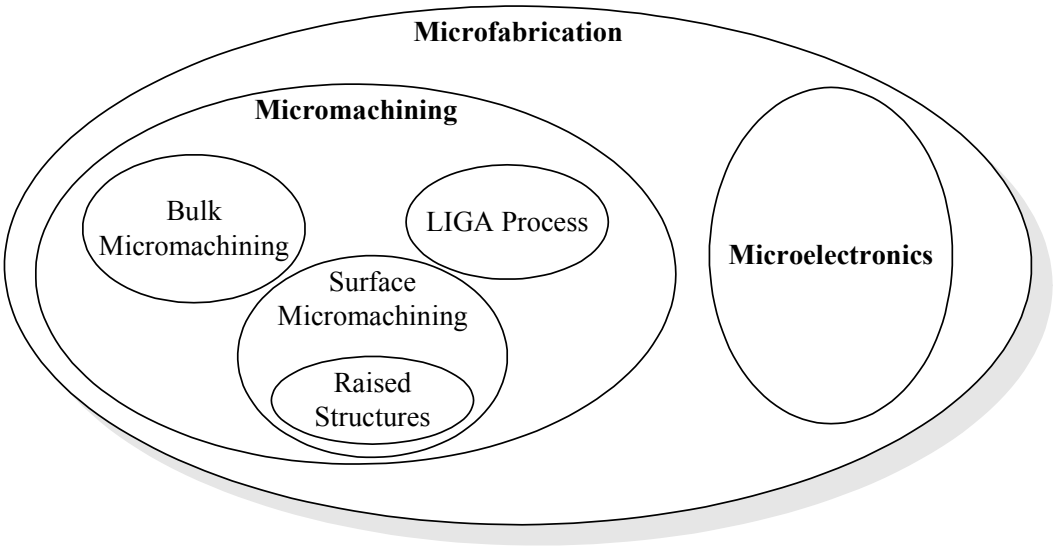

Figure 1: Relationship amongst various fields of microfabrication.

(MST) and micro-electro-mechanical systems (MEMS). While these terms are commonly used, terms like microelectronics and microfabrication are more widely recognizable, despite less common use in trade journals. The use of microfabrication, and related words, is also advantageous as these words clearly relate fabrication technologies to their macroscopic counterparts.

Compared to the field of microelectronics, the range of processes used in micromachining is very large. There are currently three main micromachining technologies: bulk micromachining, LIGA[1] [2], and surface micromachining. The focus of this thesis is surface micromachining. In particular, this thesis focuses on a subset of surface micromachining concerning raised structures. The most common use of raised structures is for free-space micro-optic-bench (FS-MOB) technology (Figure 1).

The fabrication of raised structures starts with surface micromachined components. Additional steps assemble the micromachined components into structures that are much taller than is possible with surface micromachining alone. The existing assembly processes have a number of disadvantages. Despite these disadvantages, interest in raised structures continues because of the important applications that are possible. For example, it is possible to build optical switches using raised structures.

This thesis presents a novel method, which uses electrostatic forces, for assembling the surface micromachined components. Using electrostatic forces presents a number of advantages over existing methods of assembly. First, it does not require physical contact with the miniature components. Second, it does not introduce additional materials into the system. Third, assembly of many devices can be done in parallel.

As a proof of concept, this method is used in the design of a 2x2 optical switch for fibre-optic systems. Although a completed fibre-optic switch has yet to be assembled, the performance of the electrostatic assembly method has been tested.

[1] LIGA is a German acronym for Lithography, Galvanoforming, and Plastic Moulding.

1.1. MOTIVATION

The performance of long-distance telecommunications systems based on fibre-optic trunks is, in large part, dependent on the quality of optical components available. In particular, cross-connect switches presently create a bottleneck for optical communications. Optical signals are converted to electrical signals, switched using high-speed electronics, and then converted back into optical signals for further transmission.

With the development of Erbium-doped fibre amplifiers (EDFA), electronic switches remain the largest electronic systems within optical networks. The goal of all-optical transmission networks has since become a goal of long-distance communication providers. Such a system would lead to reduced system complexity and increased performance [3].

Achieving all-optical networks, however, has been impeded by the unavailability of good optical switches. Current designs are notoriously large and unreliable. This makes current optical switches unacceptable for large cross-connects. One approach to the fabrication of smaller optical switches is micromachining. Much research is thus focused on micromachined optical systems. Researchers are pursuing designs using both bulk micromachining and surface micromachining. These devices should increase the reliability and reduce the size of the cross-connect switches.

Fortunately, micromachining research has provided a wide range of micro-optic systems [4] [5]. Micromachining, and in particular surface micromachining, is well poised to provide the desired miniature optical switches.

1.2. SURFACE MICROMACHINING

Surface micromachining is very closely related to the microelectronics[2] industry. Like microelectronics fabrication, the process starts with a silicon wafer. The fabrication process consists of mainly planar processes. That is, the fabrication steps generally only affect the top surface of the wafer. Photolithography is used extensively to control where each process affects the wafer surface.

Surface micromachining is an additive process that uses patterned thin films. Most fabrication steps consist of depositing a thin film onto the wafer, and then patterning the newly deposited thin film using photolithography. The devices are thus fabricated as a series of patterned layers.

While other materials may be present, the core of this fabrication process depends on just two core materials. The first core material is used to construct all of the structures that will be part of the completed devices, and as such is called the structural material. The second core material is used as a spacer, and is used to create vertical spaces between different structural layers. Near the end of the fabrication process, the second material is removed by a selective etchant, releasing the structures. The second core material is often called the sacrificial material[3].

A very important attribute of surface micromachining is that it is a thin film process. This constrains the types of components that can be fabricated, since the components must also be thin. However, surface micromachining can fabricate hinges. Hinges allows components to be fabricated flat, but raised after release through rotation. While the components must be thin, the assembled structure can be quite high. The original paper on raised structures [6] used the technique to create free-space microscopic optic systems, or free-space micro-optic-benches (FS-MOB).

[2] The microelectronics industry is also known as the integrated circuit (IC) industry. The term microelectronics is used in this thesis to highlight its relation to other microfabrication technologies.
[3] While several material combinations are possible, classically the structural and sacrificial materials are polysilicon and silicon dioxide, respectively.

1.3. MUMPs Process

A particular surface micromachining process is the Multi-User MEMS Process[4] (MUMPs), which uses poly-crystalline silicon as the structural material, and silicon dioxide as the sacrificial material [7]. In addition to thin films made from the two core materials, silicon nitride and gold films are also present. The thin films used in the fabrication process are listed in Table 1.

Film Name	Material	Thickness (μm)	Lithography Mask Name
Insulator	Silicon Nitride	0.6	
Ground Plane	Polysilicon	0.5	POLY0 (HOLE0)
First Sacrificial Layer	Silicon Dioxide	2.0	ANCHOR1, DIMPLE
First Structural Layer	Polysilicon	2.0	POLY1 (HOLE1)
Second Sacrificial Layer	Silicon Dioxide	0.75	ANCHOR2, P1P2VIA
Second Structural Layer	Polysilicon	1.5	POLY2 (HOLE2)
Metal	Gold	0.5	METAL (HOLEM)

Table 1: Thin films present in the MUMPs process.

In addition to sacrificial and structural layers, the MUMPs process contains three other layers: insulator, ground plane, and metal. Each of these thin films provides an additional important design feature.

1.3.1. Insulator

The insulating layer is required because the MUMPs process starts with a fairly conductive silicon wafer[5]. If different voltages are to be applied to different devices on the chip surface, then the devices must be insulated from each other. This is not possible when all components are electrically connected through the wafer.

[4] Cronos, 3026 Cornwallis Road, Research Triangle Park, North Carolina, 27709, USA.
[5] Resistivity is 1-2 Ωcm [7].

Before depositing the sacrificial and structural films, a silicon nitride thin film is deposited. Since silicon nitride is an insulator, all devices are electrically isolated from the wafer bulk[6].

1.3.2. Ground Plane

Because the vertical distances are so small, small voltage differences between thin films can lead to very large electric fields. This includes voltage differences between devices and the wafer bulk. If these voltage differences are present, the electric fields will create strong forces that pull the structural layers down to the wafer surface, where they will adhere. Devices that have adhered to the wafer surface are no longer free to move.

Ensuring that the voltage difference is very small can prevent adhesion. However, the entire wafer bulk, because of its relatively high conductivity, must be kept at the same voltage. Depending on what voltages are applied to the micromachined devices, local fields will still develop. Instead, a localized solution is needed.

A ground plane provides electrical shielding between the micromachined devices and the wafer bulk. Because it can be patterned, the ground plane can be broken up into electrically isolated islands, which can then be connected electrically so that there is no voltage difference between the ground plane and any devices immediately above.

While the ground plane is made of polysilicon, it is attached directly to the wafer surface. Therefore, it can never be released. So while the ground plane is made from the structural material, it is not often considered to be a structural layer.

[6] Stating that all structures are insulated from the wafer bulk is not strictly true. Although there is no mask for patterning the nitride layer, there are conditions where the nitride layer will be etched away and contact with the wafer bulk can then be made.

1.3.3. Metal

The polysilicon used for the ground plane and structural layers is heavily doped[7]. However, for conductivity there is no competing with metal. To provide low resistance interconnects, the MUMPs process has a gold thin film[8].

1.4. REFERENCES

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[7] David A. Koester, Ramaswamy Mahadevan, Busbee Hardy, & Karen W. Markus. MUMPsTM Design Handbook: Revision 6.0. Cronos, Research Triangle Park, 2001.

[7] Resistivity varies between 1 and 45 Ω/square [7].
[8] Resistivity varies between 0.05 and 0.07 Ω/square [7].

CHAPTER 2
TECHNIQUES FOR SURFACE MICROMACHINE DESIGNS

2.1. INTRODUCTION

In the process of my thesis work, it has become obvious that there exists a severe hole in the current documentation on device design. In articles and in books, authors approach the subject from one of two directions: processing knowledge or device knowledge. These two approaches neglect an important bridge between the fabrication process and actual device implementation.

A large skill set that is broadly applicable is required to design surface micromachined devices. These skills are basic tools that designers must possess if they are to successfully implement any device design.

New designers should first understand the processing steps involved in surface micromachining. They should then build upon this knowledge by learning the basic design techniques, which will be outlined in this chapter. Finally, new designers should learn any specific device knowledge and theory required for their project. Figure 2

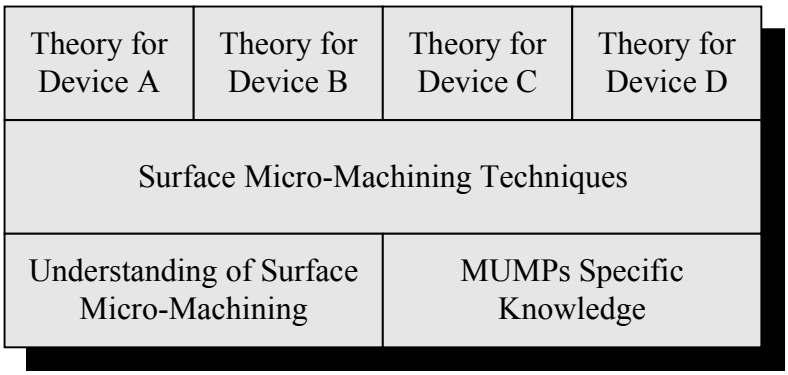

Figure 2: Knowledge layering for surface micromachined devices.

outlines this hierarchy.

The introductory chapter presented a basic introduction to surface micromachining and, in particular, the MUMPs process. This chapter will fill in the middle layer shown in Figure 2. The surface micromachining techniques presented here will fall under two categories: process techniques and design techniques.

As an aside, an understanding of the relative importance of physical phenomena at microscopic scales is very important[9].

2.2. PROCESS

Simply knowing the nominal thickness of the thin films is insufficient to reliably produce surface micromachined devices. The type and quality of thin film deposition will impact the final structure through a number of effects: conformal topography, thin film stresses, process variations, and surface adhesion. How these issues affect device operation are covered in this section.

2.2.1. Conformal Topography

In the MUMPs process, all growth is conformal[10]. The result of any processing step depends heavily on the preceding steps. Managing topography is an important part of the design process. Generally, design faults relating to topography can be classified into three categories: interference faults, structural faults, and behavioural faults.

In rare cases, the steps that follow can also affect deposited layers. An example of this is described in Section 2.3.2 of the MUMPs Design Handbook [4].

[9] The standard reference on scaling laws for microfabrication appears to be a paper by W.S.N. Trimmer [1]. The material can also be found in the book Fundamentals of Microfabrication [2], in chapter 9.

[10] In conformal deposition, film growth along side-walls and flat surfaces is equal. An important feature of conformal deposition is that topography is transferred to subsequent thin films as they are deposited.

2.2.1.1. Interference Faults

The first category of design faults consists of interference faults. During deposition, thin films conform closely to the topography of the previously deposited and patterned layers, and so are not necessarily planar. Often, the topography can trap a structure that was intended to move freely. Unless the preceding layers are designed to ensure the upper structural layers are flat where needed, the induced topography can have detrimental effects on device operation.

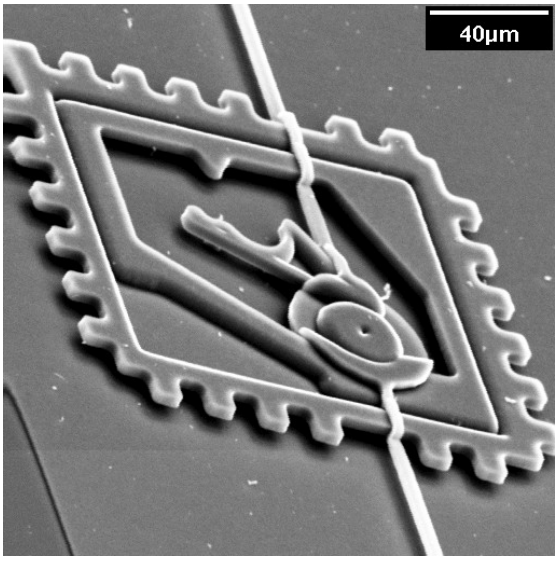

Figure 3: Part of bi-stable switch design with rod trapped by conformal deposition [3].

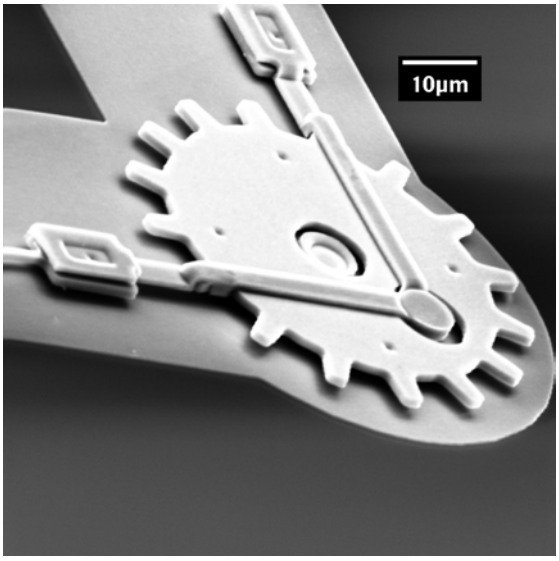

Figure 4: Motor design with two rods trapped by conformal deposition [3].

Above are two examples of devices with interference faults. In Figure 3, the beam extending past the top and bottom of the image was supposed to move up and down. Notice how the beam is folded over the edges at the two locations where it first meets the perimeter of the square structure. The beam clearly cannot move. Further, the device's pin (circular piece) has conformed to the path, effectively immobilizing it as well.

Figure 4 shows a similar problem. While the pin appears to be properly formed, the two connecting beams have conformed to the gear's teeth, preventing rotation. A redesign of this gear is shown below in Figure 6.

Figure 5 shows a different type of interference fault. Here, the staple is supposed to keep the beam close to the wafer surface. This type of support can be necessary to prevent damage during fabrication and release. However, the staple has conformed over the rod and prevents any lateral motion. Although not discernable from this image, the device requires that this rod be capable of lateral motion.

Processes other than MUMPs, for example SUMMiT[11], may planarize[12] the wafer after key steps. Certainly, the need for planarization increases with the number of structural layers. However, unless the wafer is planarized once for each structural layer, topography will still need to be managed.

[11] SUMMiT is an acronym for Sandia Ultra-planar, Multi-level MEMS Technology.
[12] Planarization is a process that aims to create a flat surface across the entire wafer. Planarization involves growing an extra thick film or growing a spacing layer, and then using a chemical-mechanical process to polish the wafer to obtain a flat surface.

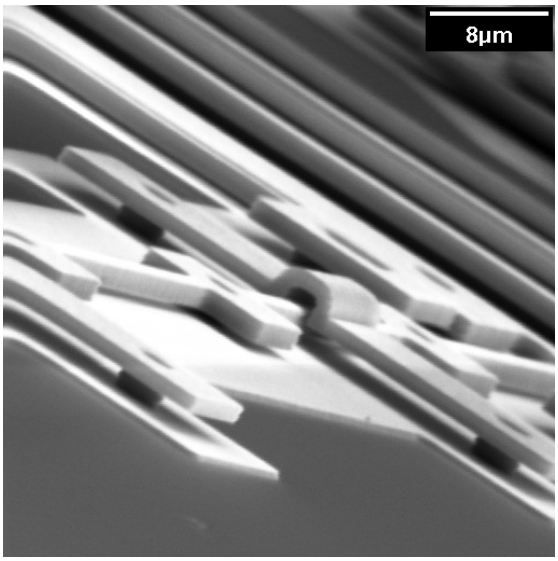

Figure 5: Staple interfering with lateral motion of a rod [3].

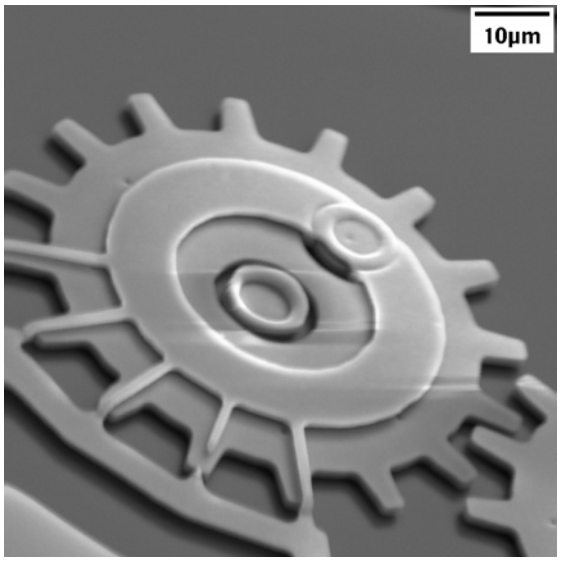

Figure 6: Gear redesigned to avoid interference faults, but now showing structural faults.

2.2.1.2. Structural Faults

Structural faults, the second category, occur when the topography creates a structural weakness in the fabricated device. Not only can the topography create stress concentration points, but beam thinning may also occur due to variations in thin film thickness across steps. These problems are compounded since lithography is more difficult at height changes. At least in the MUMPs process, minimum-width beams crossing significant steps are likely to break.

While the design shown in Figure 6 has removed the interference faults shown in Figure 4, the design now has structural faults. This is the cause of the break in the fourth connecting beam. Fortunately, this device may still work. Using more than one connecting beam has provided a measure of redundancy. Further, the use of multiple connections provides structural support, which reduces the chance that any individual beam will break.

2.2.1.3. Behavioural Faults

Behavioural faults make up the third category. A behavioural fault occurs when a device's shape changes its functional properties. For mechanical structures, this often means changes in the compliance.

Figure 7 shows two electro-thermal actuators. The top actuator is supposed to move upwards when power is applied; the bottom actuator should move downwards. The top actuator has a behavioural fault.

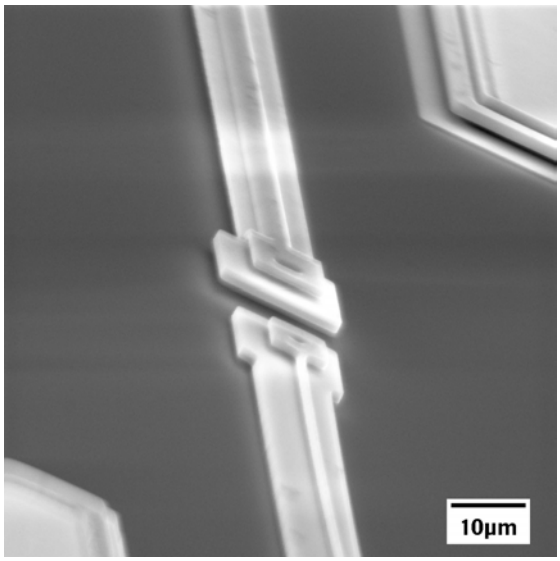

Figure 7: Picture of vertical electro-thermal actuator.

Like the bottom actuator, the top actuator is composed of a wide arm and narrow arm. Differential heating due to an applied current causes differential thermal expansion. The differential thermal expansion was supposed to cause the tip of upper arm to move upwards. However, the wide arm's topography is not flat. The narrow arm was deposited first, and the wide arm conformed over the narrow arm during deposition. Since the wide arm is not flat, its bending stiffness is significantly greater than desired, reducing any motion.

The bottom actuator, except for the fact that it is stopped by the wafer surface, works as expected. While the design is essentially the same, the reversed roles of the two beams have ensured that both arms of the actuator are flat.

Another good example of behavioural faults is when mirrors are placed on top of other structures. Unless care is taken, the buried structures will lead to height variations on the mirror's surface because of conformal deposition. These height variations are behavioural faults since mirrors should be flat.

2.2.2. Thin Film Stresses

Unfortunately, the thin films that comprise surface micromachined structures will have built-in stresses. Residual stresses can be attributed to a large number of factors, not all of which are fully understood, which means they cannot always be well controlled. Residual stresses lead to shape changes when the devices are released. These changes include simple expansion and/or contraction of components, but may also include bending.

While not all the causes of residual stress are understood, one important cause is thermal expansion. Differences in the coefficients of thermal expansion (CTE) amongst materials are perhaps the easiest source of residual stress to understand. If the films are considered to be unstressed at the deposition temperature, then the residual stresses are the result of cooling the wafer to room temperature. Since the materials have different CTEs, they will shrink by different amounts during cooling. When the wafer bulk is much thicker than the thin films, it can be considered essentially rigid. Since the films are evenly attached to the wafer surface, the thin films must therefore stretch (tensile stress) or shrink (compressive stress) to match the dimensional changes of the wafer.

To predict how thin film stresses will lead to shape change, a basic understanding of the relationships between stresses and strains is required. The basic theory is fairly simple and can be obtained from almost any elementary structural mechanics textbook.

Residual stresses perpendicular to the wafer surface are usually ignored in surface micromachining. Since structures are not constrained in this direction, their dimensions are free to move to their relaxed state. Because the structures are thin, vertical dimensional changes are usually negligible. Because they are relaxed, the stress is zero.

However, stresses parallel to the wafer surface can have significant consequences for devices. Many structures are large enough in this plane that dimensional changes are significant. Stress effects, such as buckling or curling, occur regularly. The effects of

residual stresses are typically understood in terms of the uniform stresses and the gradient stresses.

Since the wafer bulk is essentially rigid, thin film stresses are typically measured by comparing the film's strain against the bulk of the wafer.

2.2.2.1. Uniform Stresses

The uniform stress is the average stress through the thickness of the film. While it may be unsafe to consider it constant across the entire wafer, it should be slowly varying. For singly supported structures, one should expect a dimensional change as the structure relaxes to a non-stressed state (Figure 8). Doubly supported structures can be more reliable, since their length will remain fixed. However, compression over a critical compressive stress will cause doubly supported structures to buckle.

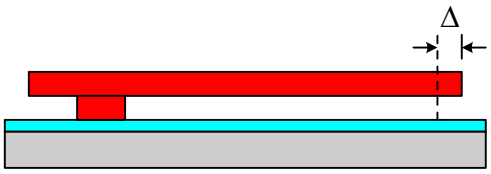

Figure 8: A singly supported structure (cantilever) showing dimensional change [5].

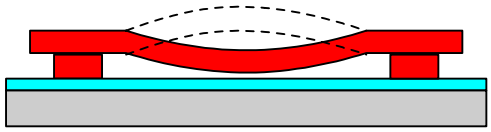

Figure 9: A doubly supported structure (Euler column) showing buckling [5].

Fortunately, the uniform stresses of the various films are somewhat controlled. Table 2.8 in the MUMPs Design Handbook [4] outlines the expected range of the residual uniform stress in the structural layers of the MUMPs process. The residual stresses are measured for each fabrication run and publicly posted.

For a singly supported structure, the dimensional changes that result from a given stress can fortunately be easily calculated. The change in length can be determined by using the following formula:

$$\varepsilon = \frac{\sigma}{E} = \frac{\Delta}{EL} \qquad (1)$$

In this formula, ε is the thin film stress[13], σ is the thin film strain, E is Young's modulus, Δ is the change in length of the cantilever, and L is the unsupported length. Since the material properties (ε, E) are known process parameters, and L is a design parameter, the expected change in the cantilever's length can be determined. Please note that in equation (1), the nominal dimensions correspond to the stressed state. Released structures will have a length change negative to that calculated using equation (1).

For doubly supported structures, the key parameter that needs to be considered is the critical buckling stress. If the film's stress is compressive, and exceeds the critical strain, the structure will buckle (Figure 9). The critical bucking strain can be determined as follows.

$$\varepsilon_{CR} = \frac{\pi^2 t^2}{3L^2} \qquad (2a)$$

$$\sigma_{CR} = \frac{E\pi^2 t^2}{3L^2} \qquad (2b)$$

In equation (2a), ε_{CR} is the critical buckling strain, t is the film thickness, and L is the unsupported length of the beam. Alternatively, one can use equation (2b), in which σ_{CR} is the critical buckling stress, and E is the modulus of elasticity. For the MUMPs process, doubly supported beams as short as 210 μm may buckle.

For doubly supported structures, the two supports must provide sufficient force to either provide the required dimensional change or the buckling strain. Otherwise, one of

[13] By convention, positive values for the stress are tensile. Negative values are compressive.

the supports will fracture. Unlike the singly supported structure, the structural strength of the supports may come into question.

Beyond any dimensional changes, residual stresses will continue to affect the dynamic behaviour of any devices. Through effects such as strain stiffening, the residual stress will change mode frequencies.

To determine the dimensional changes in more complex structures, numerical modeling may be required. The software for structural simulations is well developed and the simulations are relatively easy to configure and run.

The fabrication process does not oversize or undersize design components to account for these dimensional changes. Designs need to be robust enough to work with the range of residual stresses that may be present in the end result.

2.2.2.2. Non-uniform Stresses

Changes in the substrate temperature during film deposition, changes in the stoichiometry, changes in material density before annealing, and other effects, will lead to changes in the film's strain throughout its thickness. This is equivalent to an applied bending moment on the layer. When structures relax upon release, they will have a curvature.

The net bending moment can be calculated using equation (3).

$$M = \int_0^t \sigma(y) w \left(y - \frac{t}{2} \right) dy \qquad (3)$$

In equation (3), M is the bending moment, σ is the film stress at height y, w is the width of the structure, and t is the film's thickness. While valid, equation (3) may not be of much direct use as knowledge of the stress distribution, $\sigma(y)$, will be difficult to obtain. However, experimental methods, which may include test structures, may be able to provide an empirical value for the net bending moment.

If the bending moment is known, the deflection of a singly supported structure can be predicted relatively easily. As the structure will have a uniform bending moment throughout its length, the relatively well-known beam deflection formula can be used.

$$\delta(x) = \frac{Mx^2}{2EI} \tag{4}$$

$$\delta(x) = \frac{M(1-\upsilon^2)x^2}{2EI} \tag{5}$$

Where δ is the beam's deflection, M is the bending moment, x is the distance from the structure's support, E is the modulus of elasticity, I is the moment of inertia, and υ is Poisson's ratio. For thin beams, equation (4) should be used. However, if the beam is considerably wider than the film thickness, then the biaxial modulus of elasticity should apply, which leads to equation (5).

Non-uniform stresses are more troublesome than uniform stresses. They are both more difficult to handle theoretically and more difficult to measure. While Cronos limits the residual uniform stresses (specified in their Design Handbook) and measures them for each fabrication run, no equivalent controls are placed on non-uniform stresses.

Gradient stresses are always present, and can be severe enough to impede device operation. For example, Figure 10 illustrates a beam that was supposed to be able to move sideways. The beam has, however, curved up into the space created by its topography. As structures, including beams, reach lengths of 100μm, curvature becomes significant.

More commonly, non-uniform stresses affect gears and mirrors, where they cause bowing. While the radius of curvature will be less in these essentially 2D structures than the equivalent 1D rods, the effects can be more troublesome. For gears, excessive

bowing will cause teeth to slip. For mirrors, bowing will preclude their use in most optical applications.

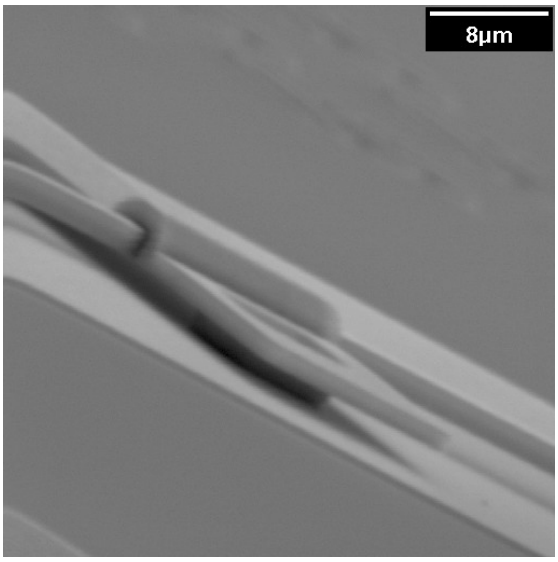

Figure 10: Beam, which, due to non-uniform stresses, has curled up, preventing sideways motion [3].

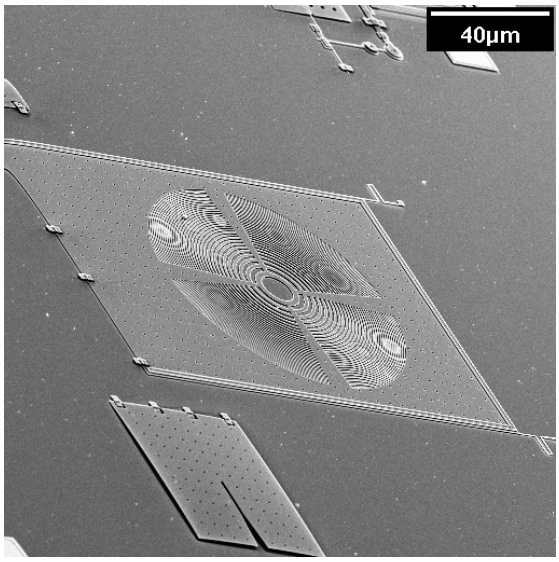

Figure 11: Fresnel-zone plate, which is relatively flat compared to its vertical support [3].

Figure 10 shows a beam with convex curvature. This figure is related to Figure 5 as the staple is causing an interference fault. However, the problem is compounded in this case by the beam's curvature, which pushes the beam up into the space created by the conformal deposition of the second structural layer. Even if the second layer were flat, the curvature would probably push the beam against the staple. The likely result would be adhesion and thus the immobilization of the beam.

Where flatness is required, some steps can be taken to reduce curvature. Notice how in Figure 11 the Fresnel-zone plate is considerable flatter than its vertical support. Since the plate is significantly larger, one would expect a larger deflection. However, the designers have reduced the curvature by stiffening the plate. The second structural layer was used around the plate's edges to increase its thickness.

In addition to gradient stresses intrinsic to the individual thin films, it is possible to create effective stress gradients when multiple films are used together. This is particularly true for structures with two different materials. For example, in the MUMPs process, the gold layer is always tensile while the polysilicon is always compressive [4]. When METAL and POLY2 are combined, the resulting structure will always have a bending moment, which may be quite large. This is the cause of the bending of the cantilevers shown in Figure 12. The devices, which are electrical relays, do not work because the actuation distance has been dramatically increased.

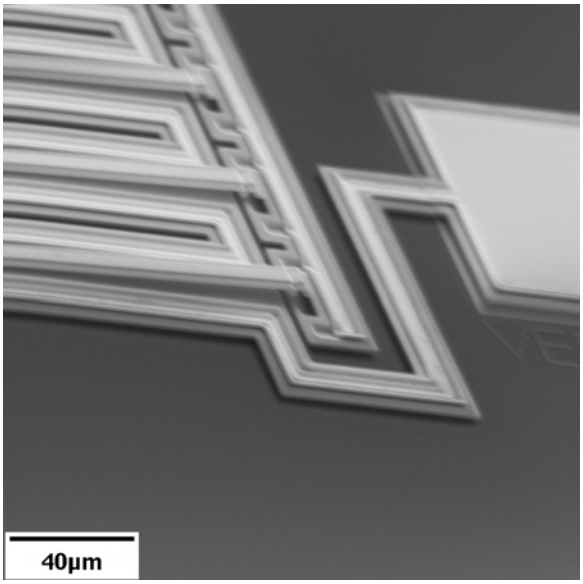

Figure 12: Cantilevers made from POLY2 and METAL. The resulting structures have large bending moments.

Designs for large structures will especially have to consider the effects of residual stresses. Because components will be spaced closely together in the vertical direction, even relatively large radii of curvature caused by non-uniform stresses can create interference faults.

2.2.3. Process Variations

Process variations can play an important role in the design of a system. The average thickness of the different layers can vary by more than ±10% from run to run[14]. There will also be variations across a die. Static and quasi-static structures can usually handle process variation by including a safety factor. Unfortunately, dynamic structures are sensitive to process variations.

[14] Table 2.8 in [6].

An important class of process variations are the thin film stresses just discussed. If control of thin film stresses is poor, then process variations will obviously be quite large.

2.2.4. Surface Adhesion

Since surface micromachined devices contain very small vertical distances, devices are not only flexible vertically, but contact distances are also very short. Additionally, the interfacial adhesion energy is very high for crystals, and is on the order of 500 to 2000 mJ/m^2 [7]. These two properties combine to make surface micromachined devices susceptible to adhesion[15]. Once contact has been established, very large forces are necessary to separate the surfaces.

In general, because of the relatively large surface area compared to volume of miniature devices, interfacial properties play a large role in micromachined devices. There exist many types of surface forces [8]: capillary force, electrostatic force, van der Waals force, solid bridging, and hydrogen bonding

Dimples are an important structure used to prevent adhesion, and will be discussed in the next section on design techniques. Dimples work by minimizing the amount of surface contact.

Reducing the interfacial adhesion energy can also prevent adhesion. Therefore, surface treatments can prevent surface adhesion. An important class of surface treatments are self-assembling monolayers (SAMs) [8] [9]. Perfluorodecyltrichlorosilane[16] (FDTS) and octadecyltrichlorosilane[17] (ODTS) are two important examples of SAMs.

[15] Often referred to as "stiction" in the micromachining literature
[16] $C_{10}H_4F_{17}SiCl_3$
[17] $C_{18}H_{37}SiCl_3$

2.3. DESIGN TECHNIQUES

Since surface micromachined devices are all made from thin films, and often from the same materials[18], many design issues are common to large collections of surface micromachined structures. This section will explain a number of these issues and how they are typically solved.

2.3.1. Design Rules

Since mask layout is common to both microelectronics and surface micromachining, both types of microfabrication design can often use the same tools. These tools include the design rule checker (DRC). DRC software looks through a design and makes sure that the geometry, which is spread across multiple mask layers, conforms to a finite number of rules. Design rules are set to ensure high device yield. Please refer to the appendices if you are unfamiliar with the types of rules that exist.

Finalized microelectronic designs rarely contain any design rule violations. However, designs for novel components often do contain design rule violations as part of the experimentation. Since micromachining is still a relatively immature technology, strict adherence to the DRC results is not possible. Understanding which rules may be broken, and the likely effects, is thus important to surface micromachining design.

2.3.1.1. Width and Spacing Rules

Designs that restrict themselves to meeting all of the nominal distances[19] for spacing and width should return from fabrication as designed. Barring serious processing errors during fabrication, the chips will return from fabrication with all features present.

Designs that restrict themselves to meeting the minimum geometry rules are on thinner ground, but in general can be expected to return from fabrication as designed. The main exception to the previous rule is thin parts (for example, beams) that traverse

[18] Polysilicon is the most common structural material.
[19] Nominal geometry rules include nominal width and nominal spacing rules.

regions with significant topography. As described in the section on structural faults, thin beams that cross over large changes in height (>1μm) are structural weak points that often break. Providing sufficient structural support can partially compensate for the structural weakness as well as provide redundancy.

The design rules for minimum width and minimum spacing should always be followed. Designs that violate minimum geometry rules will have missing, undersized, oversized or fused features. In particular, Cronos states that the minimum geometry rules for the MUMPs process are mandatory.

2.3.1.2. Overlap Rules

Overlap rules[20] exist to prevent extreme height changes, which will interfere with lithography, and to prevent unnecessary etching of underlying layers. For example, enclosure rules for anchors ensure that the anchors are completely covered by polysilicon. When enclosure rules are not followed, anchors can be partially exposed to subsequent etching during polysilicon patterning.

Despite the above, the enclosure rules are considerably more flexible than the width and spacing rules. While they certainly should be followed wherever possible, there exist many reasons to violate these rules. In particular, the MUMPs Design Handbook states that the enclosure rules are only advisory rules[21]. Users are free, at their own risk, to violate them.

2.3.1.3. Design Rule Checks

Design rule checks (DRC) are an excellent way to detect errors early and validate your design before submitting it for fabrication. Unfortunately, DRC technology for micromachining is immature and does not accurately check MEMS devices for functionality.

[20] Overlap rules include enclosure, cut-in, and cut-out rules.

[21] The Design Handbook also states that inter-level spacing rules are also advisory. However, this statement is considerably weaker. Inter-level spacing rules should be treated the same intra-level spacing rules, and thus should be mandatory.

First, there are several types of errors that DRC do not find. For example, DRC will not detect cases of minimum width beams crossing height changes that may constitute structural faults.

Second, there are several types of spurious errors that DRC may find. Most annoying is DRC software that cannot properly handle non-Manhattan[22] geometries. Where this is the case, curved edges can create thousands of spurious errors. Also, to prevent common beginner's errors, DRC rules often have checks on anchor and via layers. These rules will create errors wherever the nitride is breached (2.3.9 in [4]) or a double thickness structure is placed (2.3.10 [4]).

2.3.2. Ground Planes

The existence of the POLY0 layer in the MUMPs process is specifically for ground planes, which are necessary to electrically shield devices from the wafer. Any two conducting bodies at different potentials will experience an attractive force[23]; this includes surface micro-machined devices and the substrate. If the attractive force is strong enough, the device will be pulled down to the substrate surface. Even if the device does not adhere, significant friction will be present.

An electrical contact can be created near the device by breaching the nitride. However, breaching the nitride is not a guaranteed process and so presents reliability issues. Further, trapped charges may exist at the silicon to silicon-nitride interface. These charges will create electrical fields, which, through induced charges on the device, again lead to an attractive force. Ensuring that the substrate and devices are at the same voltage will not necessarily eliminate all electrical fields.

[22] Manhattan geometries consist of shapes in which all edges are aligned to the two axes. All corners are at right angles. If the shapes contain any corners that are not at right angles, or any curved edges, then it is not Manhattan.

[23] It is important to note that this refers to fixed voltage boundary conditions. As is well known, electrostatic forces can lead to repulsion, but only under fixed charge boundary conditions. This result for fixed voltages will be discussed in the chapter dealing with the electrostatic self-assembly.

Since the grounding plane is conducting, it cannot be placed indiscriminately; otherwise all electrical connections on the chip would be shorted. Since the main concern with substrate fields is the resulting adhesion and friction, only moving devices require a ground plane.

Ground planes should not be left floating. Unless their potential is fixed, they too can become a source of electric fields and attract devices. Many devices will actually have a voltage distribution, in which case one simply aims to reduce the attraction to a reasonable minimum.

Figure 13 shows two electro-thermal actuators, one that has a ground plane and one without. The actuator without the ground plane is no longer freestanding. Although not in view, the ground plane is connected only to the pin nearest the wide arm. This design is simple and sufficiently limits the attraction. However, this design does not completely eliminate the attraction, and may not be sufficient for larger dimensions. Because of the voltage distribution throughout the actuators, longer actuators will still experience enough attraction to reach the ground plane, where they will stick.

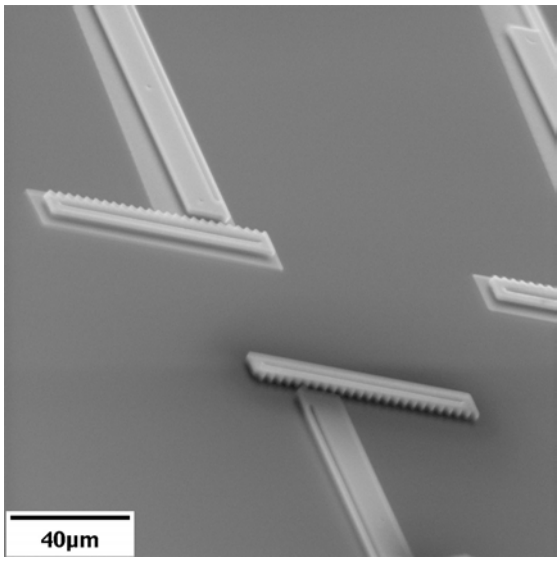

Figure 13: Electro-thermal actuator with ground plane.

2.3.3. Double Thickness Parts

In general, contact surfaces should be avoided in surface micro-machined devices because of the large relative strength of surface forces[24]. However, where contact surfaces are needed, the contact surfaces will likely need to be constructed from double-thickness parts. Because surface micromachined devices are so thin, they will

[24] Please refer back to section 2.2.4.

have significant vertical flexibility. Further, there may be bowing. To ensure that contact points stay in contact, double-thickness parts can be invaluable. While double-thickness parts are not guaranteed by Cronos, they are fabricated reliably.

At least in the MUMPs process, the main difficulty with double-thickness parts is the region of P1P2VIA that must surround them. The region can make the transition from double thickness region to single thickness regions tricky. Improper design easily leads to additional design rule violations and structural faults. Dealing with double-thickness parts can thus be a little awkward.

Figure 14 shows several surface micro-machined gears. The gear on the right has double thickness teeth, while the one on the left has single thickness teeth. Despite the relatively small size of the gears presented in Figure 14, the single-thickness teeth exhibit some offset. While the single-thickness teeth are meshing properly in this device, larger gears or a larger non-uniform gradient stress will lead to slippage. The double-thickness gears are more firmly in contact.

A close-up of the transition between single-thickness and double-thickness teeth is shown in Figure 15.

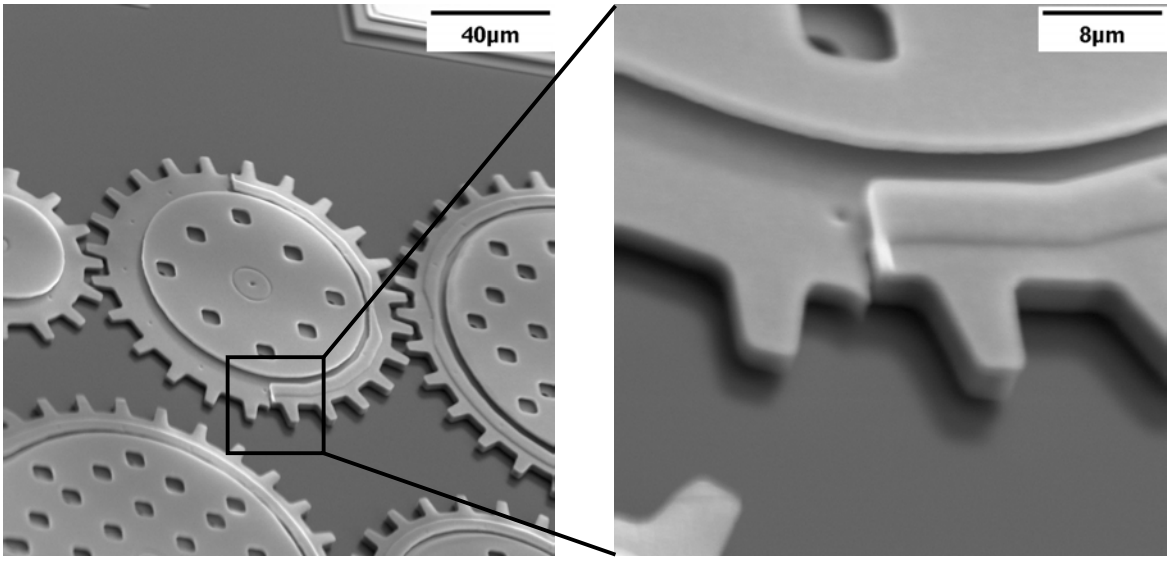

Figure 14: Image of single thickness and double thickness gears combined.

Figure 15: Close up of transition region between single and double thickness teeth of a gear.

2.3.4. Conducting Paths

Providing electrical signals is an important part of MEMS design. All of the polysilicon layers are heavily doped and have relatively low resistivities. However, when it comes to conductivity, they still cannot compete with metal. Thus, it is important to use metal in conducting paths whenever possible to lower path resistances.

Section 2.3.4 of the Design Handbook [4] specifies the layout for a pad. Many of the same issues that affect this supposedly simple layout also affect the design of conducting lines. Improperly designed conducting lines will break during the bonding process. With the exception of POLY0, all of the same layers should be present in conducting lines.

The widths of the conducting lines should be increased beyond what is required to meet design rules[25]. With the minimum widths, the topography at the centre of the conducting line is such that the metal deposition is affected, increasing the line's resistance. To ensure a low resistance, all widths should be increased by 2μm beyond what is necessary to meet design rules, as this ensures that the centre of the conducting line is flat. The suggested widths for each layer are listed in the Table 2.

[25] To include all of the layers in the conducting path and meet the design rules, the required width is 18 μm.

Layer	Width
POLY1	20
ANCHOR1	12
POLY2	12
P1P2VIA	4
METAL	6

Table 2: Recommend layer widths for MUMPs conducting line.

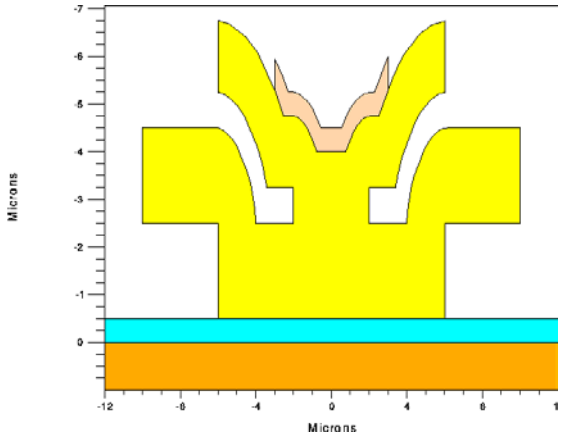

Figure 16: Structure of a conducting line after release.

The conducting line outlined here has a current limit of several 100 mA at room temperature[26]. Above this limit, the metal layer is damaged so that it can no longer carry any current. When this happens, the resistance of the conducting path increases significantly as the current must be carried by the polysilicon. While unlikely for micro-devices, if a larger current is required, one needs only to increase the width of the conducting lines to increase the current limit.

Sometimes it is necessary to use only polysilicon as a conducting path. This occurs when paths need to cross under or between other layers. When necessary, the resistance can be calculated from the geometry and the published resistivity data[27]. Obviously, wider paths are less resistive. Also, corners and contact methods can affect the resistance of the path.

2.3.5. Tethers

When designing structures to be raised, hinged components will flap around during release. This can damage the device itself as well as nearby devices. To prevent

[26] Result obtained through personal testing.
[27] Table 2.8 in [6].

this from happening, the device should be tethered to the wafer surface. These tethers are broken just before the device is to be assembled or used for the first time.

Although many techniques are possible, there exist three main methods of breaking the tethers. The most common method requires operators to break the tethers using a micromanipulator. The manipulator is dragged across the surface of the wafer and across the tethers. Alternatively, the manipulator is dropped on the tether's anchor, crushing it.

When breaking tethers in this manner, a buffer zone is required around the tethers. Unless sufficient space exists around the tethers, the probe needles will damage the surrounding structures. The tether should be at least 100μm long. There should be at least 50μm, and preferably 100μm, of surrounding space.

This technique is relatively easy to implement, and the necessary equipment exists in most clean and semi-clean facilities. While popular, this technique has several flaws. First, this technique obviously requires operator intervention. Second, this technique can create a significant amount of debris. It is virtually impossible to remove this debris, which may later contaminate other devices, and so cause devices to fail.

Another technique is laser ablation. While this avoids the debris, the necessary equipment is not as readily available.

A third technique is to design the tethers like fuses. A large current is passed through the tethers, which heats the tethers until they break. While this technique is easily automated and leaves little debris, it may not always be ideal. Since tethers are for freely moving structures, they will not be physically connected to the wafer. Ensuring a good electrical connection to the device may not be possible.

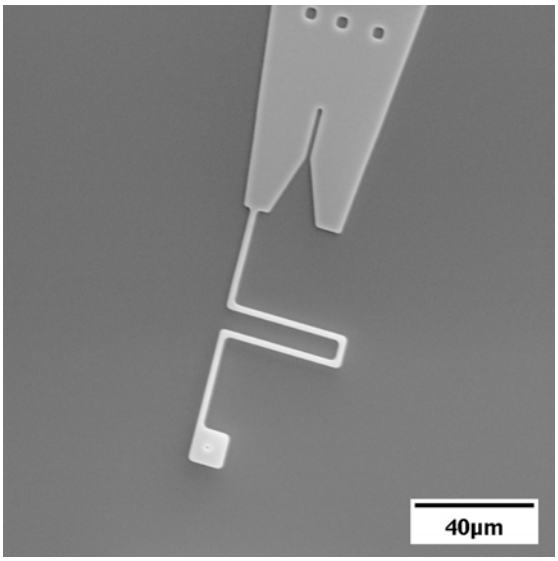

Figure 17: Tether holding the end of a vertical support.

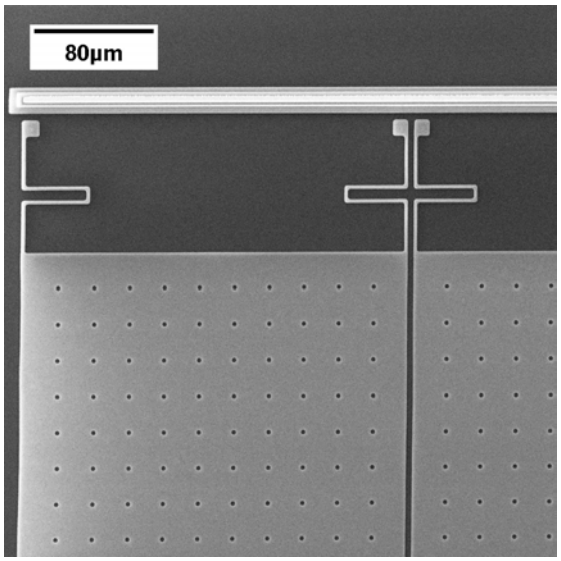

Figure 18: Tethers holding an array of mirrors.

2.3.6. Dimples

Dimples are small bumps on the underside of the first structural layer. A short wet etch is used to isotropically etch small 0.75µm cavities on top of the first sacrificial layer. The first structural layer will then have bumps, as it will conformally fill the holes. Because of the conformal deposition process, some measure of the dimples will also exist on the second structural layer.

Although there are many uses for dimples, their main purpose is to prevent adhesion. Whether or not a structure can be pinned to the surface through adhesion is determined by the elastic energy and surface energy of the structure. Elastic deformation of a structure stores energy, just like any conventional spring. Deforming a structure raises its potential energy. However, if the structure can be deformed so that it touches the wafer surface, and the surface energy lost is greater than the necessary elastic energy, then it is energetically favourable for the structure to remain collapsed.

For processes that undergo normal wet release and drying, ensuring that the collapsed state is energetically unfavourable is essential. During the drying process, capillary forces will draw structures down. While the drying process is itself highly dependent on the liquid's surface tension, the result after drying is completed depends only on the adhesive forces and structural elasticity. It is therefore is essential that the collapsed state is unstable.

For devices that use the super-critical drying method[28] [10], capillary forces no longer play a role. It is at least theoretically possible to successfully fabricate devices that would otherwise be pinned to the wafer surface. However, for reliability reasons, it is still better to ensure that the pinned state is unfavourable.

For a number of standard structures, the peel number can be calculated [7]. Structures will not adhere for peel numbers greater than one. For a doubly supported beam, the peel number is:

$$N_P = \frac{128}{5}\frac{Eh^2t^3}{\gamma_s l^4} \qquad (6)$$

In equation (6), N_P is the peel number, E is the modulus of elasticity, h is height of the beam from the wafer surface, t is the beam's thickness, γ_s is the interfacial adhesion energy per unit area, and l is the distance between the two supports. If the beam's height is much larger than its thickness, then a different formula, which can be found in [7], should be used. The interfacial adhesion energy is very high for crystals, and is on the order of 500 to 2000 mJ/m^2.

[28] Super-critical drying is used to remove the aqueous solution used in the release step. First, the aqueous solution is replaced with liquid methanol. Second, a high-pressure process replaces all methanol molecules with supercritical carbon dioxide molecules. The supercritical carbon dioxide, which is a solid, will sublimate directly to the gas phase, avoiding the capillary forces that accompany liquid-phase drying.

Other structures will have different formula for their peel numbers. Again, please refer to [7]. In particular, the required dimple spacing for plate will be different from the dimple spacing required for a simple beam.

For the MUMPs process, equation (6) can be used to calculate the maximum dimple spacing[29]. Since the boundary condition is $N_P = 1$, l can be at most 334 μm. However, equation (6) implies a completely fixed support, whereas a dimple only provides partial support. For this reason, and to add a margin of safety, dimples are typically spaced at 30 μm.

While it is important to ensure that enough dimples are present to prevent adhesion, their number should be minimized. Dimples in contact with the wafer surface may adhere, and so dimples can also be a significant source of friction.

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[29] E = 169GPa, h = 0.75μm, t = 2μm, and γ_s = 0.2J/m.

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CHAPTER 3
THEORY OF SELF-ASSEMBLY

3.1. INTRODUCTION

As a fabrication technology for MEMS, surface micromachining holds a lot of promise. Of the major micro-fabrication technologies, surface micromachining can most easily bring the huge expertise in silicon processing to bear on micromachining. The main difficulty with surface micromachining is that it is a thin film process. While this process excels at creating flat structures, structures with large vertical dimensions are difficult to manufacture.

Previous work [1] [2] [3] [4] has shown how structures with large vertical dimensions can be assembled using surface micro-machined parts. Using hinges along one edge of a plate allows that plate to be rotated out of plane with respect to the wafer. A useful arrangement is to support a single plate perpendicular to the wafer surface. Typically, two secondary plates, which are located on either side of the main plate, provide the support. The plates can be lifted from the surface using micromanipulators, and, with care, correctly positioned. This technique has proven useful, and has been used to build mirrors, Fresnel-zone plates, and complete optical systems.

However, the above technique has several disadvantages. First, using micromanipulators requires structures to be assembled manually. The work is delicate, must be performed under a microscope, and requires practice. In short, the operator must be skilled. Second, the technique does not generalize well. More complicated 3D structures probably could not be constructed using this technique. Third, and most important, the assembly must be done in series, defeating one of the big advantages micromachining provides for fabrication, parallel fabrication.

Besides manual assembly, there are presently three other important methods of assembly [5]. First, integrated motors can raise structures. Second, the surface tension of small molten droplets is enough to raise structures. Third, assembly can be done using polymer shrinkage [5]. The use of magnetic actuation has also been investigated [6].

This chapter presents a method for the assembly of surface micromachined parts that overcomes these disadvantages. Actuation is provided by electrostatic forces, which present a number of advantages. Further, the entire process can be automated using readily available IC manufacturing equipment.

3.2. ELECTROSTATIC THEORY OF SELF-ASSEMBLY

3.2.1. Electrostatics

Consider a square plate attached to the wafer surface by hinges along one edge (Figure 19). The plate and its hinges rest on top of an electrode. This plate, while free to rotate along the edge with the hinges, is held in place by gravity. If the plate is conducting, the plate can be moved so that it is perpendicular to the wafer's surface by providing a sufficiently strong electric field. The electric field will induce electrostatic pressure on the plate. To lift the plate, the opposite sides must see different electric field strengths, and so the plate must have a fixed potential.

The second electrode necessary for creating the electric field is a conducting plate, parallel to the wafer's surface. For reasons that will become clear later, this plate will be grounded. Applying a voltage between the ground plane and the plate will then create the electric field.

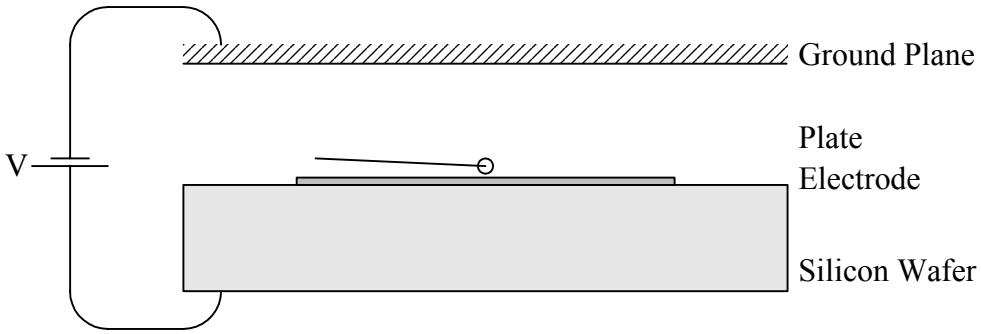

Figure 19: Configuration of wafer, surface micromachined plate, and ground plane used for electrostatic actuation.

The electrostatic pressure generated by this electric field can be determined as follows [8]:

$$P = -\frac{\varepsilon_0 E^2}{2} \tag{7}$$

$$F_e = PA = -\frac{\varepsilon_0 E^2 A}{2} \tag{8}$$

In equation (7), P is the electrostatic pressure, ε_0 is the permittivity of free space, and E is the component of electric field strength perpendicular to the surface, at the surface, of the conductor. The pressure is given a negative sign to indicate that unlike conventional pressure, which causes uniform compression (for example, hydrostatic pressure), electrostatic pressure causes uniform tension. For a two-dimensional structure that has an electric field on only one side, the total electrostatic force can be calculated using equation (8).

For the particular case under consideration and neglecting fringe effects, equation (7) can be rewritten as follows:

$$P = -\frac{\varepsilon_0 V^2}{2h^2} \tag{9}$$

In equation (9), the variables are defined as before. Additionally, V is the voltage applied to the plate, and h is the height of the grounded plane.

The electrostatic pressure must overcome the weight of the plate. Additionally, there may be friction at the hinges or adhesion between the plate and the wafer surface, but these additional forces will be neglected in this treatment for simplicity. This plate's weight can be easily determined from the geometry and material properties:

$$F_g = At\rho g \tag{10}$$

Where F_g is the force of gravity on the plate, A is the area of the plate, t is the thickness of the plate, ρ is the density of the plate, and g is the acceleration due to gravity.

Using the above equations, one can write the force balance equation for the plate. Using this equation, one can determine the voltage necessary to lift the plate.

$$F_g + F_e = F_g + AP = 0 \tag{11}$$

$$At\rho g - \frac{A\varepsilon_0 V^2}{2h^2} = 0$$

$$V_{lift-off} = \sqrt{\frac{2h^2 t\rho g}{\varepsilon_0}} \tag{12}$$

For example, a 2 μm thick plate of polysilicon with a grounded plane at a height of 0.5 mm would have a lift-off voltage of 50.5 volts. However, this value uses the parallel plate approximation, which will never apply. To avoid shorting, the ground

plane has to be high enough to be out of reach of the plate. This implies that, in at least one dimension, the plate's size is less than the plane's height and so the parallel approximation is not valid. Fortunately, when the ground plane is larger than the plate, the effect of fringing fields is to lower the required voltage as the field converges to the plate. The lift-off voltage will be lower than equation (12) implies.

If the plate were not fixed along one edge, it would accelerate until it impacts the ground plane. However, the hinges constrain one edge of the plate to the surface. The plate thus rotates until it is perpendicular to the wafer surface. With damping, it should settle to this position. In this state, the plate pulls at its hinges.

The above theory will be compared against numerical simulations. Since all charge distributions and electric fields vary linearly with the applied voltage, the system needs to be modeled at only a single applied voltage. However, since the applied force on the plate is due to electrostatic pressure, the force will vary with V^2.

$$F_e = \alpha V^2 \tag{13}$$

$$V_{lift-off} = \sqrt{\frac{At\rho g}{\alpha}} \tag{14}$$

Where F_e is the electrostatic force applied to the mirror, α is the constant of proportionality, and V is the voltage applied to the plate. Equation (13) should be compared to equation (9). The value of α can be extracted from the numerical simulations. Since total electrostatic energy of a system is easily determined numerically, the force can be determined by using the method of virtual work [8].

The value of 0.5 mm was chosen to ease the numerical simulation. In practice, the height of the grounded plane will be on the order of 0.5 to 2 mm.

3.2.2. Process

The electrostatic theory just presented can be used to assemble raised structures. The easiest structure to raise is a simple mirror. A layout for a simple plate is shown in Figure 20. The main square structure is the plate to be raised. In the particular case of Figure 20, the plate is actually a binary-amplitude Fresnel-zone plate. However, the assembly of any structure with a square frame is basically equivalent. The two semi-triangular components to each side of the plate are the vertical supports. When fully assembled, the notches at the tips of the vertical supports will mate with the plate.

Through the pads, the plate and the two vertical supports should be connected to external independent voltage sources. Figure 21 is a model of the device after release.

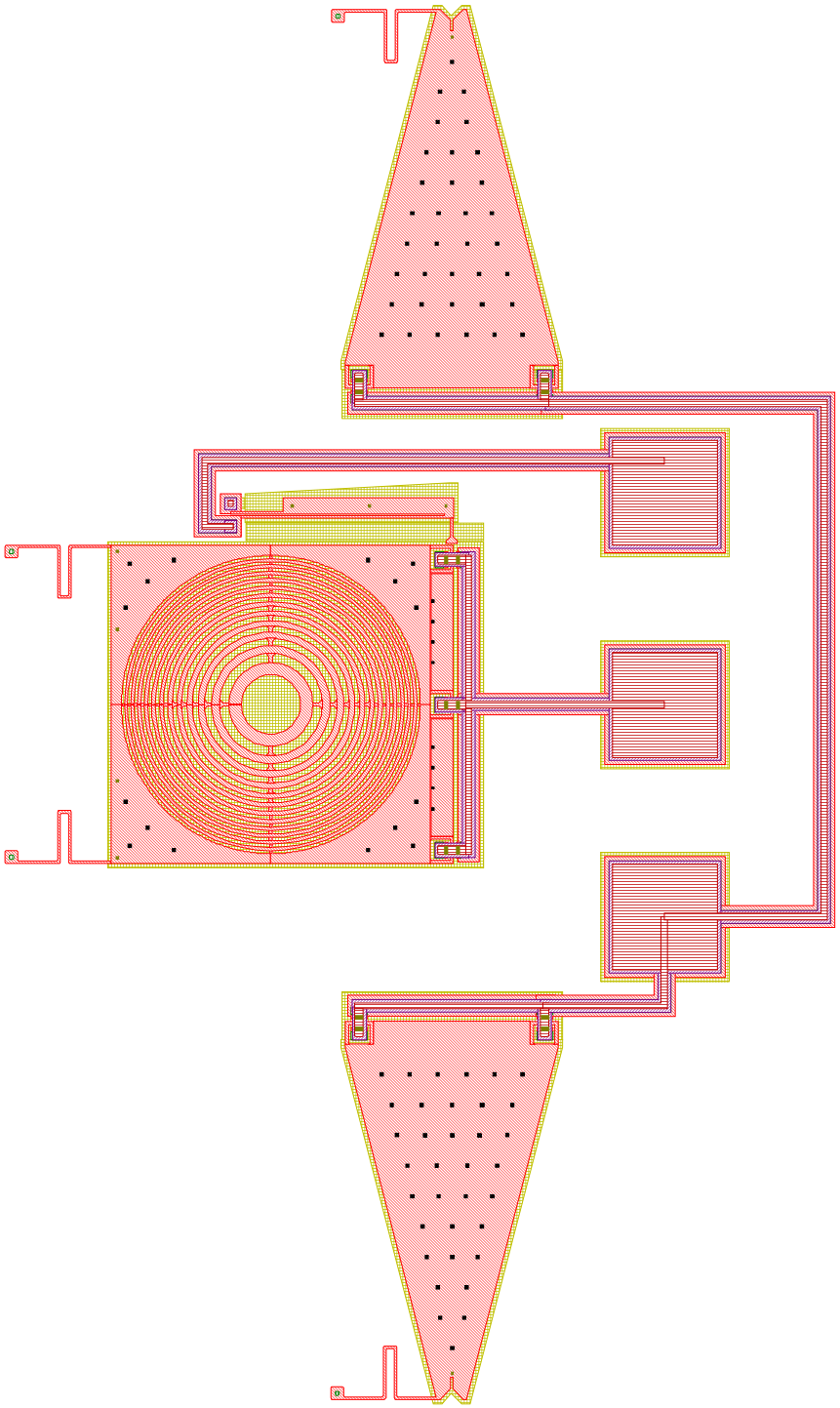

Figure 20: Layout for electrostatic self-assembling mirror.

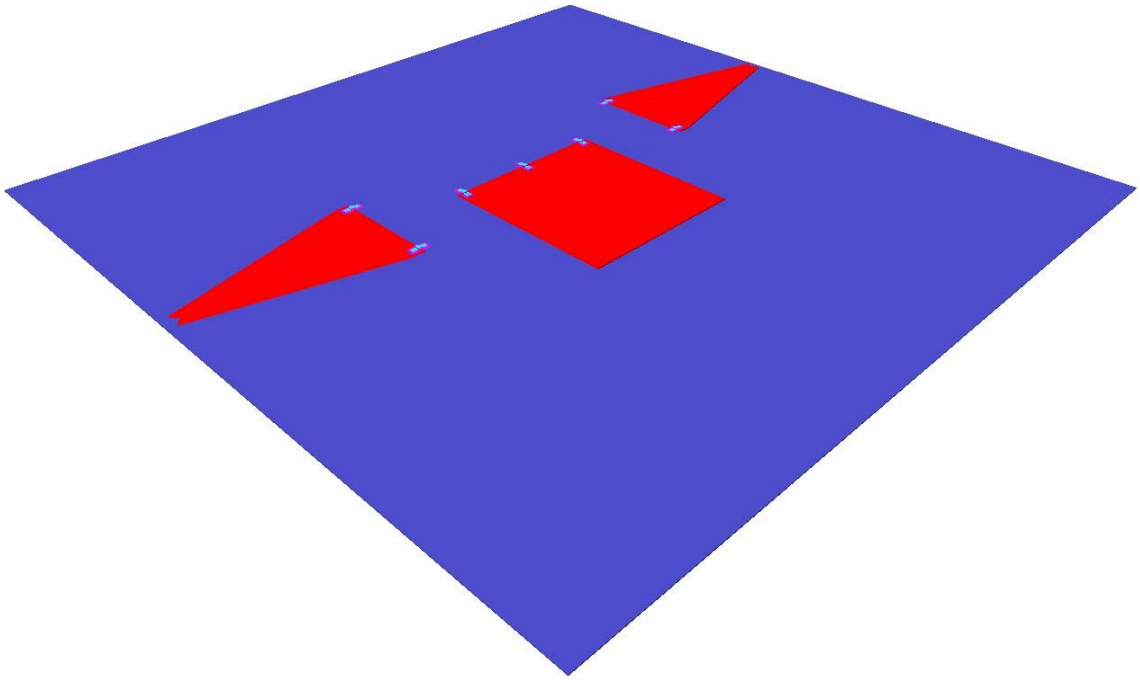

Figure 21: Mirror parts as returned from fabrication.

This process depends on a grounded plane close to the wafer surface. One way to provide the ground plane is to route an electrical connection to the edge of the chip. The chip can then be mounted in a standard ceramic package and bonded. Placing a conductor across the top of the package will provide the ground plane.

Apply the lift-off voltage, calculated using equation (12) or equation (14), to both the plate and the two vertical supports. As described above, all three components should lift-off and rotate to a position perpendicular to the wafer surface, as shown in Figure 22. Ground the two outside plates (vertical supports). The vertical supports are then no longer attracted to the grounded plane since they are at the same voltage. However, the vertical supports are now attracted to the mirror plate, and so should fall inward, connecting with the mirror plate, and completing the assembly. The vertical supports and

the mirror plate will short, so the voltage supplies need to be current limited. Figure 23 is a model of the assembled device.

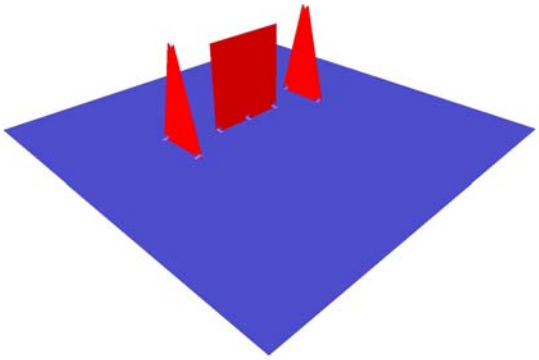

Figure 22: Mirror during fabrication; plates raised.

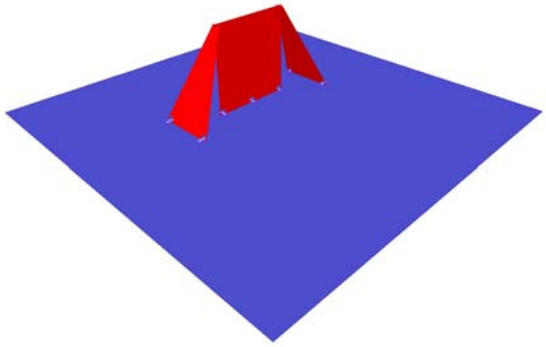

Figure 23: Final assembled mirror.

While the preceding discussion obviously applies to the components described in references [1] and [4], it can also be generalized to other types of components. For example, this method can be used to assemble boxes, with and without tops. The open boxes would certainly be useful for component placement.

3.3. Mechanical Theory of Self-Assembly

Numerical simulations, which are covered in the next chapter, showed that, if the voltage is kept constant, the electrostatic force on the plate increases between the lowered and raised positions. While dependent on geometry, the force increase is near 100%. Additionally, there may be forces due to mechanical shock when the mirror reaches its highest position and is stopped by the hinges' staples. Two designs for the plate and hinges will be considered, which are outlined in Figure 24 and Figure 25.

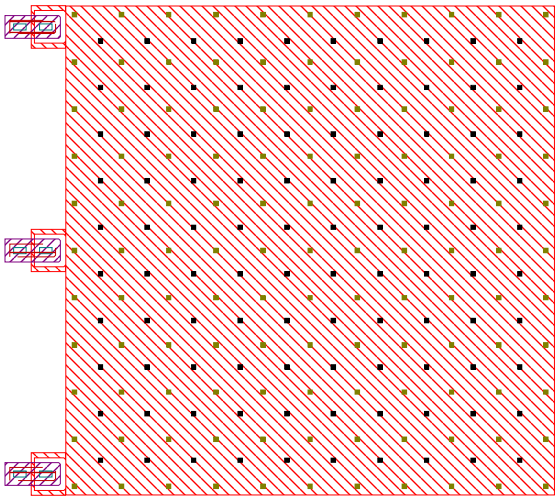

Figure 24: Mask layout for type A plate design.

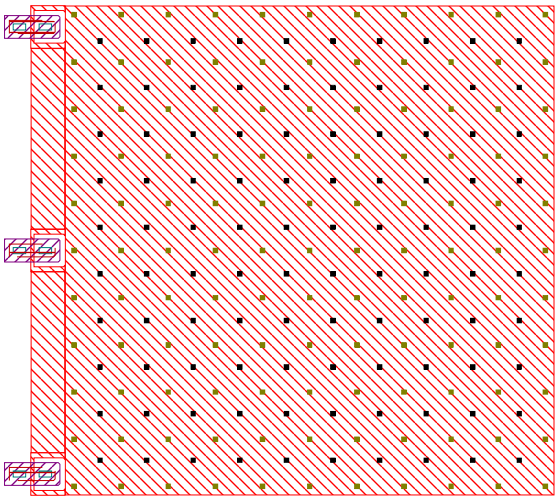

Figure 25: Mask layout for type B plate design.

In the raised position, the hinges must resist the electrostatic force, less the weight of the plate. The electrostatic force on the plate is 116% higher[30] when raised than while resting. Assuming that the voltage is set so that the electrostatic force exactly equals the plate's weight when resting, then the hinges must support 116% of the plate's weight when the plate is in the raised position.

$$F_g = 1.16gtA\rho \qquad (15a)$$

$$= (1.16)(9.81\ \text{m/s}^2)(2.0\ \mu\text{m})(300\ \mu\text{m})(300\ \mu\text{m})(2331\ \text{kg/m}^3) \qquad (15b)$$

$$\approx 4.77\ \text{nN} \qquad (15c)$$

Clearly, the required force is very small. Even when carried by six beams with a total cross-section area of 24 μm^2, the average stress is only 199 Pa. This is extremely small; the yield strength of poly-silicon is 1-2 GPa. Thus there is a safety factor of approximately seven orders of magnitude.

[30] This value was not obtained using analytical methods. It was determined using numerical simulations, which will be discussed in the next chapter.

Significant stress concentration will occur at the corners of the hinges. The stress concentration factor can be determined from the corner's radius of curvature and beam's thickness [9]. At worse, the hinge's beams will have to comply with the minimum width layout rule, so the beam thickness will be at least 2μm. For the MUMPs process, masks have a resolution of 0.1 μm. Assuming a radius on this order, then (R/t) is 0.05 and the stress concentration factor is approximately 20. The maximum stress is thus 3.98 kPa, which is still well below the yield strength.

3.4. CONCLUSION

With an external ground plane, it is fairly easy to rotate surface micromachined parts off the wafer. Further, while the plates can be actuated independently, they can also be actuated in parallel. These attributes make for an assembly process with considerable speed and flexibility.

Mechanical analysis shows that this process puts very little mechanical stress on the components. Thus this process may be better suited for sensitive or fragile devices than other self-assembly processes.

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CHAPTER 4
SIMULATIONS

While analytical results are certainly useful, they often contain many simplifying assumptions used to make the mathematics tractable. Although obtaining good results can be difficult, numerical simulations can provide greater accuracy because fewer assumptions are needed. Just as important however, they can be used to provide a check on the analytical results.

Of the four simulations discussed in this chapter, only one has not been discussed analytically. Because of the problem's difficulty, this paper presents no analytical electrostatic results for plates when raised. For this model, the numerical results must stand alone.

All of the numerical simulations were performed with the "ANSYS" software package[31]. The source code used for the simulations is available in the appendices.

4.1. ADVANCED SIMULATION TECHNIQUES

4.1.1. Maxwell Surface Flags

In electrostatic analysis, the forces created by electrostatic pressure do not affect the solution. ANSYS therefore does not calculate the forces due to electrostatic pressure unless specifically requested. During application of boundary conditions, the model can specify a number of surfaces[32] as Maxwell surfaces [1]. Unlike other boundary conditions, Maxwell surfaces are not really loads. Instead, they indicate the surfaces on which the forces due to electrostatic pressure are to be calculated.

In particular, Maxwell surface flags were used in the electrostatic self-assembly simulations. In these simulations, Maxwell flags were set on the edges of the polysilicon

[31] ANSYS, Inc., 275 Technology Drive, Canonsburg, Pennsylvania, 15317, USA.
[32] In 2D analysis, surfaces are actually lines.

plate. The calculated forces were summed to determine the total electric force on the polysilicon plate.

4.1.2. Sub-modeling

Before describing the individual models used for simulation, the technique of sub-modeling needs an introduction. Sub-modeling is used to more accurately model a small portion of a larger model [2]. Sub-modeling is also known as the cut-boundary displacement method or the specified boundary displacement method.

When modeling a system, a sub-region may be of particular interest. In this region, the mesh may not be fine enough[33] to provide enough detail for accurate results. To obtain greater detail, the mesh needs to be refined. Unfortunately, a large range of element sizes within the same mesh leads to poor meshes and hence poor accuracy. The easiest solution is to refine the mesh for the entire model. Unfortunately, this approach has a single important disadvantage, and so sub-modeling is often used.

The disadvantage with refining the mesh of the larger model is that it greatly increases the number of nodes in the model. As the number of nodes is related to processing time, the refined model may no longer be computationally feasible. In other cases[34], the licensing may specify an upper bound on the number of nodes allowed in each model. Simply refining the mesh may not be possible if a hard limit on the node count exists.

Instead of refining the mesh for the entire model, which can be computationally difficult, a new, independent model is created for the region of interest. The new model is known as the sub-model. The sub-model contains the geometry from only a portion of the coarse model. Since the geometry is smaller, the sub-model can then be more finely meshed.

[33] The element size is too large.
[34] This is the case at Simon Fraser University. The current license allows approximately 100 000 nodes.

In the sub-model, the cut-boundary is the boundary of the sub-model that represents a cut through the coarse model. The boundary conditions for nodes along the cut boundary are calculated from the results generated by the coarse model. As the mesh will be finer, the boundary conditions for most of the nodes along the cut boundary will be generated by interpolation [2].

4.2. ELECTROSTATIC SIMULATIONS FOR SELF-ASSEMBLY

To confirm the analytical results presented in the last chapter, a specific geometry was chosen and modelled using ANSYS. The specific geometry was a 300 μm by 300 μm plate with 20 μm hinges. The ground plane was suspended at a height of 500 μm.

For the electrostatic simulation, the PLANE121 element was used. PLANE121 is a two-dimensional 8-noded electrostatic modelling element [3]. There are a number of facts that determined this choice. First, the simulation's only degree of freedom is voltage. Second, only a 2D slice through the axis of symmetry of the raised plate will be modelled. Third, since there are no curved edges a low-order element should be used. However, ANSYS does not provide a 2D low-order element for electrostatic analysis, so the high-order element must be used.

While a full 3D simulation is certainly possible, Simon Fraser University's license limits the number of nodes available to each model. Achieving a good mesh on the 2D model approaches the limit of 100 000 nodes because of the extremes in dimensions. Film thickness, which ranged from 0.6 to 2.0 μm, is very small when compared with the lateral dimension and the height of the ground plane.

A careful reading of the ANSYS listings, which are available in the appendices, will also show that the INFIN110 element is also defined, but not used. The INFIN110 is a two dimensional infinite solid [3], and is used to model infinite boundaries. Ideally, INFIN110 elements should be used along all of the edges of the model except the top,

which is the ground plane. The voltage at infinity could then be set to zero, which would improve the accuracy of the model. Modifying the ANSYS model to incorporate this is for future work. Presently, no boundary conditions are applied along the three edges.

Following the element definitions, the material properties used in the model are defined. For an electrostatic model without conduction, the only material property needed is the relative permittivity. The model contains three materials, air, silicon nitride, and polysilicon. Table 3 shows the values used in the model.

Material	Relative Permittivity [4]
Air	1.0
Poly-Silicon	11.7
Silicon Nitride	7.5

Table 3: Relative permittivities used in electrostatic ANSYS simulations.

The remaining steps, which won't be detailed, are to create the geometry, create the mesh, apply boundary conditions, and then solve the model. Once solved, ANSYS will know the voltage at every node. From these data, ANSYS can quickly determine not only voltage distributions, but also the electric fields throughout the model.

The first model constructed was for the plate laying flat. This model makes use of both Maxwell surfaces and sub-modeling. The numerically determined electric fields affecting the plate are shown in Figure 26. ANSYS determined that the electric pressure applied a force of $F_y = 6.4908 \times 10^{-7}\ V^2$, which corresponds to a lift-off voltage of ~46 volts. This compares quite well to the value of ~51 volts, which was obtained by using equation (12).

Fortunately, the analytical results will generally be conservative. Since the ground plane will be significantly larger than the structure to be raised, the electric fields will tend to concentrate over the structure. The resulting electric fields will therefore be larger than predicted by the parallel plate approximation used to derive the analytical results.

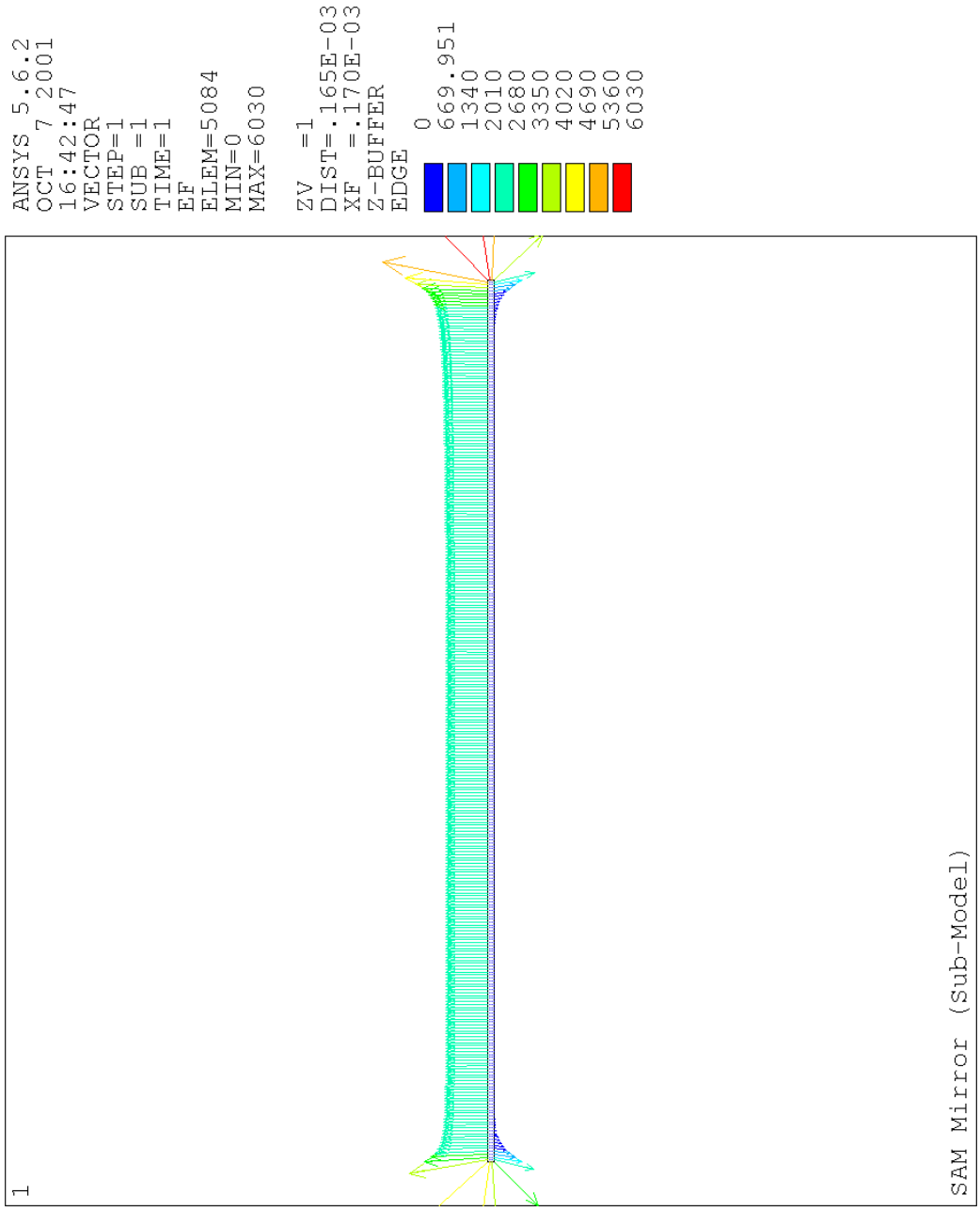

Figure 26: Electric field affecting the polysilicon plate while resting.

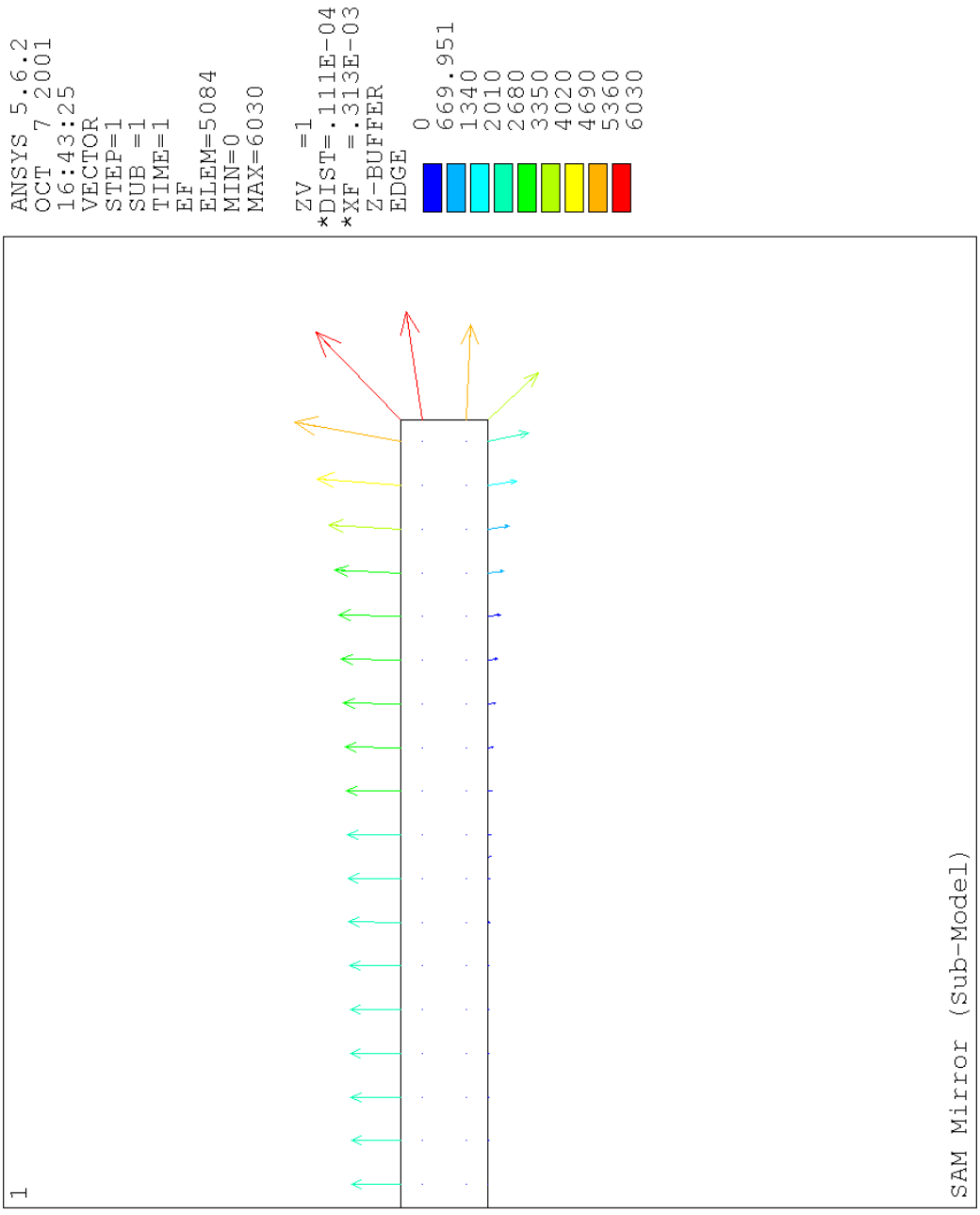

Figure 27: Close-up of fringe fields affecting the polysilicon plate while resting.

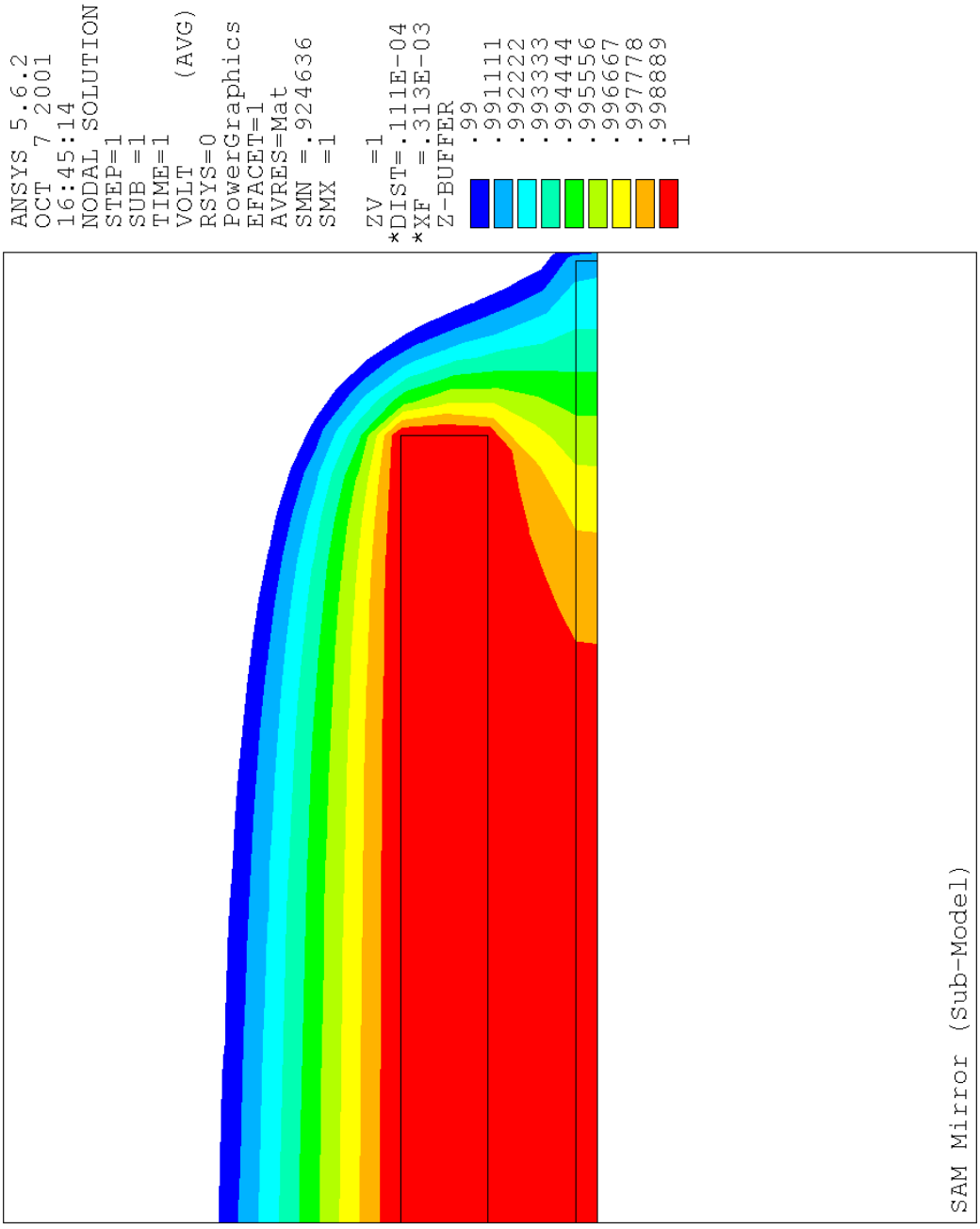

Figure 28: Fine scale voltage distribution near edge of polysilicon plate while resting.

The plate modeled is designed to be symmetric when raised. The plate thus rests to one side of the ground plane. This asymmetry leads to a difference in the fringe fields at the edges of the plate, and hence to a horizontal force. This force, which was not considered in the analytical results, is present in the ANSYS simulation. This force is significantly smaller[35] than the vertical force experienced.

To ensure that the plate would completely rise, a second model was created. In the second model, the plate was modeled in the upright position. The vertical force on the mirror in this position is $F_y = 1.3980\text{x}10^{-7}\ V^2$ (F_y measured in Newtons when V is measured in volts). Compared to the force experienced by the plate in the resting position, this force is more than double. Assuming a smooth change in the vertical force on the mirror while it is being raised, this represents a stable equilibrium point.

Figure 29 shows the electric fields affecting the plate while raised. They are not exactly symmetric horizontally, which is contrary to expectations. While the model is geometrically symmetric, the automatically created mesh is not. Refining the mesh would solve the problem, but unfortunately this model is already at the node limit for the available version of ANSYS. Although it wasn't pursued, a more elegant solution would be to use the symmetry when creating the model.

Unfortunately, sub-modeling is not applicable. Since the results of the coarse model are applied to the cut-boundary, the errors found in the coarse model would be applied to the sub-model. Sub-modeling was not used for this analysis.

[35] $F_x = 1.1164\text{x}10^{-8}\ V^2$.

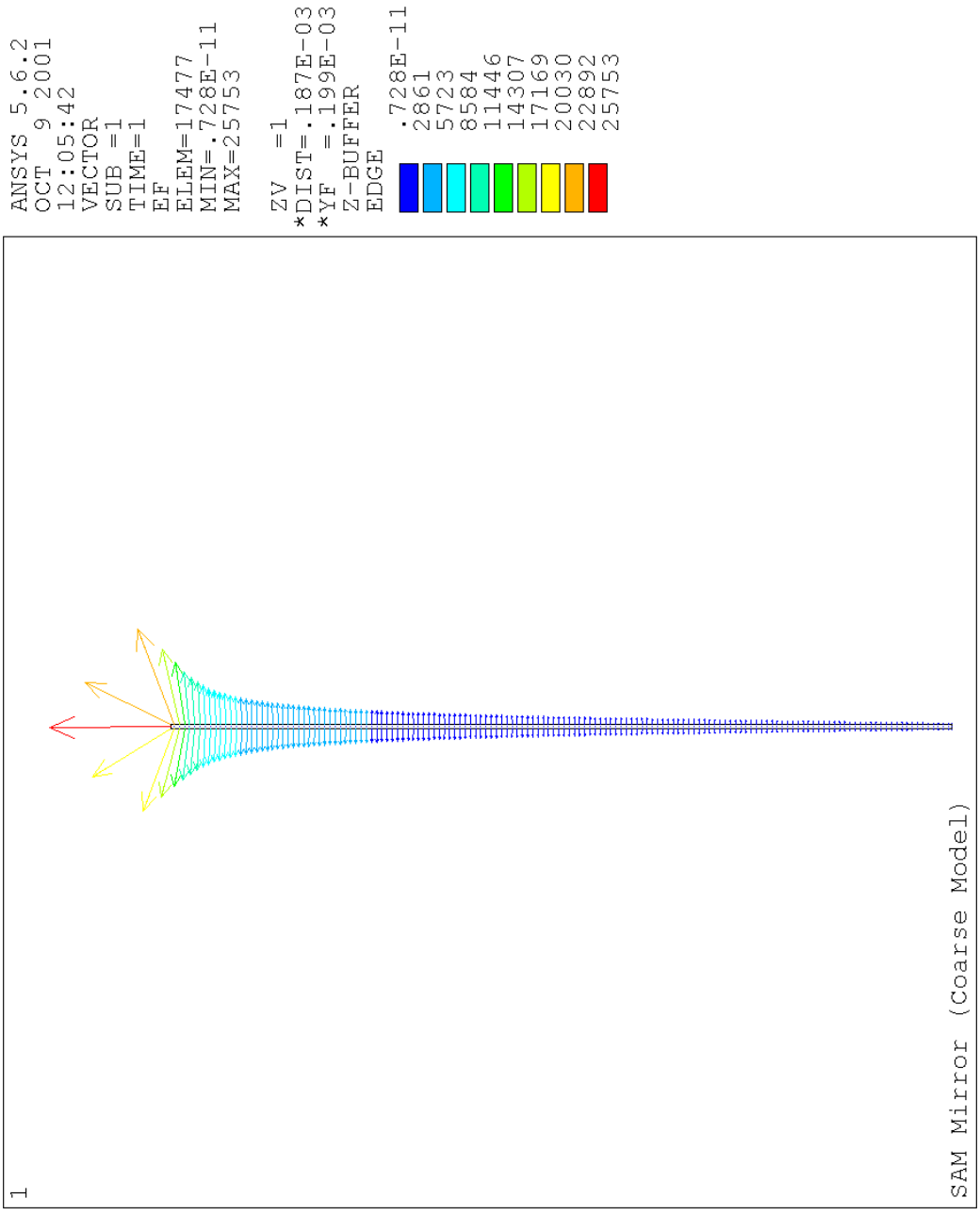

Figure 29: Electric fields affecting polysilicon plate while raised.

4.3. MECHANICAL SIMULATIONS FOR SELF-ASSEMBLY

ANSYS was used to simulate the loading on both type A and type B plates.

Geometrically, the hinges are modeled as perfect corners, which have stress concentration factors of infinity. However, ANSYS does not derive results directly from the geometric model, but from the generated mesh. The finite element length of the mesh restricts the stress concentration. However, the maximum stress calculated by ANSYS will increase with decreasing mesh size. The calculated maximum stress would only be valid if the geometric model included filets at the corners. This would also require a mesh with element lengths significantly smaller that the corner radius.

For the mechanical simulations, the PLANE42 element, which is a low-order 2D structural element [3], was used. With this element, each node supports two degree of freedom: displacement in the *x* and *y* directions. The PLANE42 element has an option to specify a thickness for the structure. The model is thus, while geometrically 2D, fully specified in all three dimensions.

Three material properties are needed for the mechanical analysis: modulus of elasticity, Poisson's ratio, and density.

The modulus of elasticity for silicon varies, depending on the microstructure, between 150 GPa to 175 GPa [5]. For bulk silicon, the modulus of elasticity is 169 GPa [6]. This value agrees with measurements performed on polysilicon deposited in the MUMPs process [7] [8]. Run-to-run variation in the modulus of elasticity in the MUMPs process is approximately 4%.

Poisson's ratio for bulk silicon is 0.26 [6]. However, a more commonly quoted value for silicon thin films is 0.22 [7] [8].

The density of silicon is 2331 kg m^{-1} [4].

Sub-modeling was used to refine stress calculations in the hinges. The successive models are outlined in Figure 30, Figure 31, and Figure 32. Figure 32 is of interest as it shows a large stress concentration at the point where the hinge is first supported by the staple. It appears that this point is, in fact, where the largest stress concentration occurs. This new stress concentration point is of the same order though as the corner, and so should not present a structural fault considering the large safety factor.

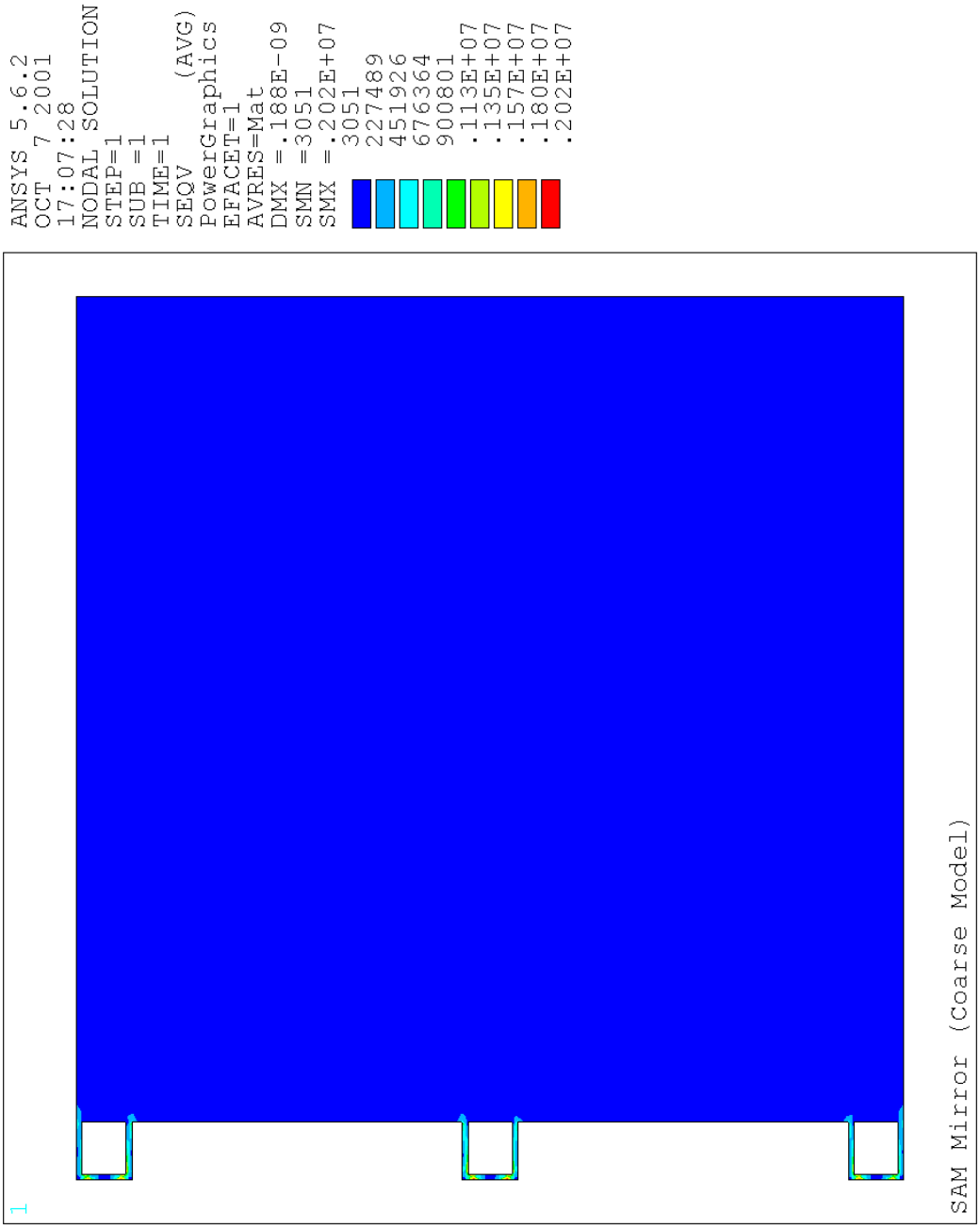

Figure 30: Plot of von Mises stress in type-a plate when loaded by 10 μN.

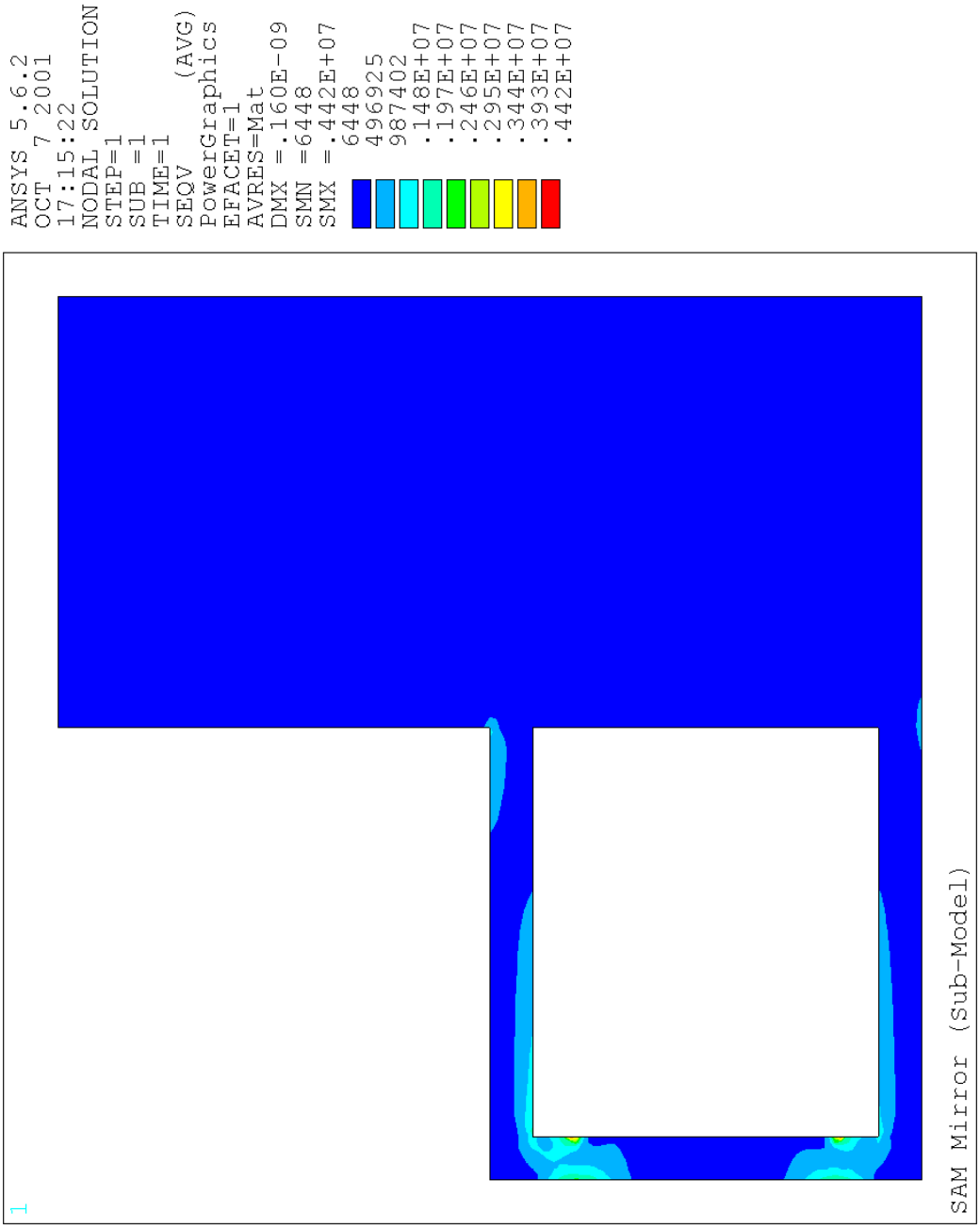

Figure 31: Close up of von Mises stress in type-a plate when loaded by 10 μN.

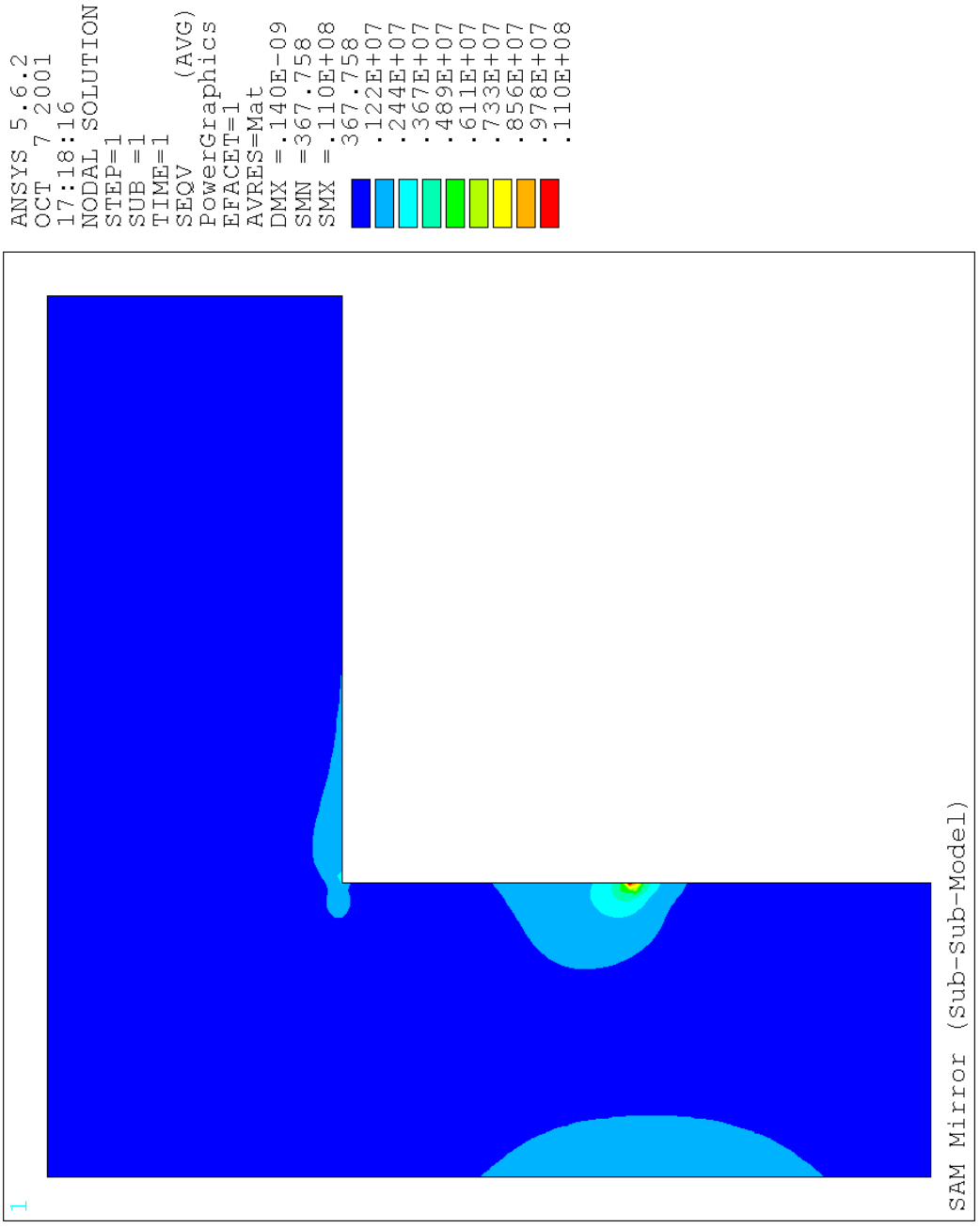

Figure 32: Close up of von Mises stress in type-a plate when loaded by 10 μN.

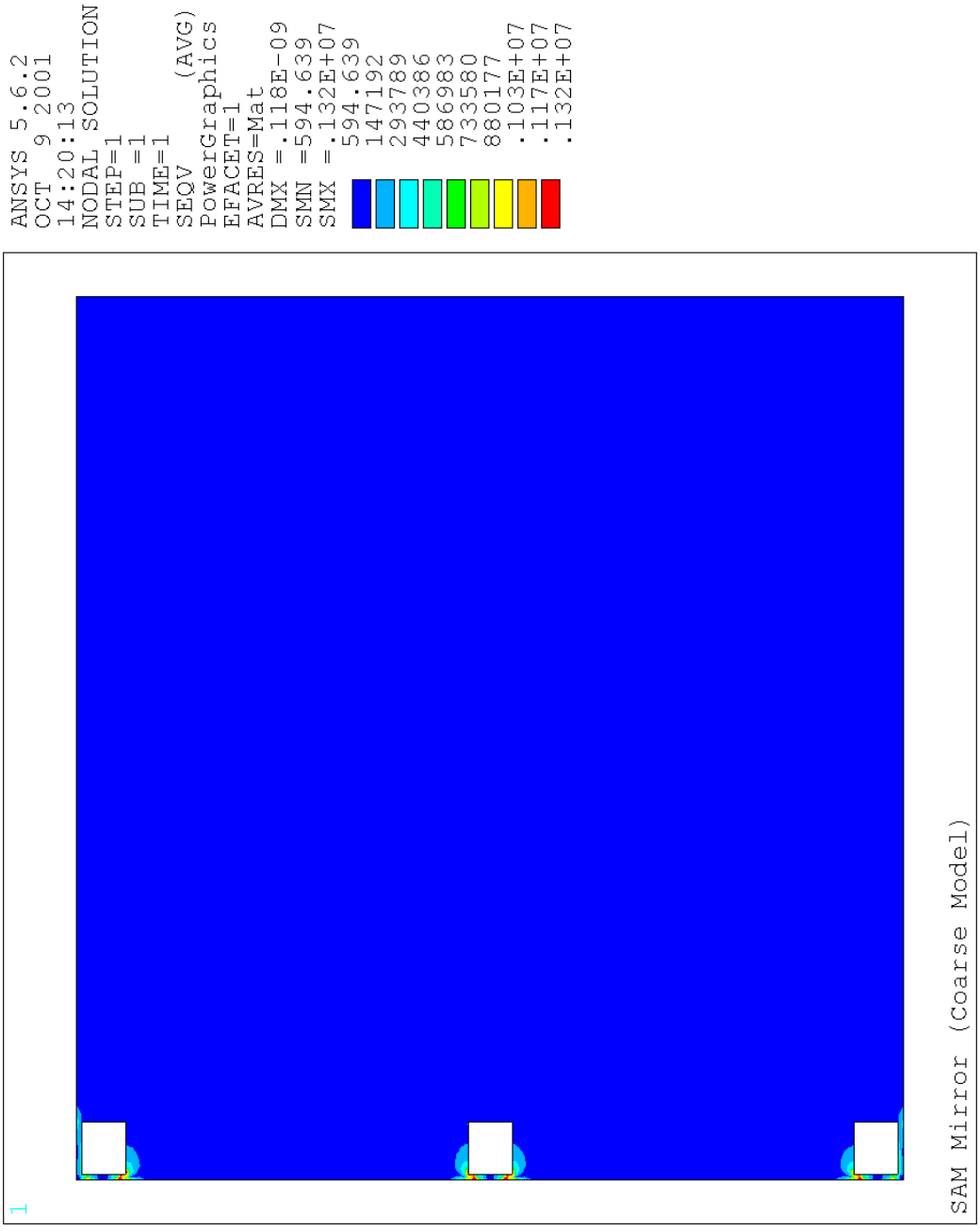

Figure 33: Plot of von Mises stress in type-b plate when loaded by 10 μN.

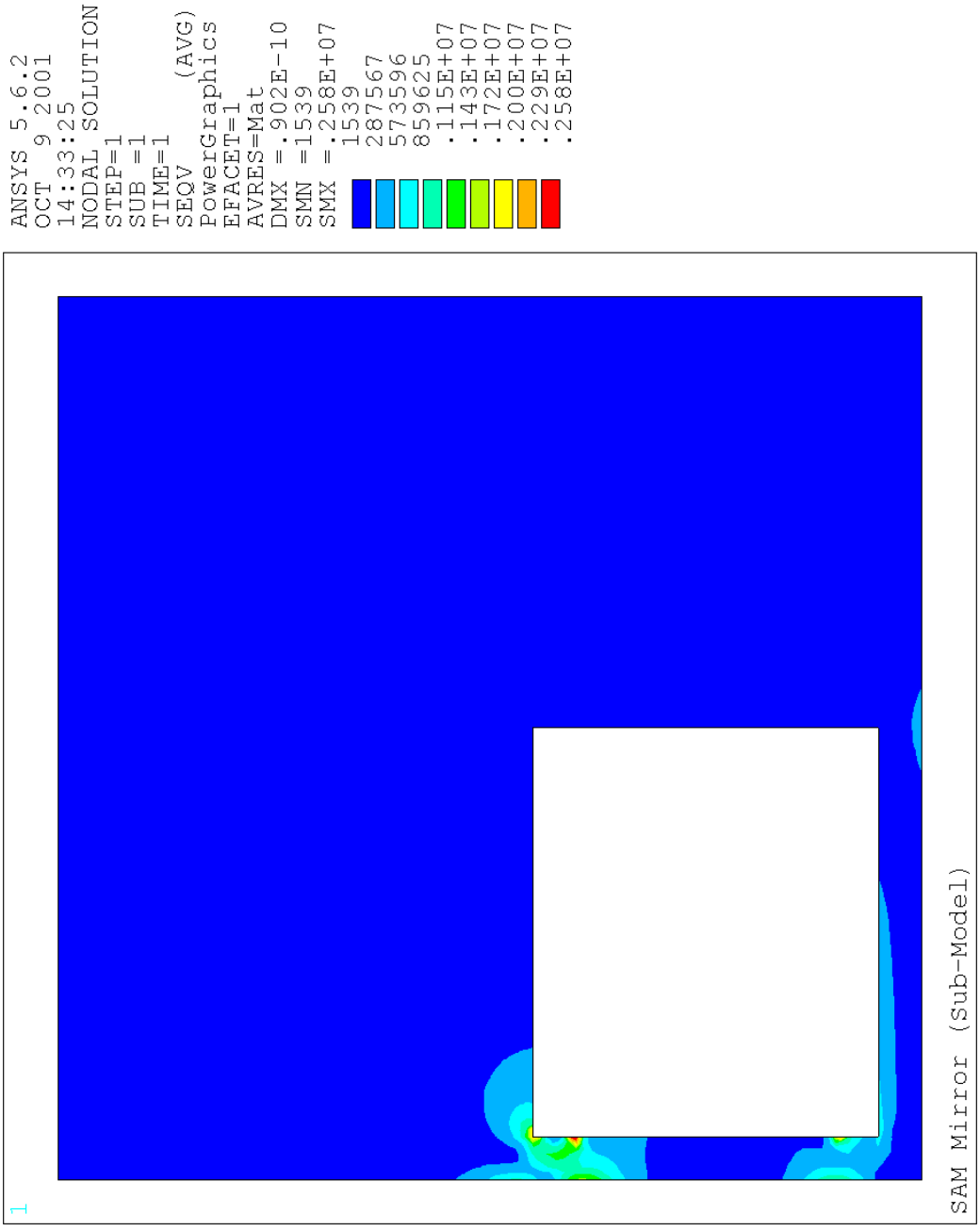

Figure 34: Close up of von Mises stress in type-b plate when loaded by 10 μN.

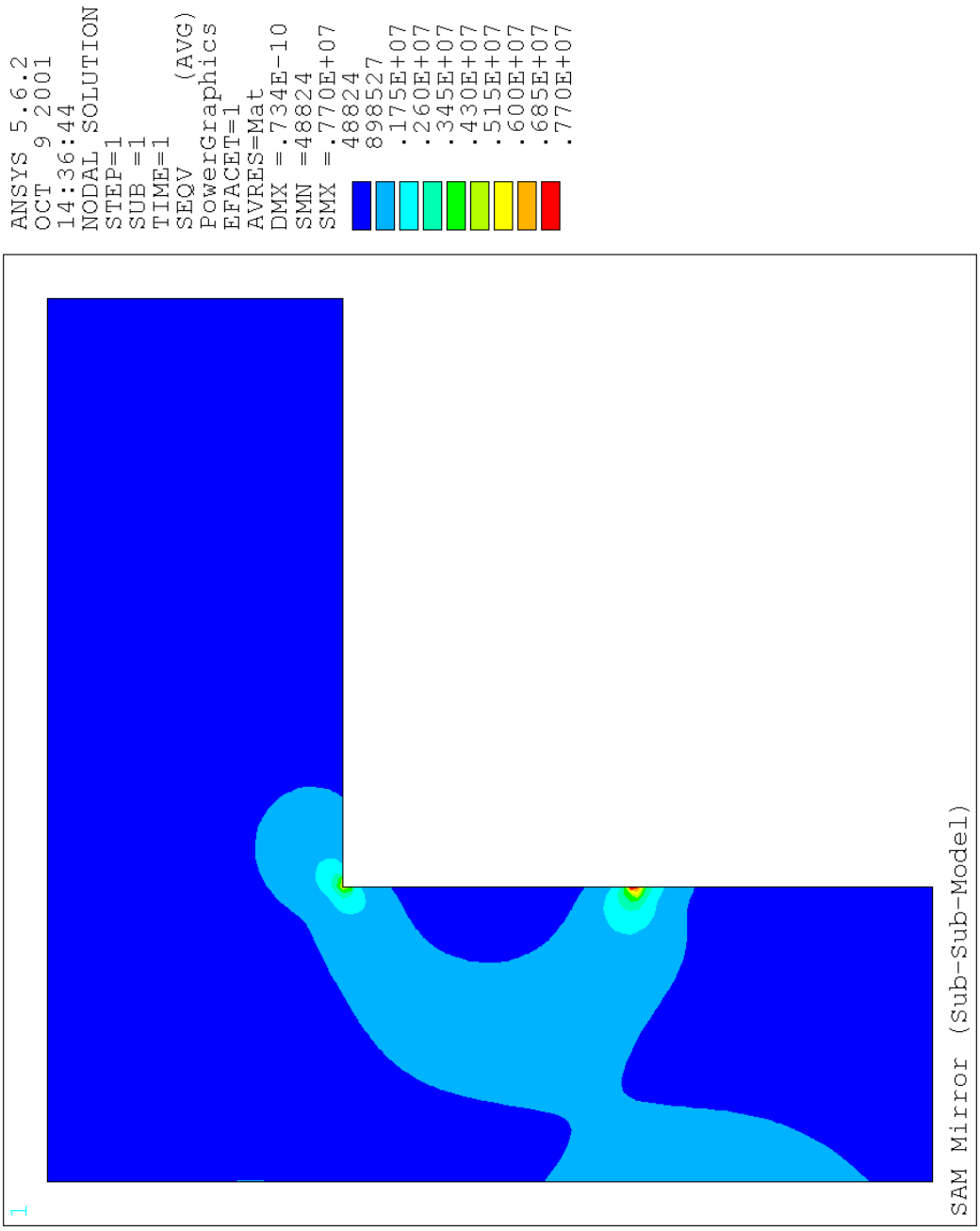

Figure 35: Close up of von Mises stress in type-b plate when loaded by 10 μN.

4.4. REFERENCES

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CHAPTER 5
OPTICAL THEORY OF MICRO-OPTIC STRUCTURES

5.1. INTRODUCTION

Despite significant academic interest in miniaturized optical systems [1] [2] [3] [4] [5], micromachined optical systems have seen little use outside of labs. This is obviously due to commercially unacceptable performance. The difficulties can, in large part, be traced to the alignment of the optical components. Because of the current limitations of micromachining technologies, tolerances on component placement will be a significant fraction of a system's overall dimensions. Alignment tolerances can therefore destroy system performance.

This indicates that further research into controlling manufacturing tolerances, or their effect on system performance, is required. Important to this effort are methods for analyzing the effects of manufacturing tolerances on optical performance. To this end, we have extended the method of ray-transfer matrices.

For paraxial optics, ray-transfer matrices can completely characterize a system in a compact form [6]. Designers can easily assemble the system matrix, which can be used to predict the output ray for any input. The system matrix can also be used to model Gaussian beams[36].

Unfortunately, ray-transfer matrices assume that all components are perfectly aligned to the optical axis. This is a critical shortcoming when trying to model the effects of manufacturing tolerances. This chapter will present a simple extension to standard ray-transfer matrices. The extension allows designers to account for and track the effects of component misplacement.

[36] In a Gaussian beam, the light intensity has circular symmetry. Further, the intensity decreases with distance from the beam's axis with a Gaussian form: $I = \exp(-r^2 / 2w^2)$ [6].

This chapter will also show how to use the extended ray-transfer matrices to calculate the coupling efficiency in a simple optical switch.

5.2. EXTENDED RAY-TRANSFER MATRICES

In paraxial ray tracing, an optical ray is represented by the ray's distance from the optical axis, y, and its slope or angle with respect to the optical axis, α, [6]. Each component in the optical system transforms these parameters. In paraxial optics, these transformations are linear and so can be represented by matrices.

A complex optical system can be represented by multiplying the matrices together to obtain the system matrix. The system matrix, in addition to locating all of the system's cardinal points [6], can be used to calculate the position and orientation of the output ray from an input ray.

$$\vec{r}_o = \overline{S}\vec{r}_i \tag{16a}$$

$$\begin{bmatrix} y_o \\ \alpha_o \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} y_i \\ \alpha_i \end{bmatrix} \tag{16b}$$

While this method certainly simplifies ray tracing, it does have an important limitation. It cannot represent translation since translation is not a linear transformation; it is an affine transformation. Translations play an important role in accounting for manufacturing tolerances. The solution is to use a homogeneous coordinate system [7][37]. In essence, the coordinate system is extended to the third dimension, which we will represent by w. In all vectors, the value of w should be one. The extended ray-transfer matrices will then have the form outlined in equation (17).

[37] Homogeneous coordinate systems are extremely important to computer graphics. This is just one amongst many books that will cover this topic.

$$\begin{bmatrix} y_o \\ \alpha_o \\ 1 \end{bmatrix} = \begin{bmatrix} A & B & d \\ C & D & \theta \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} y_i \\ \alpha_i \\ 1 \end{bmatrix} \qquad (17)$$

Using extended ray-transfer matrices, despite increasing the matrix size from 2x2 to 3x3, really only introduces two new variables, d and θ. The naming of these variables will be clarified later in this chapter. The elements A, B, C, and D are the elements found in the traditional system matrix and can be used in much the same way. If the standard ray-transfer matrix for an optical component is known, it can be easily extended by substituting the standard values for A, B, C, and D into equation (17) and setting d and θ to zero.

The extended ray-transfer matrices for components used in the example that will follow are shown in Table 4. Please refer to [6] for a complete list.

Optical Component	Matrix	Description
Mirror[38]	$\overline{M} = \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	Mirrors aligned at 45° to the optical axis will invert the ray's height and angle.
Spacing	$\overline{L}_l = \begin{bmatrix} 1 & l & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	In the space between components, the ray's height will change depending on its angle.
Thin-lens	$\overline{F}_f = \begin{bmatrix} 1 & 0 & 0 \\ -1/f & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	A thin-lens will change the angle of a ray. Collimating lenses have a positive focal length; dispersive lenses have a negative focal length.

[38] Not a general component.

Translation	$\overline{T}_{y,\alpha} = \begin{bmatrix} 1 & 0 & y \\ 0 & 1 & \alpha \\ 0 & 0 & 1 \end{bmatrix}$	The ray is offset by the values of y and α.

Table 4: Summary of ray-transfer matrices.

The component matrices outlined in Table 4 are suited for cylindrically symmetric optical systems. Even if the system is not cylindrical, the two axes perpendicular to the optical axis can usually be treated independently. Each axis thus has its own system matrix. One matrix handles the transformation of (y, α); the second matrix handles the transformation of (x, β).

When considering a single transverse axis, components have three degrees of freedom in misalignment, y, z, and α. Misalignment along the optical axis, z, is easily modeled by modifying any spacing matrices. However, misalignment in the other two parameters should be handled by modifying the component's ray-transfer matrix. The definition of y and α is shown in Figure 36. Equation (18) works by translating the incoming ray, which is measured against the system's optical axis, onto the components displaced optical axis. The outgoing ray is translated back onto the system's optical axis.

$$\overline{C'} = \overline{T}_{y,\alpha}\,\overline{C}\,\overline{T}_{-y,-\alpha} \qquad (18)$$

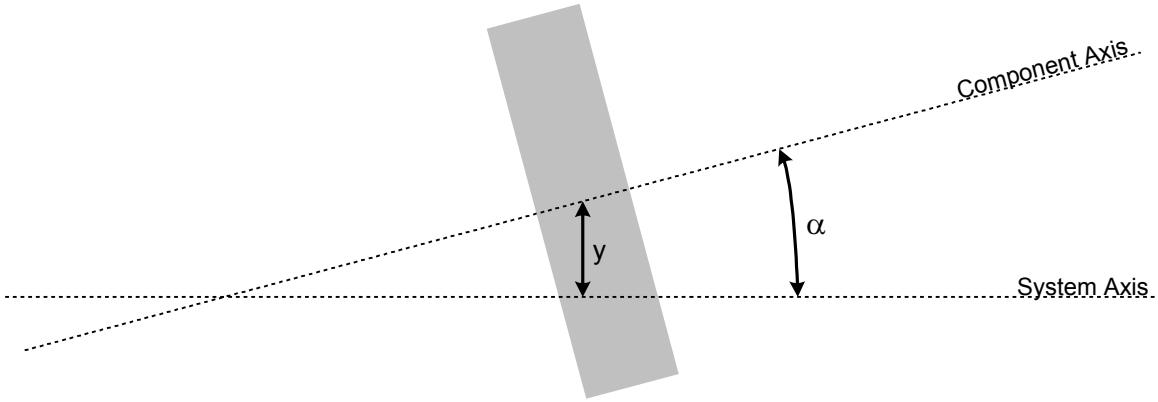

Figure 36: Misalignment measurements.

5.3. SYSTEM MATRIX FOR OPTICAL SWITCH

In introducing extended ray-transfer matrices, the natural coordinate system was *x*, *y*, and *z*, where *x* and *y* were transverse directions, and *z* was parallel to the optic axis. However, that coordinate system is less useful when discussing an actual device. In this section, the coordinate system will match the on-chip physical implementation, with *z* being perpendicular to the wafer surface.

A major concern for micro-machined optical systems is non-uniform residual stresses and the bowing that they induce. Any curvature of the optical components, in particular the mirror, will lead to additional losses. While not included here, the forms for component matrices handling curved surfaces are known and can be found in [6].

The common layout for fibre-optic switches based on free-space micro-optical-bench technology is an NxN grid [8]. As outlined in Figure 37, the light path in all cases contains three components, two lenses and a mirror. The matrices for these components are listed in Table 5. We will develop the system matrix for a single light path.

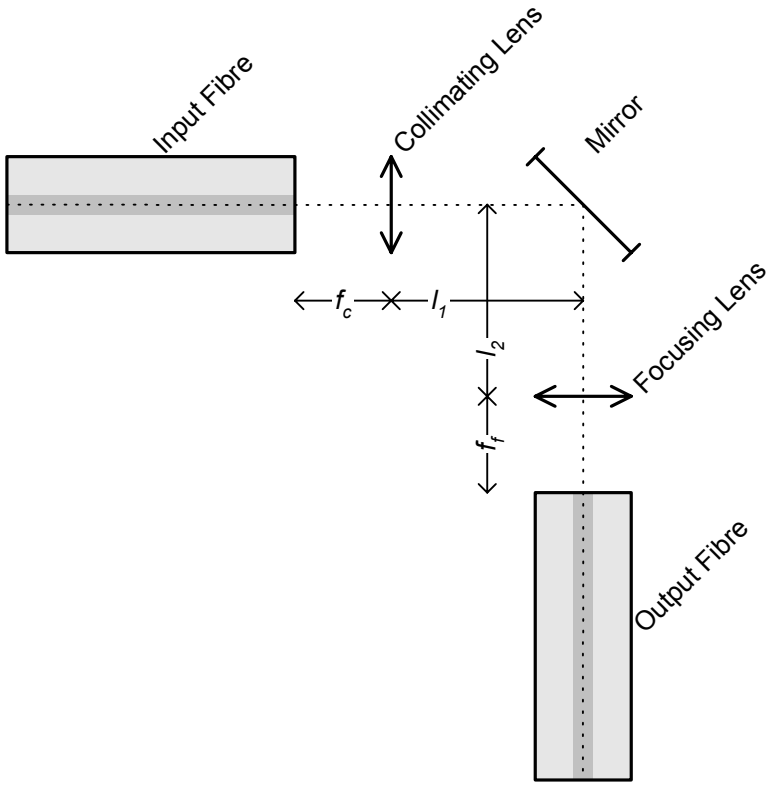

Figure 37: Schematic of one optical path in a simple optical switch.

Component	Equation	Matrix
Collimating lens	$\overline{T}_{y_c,\alpha_c}\overline{F}_{f_c}\overline{T}_{-y_c,-\alpha_c}$	$\overline{C}_c = \begin{bmatrix} 1 & 0 & 0 \\ -1/f_c & 1 & y_c/f_c \\ 0 & 0 & 1 \end{bmatrix}$
Mirror	$\overline{T}_{x_m,\alpha_m}\overline{M}\overline{T}_{-y_m,-\alpha_m}$	$\overline{C}_m = \begin{bmatrix} -1 & 0 & x_m + y_m \\ 0 & -1 & 2\alpha_m \\ 0 & 0 & 1 \end{bmatrix}$
Focusing lens	$\overline{T}_{x_f,\alpha_f}\overline{F}_{f_f}\overline{T}_{-x_f,-\alpha_f}$	$\overline{C}_f = \begin{bmatrix} 1 & 0 & 0 \\ -1/f_f & 1 & x_f/f_f \\ 0 & 0 & 1 \end{bmatrix}$

Table 5: Ray-transfer matrices for component of optical switch.

The complete optical system can be derived by adding in the effects of optical misalignment for the input and output fibre and the spacing between components. The translation matrices at the beginning and end of equation (19) connect the system's optical axis to the output fibre and input fibre's axes respectively. The matrix multiplication should be read from left to right.

$$\overline{S} = \overline{T}_{-x_o,-\alpha_o}\,\overline{L}_{f_f+y_f-y_o}\,\overline{C}_f\,\overline{L}_{l_2+y_m-y_f}\,\overline{C}_m\,\overline{L}_{l_1+x_c-x_m}\,\overline{C}_c\,\overline{L}_{f_f+x_i-x_c}\,\overline{T}_{y_i,\alpha_i} \tag{19}$$

The complete expression for $\overline{S}$ will not be reproduced here, as it is quite large. Smaller terms are dropped to simplify the matrix. The matrix has also been simplified by assuming that f_c and f_f are equal[39]. This results in equations (20) through (26).

$$\overline{S} = \begin{bmatrix} A & B & d \\ C & D & \theta \\ 0 & 0 & 1 \end{bmatrix} \tag{20}$$

$$A = 1 \tag{21}$$

$$B = -x_i + x_c + y_f - y_o \tag{22}$$

$$C = \frac{2}{f} - \frac{l_1 + l_2 - x_c + x_m + y_m - y_f}{f^2} \tag{23}$$

$$D = 1 \tag{24}$$

$$d = y_i - y_c + x_f - x_o + 2\alpha_m f \tag{25}$$

[39] This is not a general case; many designs will have f_c and f_f unequal.

$$\theta = \alpha_i + 2\alpha_m - \alpha_o + (l_1 + l_2)\frac{-y_i + y_c + y_c}{f^2} + \frac{2y_i - y_c + y_m + x_m + x_f}{f} \qquad (26)$$

As before, it should be noted that the system matrix only handles one dimension. For a circular beam in a traditional optic system, this may be sufficient. However, the input beam may be astigmatic, but, more importantly, most micro-optical systems will not treat both axes similarly.

Equation (19) represents the system matrix for the plane that is parallel the wafer surface. A similar equation can be derived for the plane perpendicular to the wafer surface. This results in a second system matrix, $\overline{S}'$. The insertion losses, considered next, can easily include the effects due to the second system matrix.

5.4. INSERTION LOSSES

To calculate the insertion loss, we need to extract four parameters from $\overline{S}$. These parameters are the beam size, beam curvature, beam offset, and beam tilt. Fortunately, all of these parameters can be easily extracted from the system matrix.

5.4.1. Beam Width and Curvature

At a particular point, the direction, width, and curvature completely characterize a Gaussian beam. Since the beam direction does not change without outside influence, focus typically lies on the width and curvature. These two parameters can be combined into the complex radius of curvature [6], which can be calculated using equation (27).

$$\frac{1}{\tilde{q}_o} = \frac{1}{R} + \frac{i\lambda}{\pi w^2} \qquad (27)$$

In equation (27), $\tilde{q}$ is the complex radius of curvature, R is the radius of curvature, λ is the wavelength, and w is the transverse width. The electric field strength drops by a factor of e at a distance of w from the beam's centre. For reference, the

equations used to recover the beam parameters from the complex radius of curvature are given below.

$$R = \frac{1}{\mathrm{Re}\left\{\tilde{q}^{-1}\right\}} \tag{28}$$

$$w = \sqrt{\frac{\lambda}{\pi \,\mathrm{Im}\left\{\tilde{q}^{-1}\right\}}} \tag{29}$$

Using the complex radius of curvature to characterize the input beam allows us to use the misnamed General Law of Laser Propagation [6]. The complex radius of curvature can be determined at the output of an optical system using the system matrix.

$$\tilde{q}_o = \frac{A\tilde{q}_i + B}{C\tilde{q}_i + D} \tag{30}$$

In equation (30), $\tilde{q}_i$ and $\tilde{q}_o$ are the curvature radii of the input and output beams respectively, and A, B, C, and D are elements from the system matrix. These are the elements from the traditional order-2 system matrix. Equation (30) implies that the ideal values for the traditional elements for A, B, C, and D are 1, 0, 0, and 1[40].

Together, equations (27) and (30) can be used to determine the beam width and beam curvature at the output of an optical system.

In part, the coupling efficiency is dependent on how well the output beam's parameters, $\tilde{q}_o$, match the output fibre's beam parameters, $\tilde{q}$. The transmission coefficient can be expressed as follows [10]:

[40] These are the ideal values if the input and output fibres are identical; identical fibres will have equal beam width's at the fibre end.

$$t_q = \frac{2}{\sqrt{\left(\frac{w_o}{w} + \frac{w}{w_o}\right)^2 + \left(\frac{kww_o}{2}\right)^2 \left(\frac{1}{R_o} - \frac{1}{R}\right)^2}} \tag{31}$$

$$k = \frac{2\pi}{\lambda} \tag{32}$$

In equation (31), t_q is the transmission coefficient due to beam mismatch, w_o and w are the beam widths of the system output and output fibre respectively, k is the free-space wave number, R_o and R are the beam radii of the system output and output fibre respectively, and λ is the free-space wavelength.

The transmission coefficient, as calculated in equation (31), only accounts for beam mismatch in one dimension. Using equation (31), the transmission coefficient due to $\overline{S}'$ can be determined. The complete transmission coefficient is then the product of t_q and t_q'.

5.4.2. Beam Offset and Tilt

The beam offset and tilt can be determined simply by directing a beam along the input optical axis. The distance and angle of this beam with respect to the output optical axis is the offset and tilt. Fortunately, these parameters are easily calculated using $\overline{S}$.

$$\begin{aligned} \vec{r}_o &= \overline{S}\begin{bmatrix} y_i & \alpha_i & 1 \end{bmatrix}^T \\ \vec{r}_o &= \overline{S}\begin{bmatrix} 0 & 0 & 1 \end{bmatrix}^T \end{aligned} \tag{33}$$

The components of $\vec{r}_o$ will determine the offset and tilt. Because of the simple form of the input vector, the output vector can be read directly from the system matrix. This leads to the following values for the offset and tilt.

$$r_{oy} = \overline{S}_{1,3} = d$$
$$r_{o\alpha} = \overline{S}_{2,3} = \theta \qquad (34)$$

We can see from equation (34) that r_{oy} and $r_{o\alpha}$ map direct to single elements of the system matrix. The naming of these elements should now be clear. The beam offset and tilt can be read directly from the system matrix, and for this particular example, can be determined by using equations (25) and (26).

The transmission coefficient due to beam offset and tilt can be calculated using the following equations [10]. Equations (35) and (37) are the transmission coefficients for tilt and offset respectively. Equations (36) and (38) represent the tilt and offset tolerances.

$$t_\theta = \sqrt{\exp\left[-\left(\frac{\theta}{\theta_e}\right)^2\right]} \qquad (35)$$

$$\theta_e = \frac{2^{3/2}}{kt_q\sqrt{w_o^2 + w^2}} \qquad (36)$$

$$t_d = \sqrt{\exp\left[-\left(\frac{d}{d_e}\right)^2\right]} \qquad (37)$$

$$d_e = \frac{2^{1/2}}{t_d\sqrt{\frac{1}{w_o^2} + \frac{1}{w^2}}} \qquad (38)$$

The transmission coefficient for the axis, including all effects, is simply the product of t_q, t_θ, and t_d.

$$t = t_q t_\theta t_d \tag{39}$$

5.4.3. Example

Using the full expression for $\overline{S}$, the minimum and maximum values for the system elements for the matrix were determined. Design parameters were all 500μm (f_c, f_f, l_1, and l_2). The lateral fabrication tolerances were assumed to be ±2μm ($x_?$ and $y_?$)[41]. The angular fabrication tolerances were all taken to be ±0.0133 radians[42] ($\alpha_?$). Finally, the operating wavelength was assumed to be 1.55μm. This led to the following minimum and maximum values for the elements of $\overline{S}$.

$$\overline{S_{\min}} = \begin{bmatrix} 0.999936 & -0.000008 & -0.000021 \\ -32 & 0.999936 & -0.042934 \\ 0 & 0 & 1 \end{bmatrix} \tag{40}$$

$$\overline{S_{\max}} = \begin{bmatrix} 1.000128 & 0.000008 & 0.000021 \\ 32 & 1.000128 & 0.042934 \\ 0 & 0 & 1 \end{bmatrix} \tag{41}$$

The beam wavefronts are planar when the beam exits the fibre. This implies $R \to \infty$. We will also assume that the input beam has a width of 6.556 μm. Thus, $\tilde{q}_i$ is i87.1 μm. Using equation (30), $\tilde{q}_o$ is found to be virtually equal to $\tilde{q}_i$. Note that this is also the complex radius of curvature desired for perfect coupling into the output fibre. The transmission coefficient is greater than 99% ($0.99 < t_q < 1$) with the variations in the system matrix. By far, coupling loses are dominated by beam offset, d, and beam tilt, θ.

[41] A tolerance of 2μm, while representing the minimum spacing for the MUMPs process, is probably too large. Since staple self-align to the underlying hinges because of conformal deposition, and since the pixel size of the masks is 0.1μm, fabrication tolerances may be as low as 0.1μm

[42] $\alpha_?$ = arctan(4μm / 300μm)

Unfortunately, the beam offset and tilt cause a large insertion loss. The offset tolerance is virtually equal to the beam width, $d_e = 6.556$ μm. Noting that only the absolute value of the beam mismatch is important, the beam offset of 21 μm is clearly going to cause a significant insertion loss. Similarly, the tilt tolerance is 0.075 radians, while beam tilt is actually 0.043 radians, is going to cause significant insertion loss.

Combining the transmission coefficients for all three effects, the transmission coefficient will be only 5.0×10^{-3}. The transmittivity is thus only 2.5×10^{-5}. Excluding coupling loses for the other axis[43], the switch's insertion loss will be 46 dB.

If the lenses are Fresnel-zone plates, then their transmission efficiencies also need to be considered. A brief treatment of Fresnel-zone plate transmittivity is provided in the next chapter.

For designers, it is important to note that from the equations for tilt and offset tolerance, equations (36) and (38), that beam width mismatch, while diminishing the optimal coupling efficiency, will increase the tilt and offset tolerances. As a general rule, optimal coupling efficiency, t_q, can be traded for greater alignment tolerance. Techniques for increasing the offset and tilt tolerances, at the expense of peak coupling efficiency, can be found in [10]. For the manufacturing tolerances outlined here, the coupling efficiency would need to be managed to obtain a reliable product.

5.5. CONCLUSION

The use of a homogeneous co-ordinate system creates a simple extension to ray-transfer matrices. The extended method provides a concise notation that can handle manufacturing tolerances in paraxial optical systems. Once the system matrix has been assembled, the system's properties are readily available for both simple ray tracing and Gaussian beam tracing.

[43] Also excluding coupling losses due to component curvature.

The mathematical tool presented here should be of great service to micromachined optical systems. The ability to analytically characterize a system's performance is of great engineering value. Designers can now see what system parameters most affect, for example, coupling losses.

5.6. REFERENCES

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CHAPTER 6
DESIGN

This chapter will cover the implementation of a free-space optical switch. The switch will make use of the electrostatic self-assembly process previously discussed to create many of the optical devices. The discussion will start with hinges, which create the rotational freedom that is central to the assembly process. Focus will then move to the various devices that are needed to create the fibre-optic switch: Fresnel-zone plates, fibre pipe scaffolds, and mirrors. Near the end of this chapter, designs for the two chips that have been fabricated and tested will be presented.

6.1. HINGES

Ideally, hinges should prevent translation of the attached structure while allowing rotation. The development of surface micro-machined hinges in the early 1990s led to a whole new class of surface micro-machined devices [1] [2]. Devices can be fabricated flat, which is required by the limitations of the surface micro-machining process, and, following release, rotated off the wafer surface and assembled into fully 3D structures. While there are three types of micro-machined hinges, raised structures primarily use staple hinges[44]. Their design is therefore of particular importance.

As mentioned in the chapter on techniques for surface micro-machined designs, the design of even relatively simple components, such as pads and conducting lines, is easily complicated. These complications unfortunately hold for staple hinges as well. The simplest staple hinge design, outlined in Figure 38, contains a number of problems.

[44] Staple hinges are also known as substrate hinges.

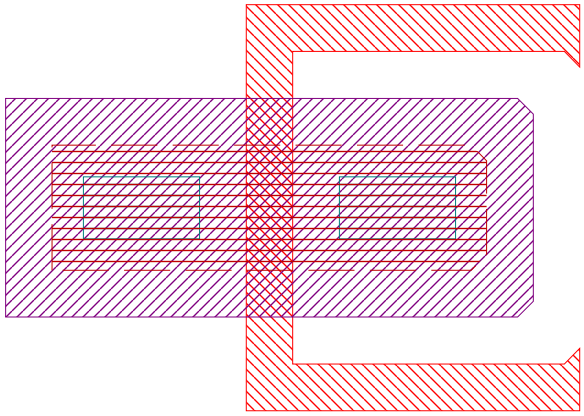

Figure 38: Mask layout for standard staple hinge design.

The success of a hinge design clearly revolves[45] around the shape of its interior space. Athena[46] is a useful software tool for verifying hinge designs since it is capable of simulating the fabrication steps used in surface micromachining. The source code for all Athena simulations is available in the appendices.

Below is a simulated cross-section of the standard staple hinge design, Figure 39, and an SEM[47] image showing the profile of a standard staple, Figure 40. While the interior space is large enough for 3 μm wide and 2 μm thick axle to rotate at the centre, the two wings visible in Figure 39 are not. If the component shifts before being raised, then the axle will become lodged in one of the wings, where it is no longer free to rotate. This difficulty is especially important for structures that are to be raised manually. Manipulation with probe needles will very likely push the structure into one of the wings.

[45] No pun intended.
[46] Silvaco International, 4701 Patrick Henry Drive, Santa Clara, California, 95054, USA.
[47] SEM is an acronym for scanning electron microscope.

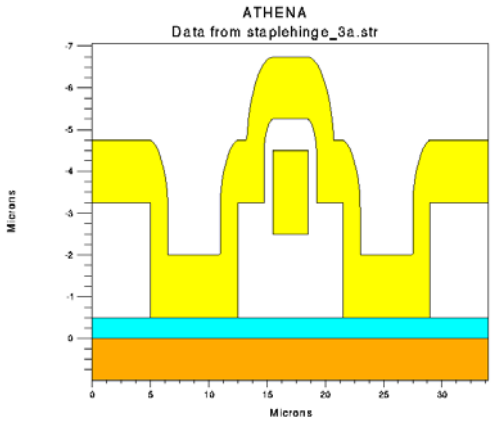

Figure 39: Cross-section of standard staple hinge design.

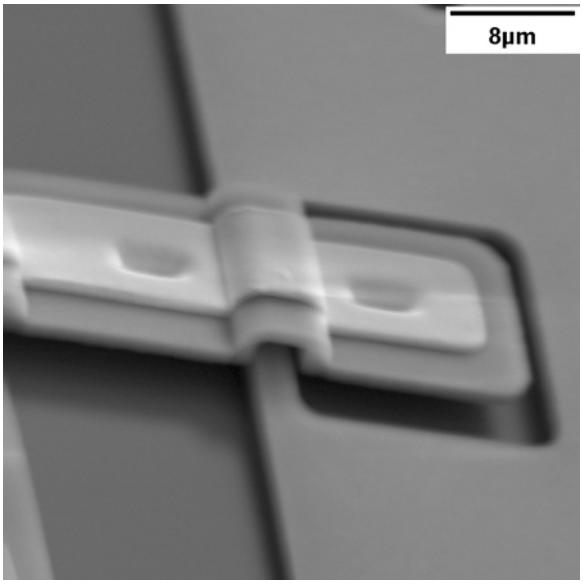

Figure 40: SEM showing profile of a staple.

While focusing on the cross-section, it is important to remember that overhangs exist all around the anchor. Thus, if the component shifts in any direction it can be caught under the second structural layer.

To overcome the difficulties of the standard staple hinge design, a number of variations were tried. The final version, Type E, is very different. The mask layout and simulated cross-section are shown in Figure 41 and Figure 42 respectively. Please refer to the Athena Listings for source code for the simulation. First, instead of using POLY2 and ANCHOR2 to create the staple, POLY1 is included. The POLY2 layer is connected to the wafer surface through POLY1, instead of directly. This reduces the height of the wings in the interior space from 2.75 µm to 2.0 µm. The POLY1 is nominally 2.0 µm thick, so there is still the possibility that the hinge will become trapped. The DIMPLE layer is used on the wings to lower them another 0.75 µm. The heights of the wings are reduced to only 1.25 µm.

Another major difference between Type-A and Type-E hinge designs is that, except along the interior, all of the enclosure rules have been ignored in the Type-E design. This leads to the outside edges of the staple hinge's anchors having relatively smooth surfaces, which present no spaces in which the rotating part can become trapped.

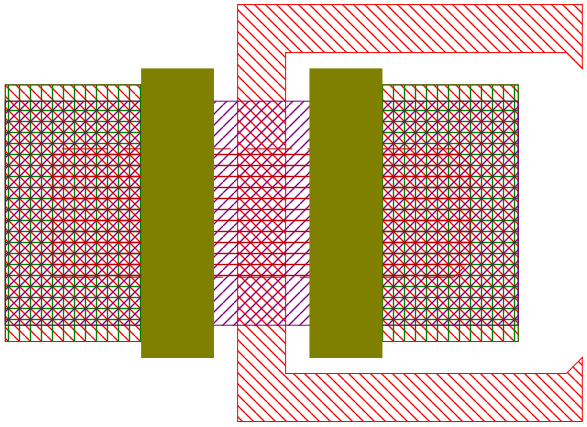

Figure 41: Mask Layout for Type E staple hinge design.

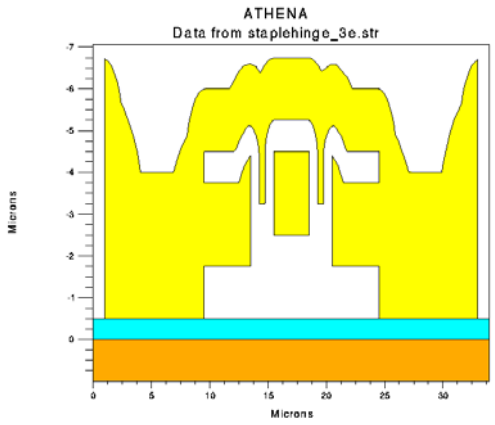

Figure 42: Cross-section of Type E staple hinge design.

Both hinge designs contain sufficient space for a 3µm by 2µm rod to rotate. Any rotating component will also have dimples to prevent adhesion to the wafer surface, so the point of rotation is 1.75 µm high. This is outlined in Figure 43 and Figure 44. Figure 43 also show how a hinge, lodged in one of the wings, will not be able to fully rotate.

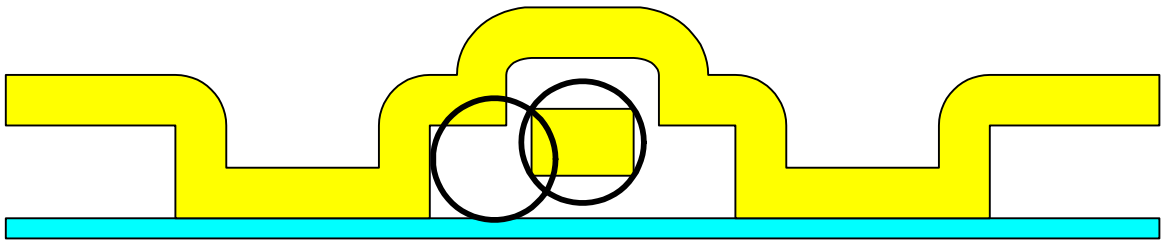

Figure 43: Rotation in a standard staple hinge.

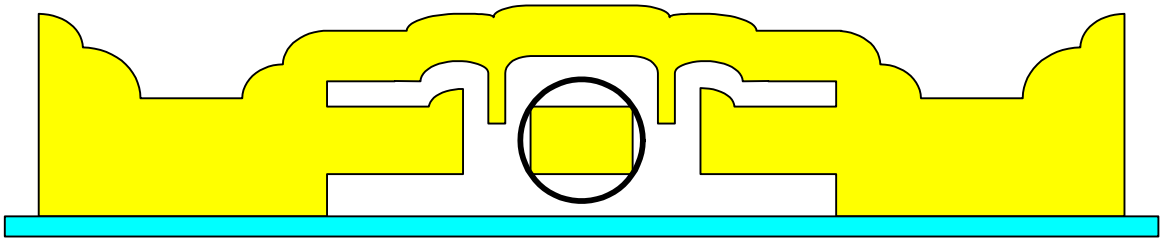

Figure 44: Rotation in a Type E staple hinge.

6.2. FRESNEL-ZONE PLATES

Fresnel-zone plates (FZP), which are also known as binary-amplitude Fresnel lenses [3], can be used as lenses like the much more common glass or plastic lenses. Unlike refractive optical lenses, Fresnel-zone plates focus light through interference effects. This requires that the light be coherent. While not as generally applicable as refractive lenses, Fresnel-zone plates have a major advantage for surface micromachining. Fresnel-zone plates can be easily constructed in all surface micromachining processes.

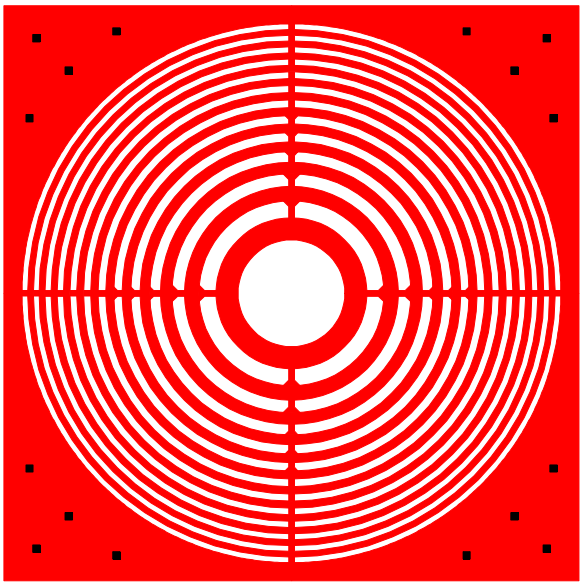

Figure 45: Mask layout for a Fresnel-zone plate.

Micromachined refractive lenses have also been demonstrated [4]. The refractive lenses use a surface micromachined frame. Photoresist is reformed after release by heating. During reflow, gravity plays a very small role compared to surface tension. The resulting surfaces of the photoresist are nearly spherical, resulting in a lens.

6.2.1. Focal Length

The alternating regions of transparent and opaque regions are called Fresnel zones. By blocking every other zone, light with planar wavefronts passing through the plate will constructively interfere at the focal point. The zone radii required to achieve constructive interference at a distance f_1 can be determined by the following equation:

$$R_N^2 = \left(f_1 + \frac{N\lambda}{2} \right)^2 - f_1^2 \qquad (42)$$

$$R_N^2 = N f_1 \lambda \qquad (43)$$

In equation (42), R_N is the radius of the Nth boundary, λ is the wavelength of the light, and, as above, f_1 is the distance to the point of constructive interference. When the wavelength, λ, is much greater than f_1, approximations can be made which lead to the equation (43).

To generalize, the FZP will act as a lens with a focal length of f_1 for light with a wavelength λ. FZPs can thus be very useful for optics involving monochromatic, or nearly monochromatic, light. Setting $N = 1$ leads to a simple equation to determine the focal length of a FZP:

$$f = f_1 = \frac{R_1^2}{\lambda} \qquad (44)$$

However, unlike a standard lens that uses refraction, a FZP has multiple focal points. As one moves from the main focal point towards the plate along the axis, the same radius R_1 actually covers more Fresnel zones. When one reaches the point half the length of f_1 from the plate, the first zone actually covers two zones for the new position, where all light therefore destructively interferes. Continuing to one third of f_1, the original R_1 actually covers three Fresnel zones. Again, constructive interference occurs

and an additional focal point can be found. However, the intensity at this point is only 1/9 the intensity at f_1. The other focal points, and their relative intensities, can be found by the following equations:

$$f_N = \frac{R_1^2}{N}, N \text{ odd} \tag{45}$$

$$I_N = \frac{I_1}{N^2}, N \text{ odd} \tag{46}$$

6.2.2. Transmission Efficiency

A FZP has lower transmission efficiency than a refractive lens. Even if the FZP is large enough to capture all of the light from the source (so we can ignore the effects of the lens' aperture), the opaque sections of FZP will still absorb much of the light.

As a rough rule of thumb, the transmission efficiency can be approximated by the ratio of the opaque area to the total area of the FZP. Since the alternating rings of a FZP are of equal area [5], this indicates that the transmission efficiency of a FZP is at most 50% (neglecting the area taken up by the supports). A more accurate approximation can be obtained by using equation (46). The intensity of the transmitted light should equal the sum of the intensity at all of the focal points.

$$I_T = \sum_{n=0}^{\infty} \frac{I_1}{(2n+1)^2} = \frac{\pi^2 I_1}{8} \tag{47}$$

Despite the existence of an infinite number of focal points, the power contained in the higher order focal points (N>1) is only a small portion of the transmitted power. The main focal point, f_1, receives 81% of the transmitted light, for an overall transmission efficiency of 41%.

6.3. FIBRE PIPE SCAFFOLDS

The prototype chip, described later, contains basically one type of device, a raised plate. Although some of the raised plates contained Fresnel-zones, the method of assembly is the same as for simple plates and mirrors.

To align optical fibre to the Fresnel-zone plates, and to exercise the self-assembly technique, the current design additionally has four fibre pipes. While not actually pipes, these structures are essentially scaffolding designed to hold an optical fibre with a radius of 250 μm.

Each pipe is a linear array of a basic cell, which has a layout shown in Figure 46. The largest structure, which is shaped like a 'U', has a semi-circular space. This is the region into which the fibre will fit. The two largest vertical supports to the left and right are designed to mate with the 'U' section during assembly.

Because of the size of the 'U' structure, the fibre pipe's basic cell is quite large, and would not provide consistent support to the optical fibre. To overcome this, and to make use of the available space, smaller structures that only provide vertical support are included in the basic cell. Several of the smaller structures should be visible running along the central vertical axis of the design. These structures have a height of 45 μm.

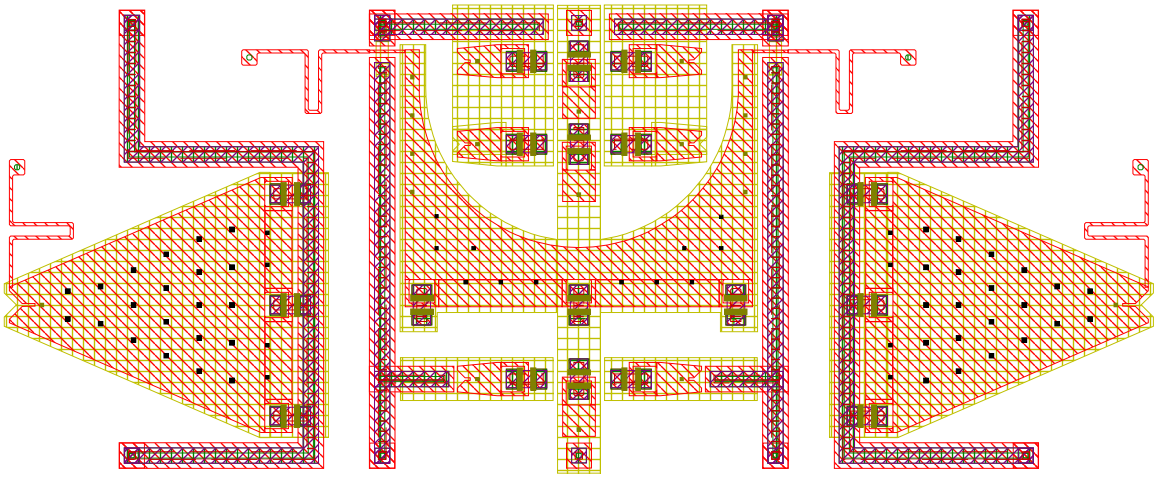

Figure 46: Mask layout for unit cell of fibre pipe.

6.4. MIRRORS

The mirrors are the simplest components of the design. However, a few additional comments are in order.

Optically flat mirrors are not possible with the MUMPs process [6]. To achieve optically flat mirrors, a number of effects must be controlled. Dimples, which are used to create bumps on the bottom surface of the mirror, are needed to prevent adhesion. Because of the conformal deposition process, each dimple also creates a small indentation on the top surface of the mirror. This effect can be overcome by polishing the top surface of the mirror during fabrication.

Additionally, surface micro-machined mirrors are curved due to non-uniform stresses [7]. The curvature could be accounted for during optical modelling and corrected for, but only if the radius of curvature was fixed. However, Cronos does not specify any control on the non-uniform stresses [8].

Also preventing ideal operation, surface micro-machined mirrors require regularly spaced etch holes. Without the etch holes, the sacrificial material beneath the mirror will not be completely removed, and the mirror will remained physically connected to the

wafer surface. While not affecting the optical flatness of the mirror, the etch holes will contribute to optical losses, because, obviously, holes do not reflect. Additionally, because the holes are regularly spaced, there may be interference effects [9].

Finally, while polysilicon is fairly reflective for visible light, it is transparent to light with wavelengths in the infrared region [10]. The infrared region is an especially important regime for optical systems because of its importance to long distance fibre-optic systems. The MUMPs process can be used, since gold, the metal used in the MUMPs process, is very reflective in the infrared. However, the enclosure rules for polysilicon and gold can greatly increase the optical size of the etch holes.

6.5. PROTOTYPE DESIGN

Prototype chips were fabricated using the MUMPs process, available through Cronos. The prototype design was originally intended to be the core of an optical switch design [11], but not the entire system. A number of the chips' features reflect this fact. However, the optical switch design that the prototype chips reflect was not pursued. The key concern of these chips is the electrostatic actuation of the mirrors. Figure 47 shows the mask layout for the prototype design.

The design includes four FZPs. Originally, testing was planned using a HeNe laser as the light source. The lenses were therefore designed for an operating wavelength of 680 nm. The short operating wavelength is noticeable in the design of the Fresnel-zones plates. The zones do not extend to the edge of the lens. Unfortunately, the zone widths would have to be less than 2 μm, which is the minimum spacing rule for the MUMPs process [8].

The FZPs were not designed for electrostatic self-assembly. However, they are all connected to a conducting line. This line exists to provide an actuation voltage to the FZPs. While self-supporting once assembled, the actuation voltage is used to increase the vertical alignment accuracy during operation.

The prototype design contained four mirrors. These mirrors were designed for electrostatic actuation.

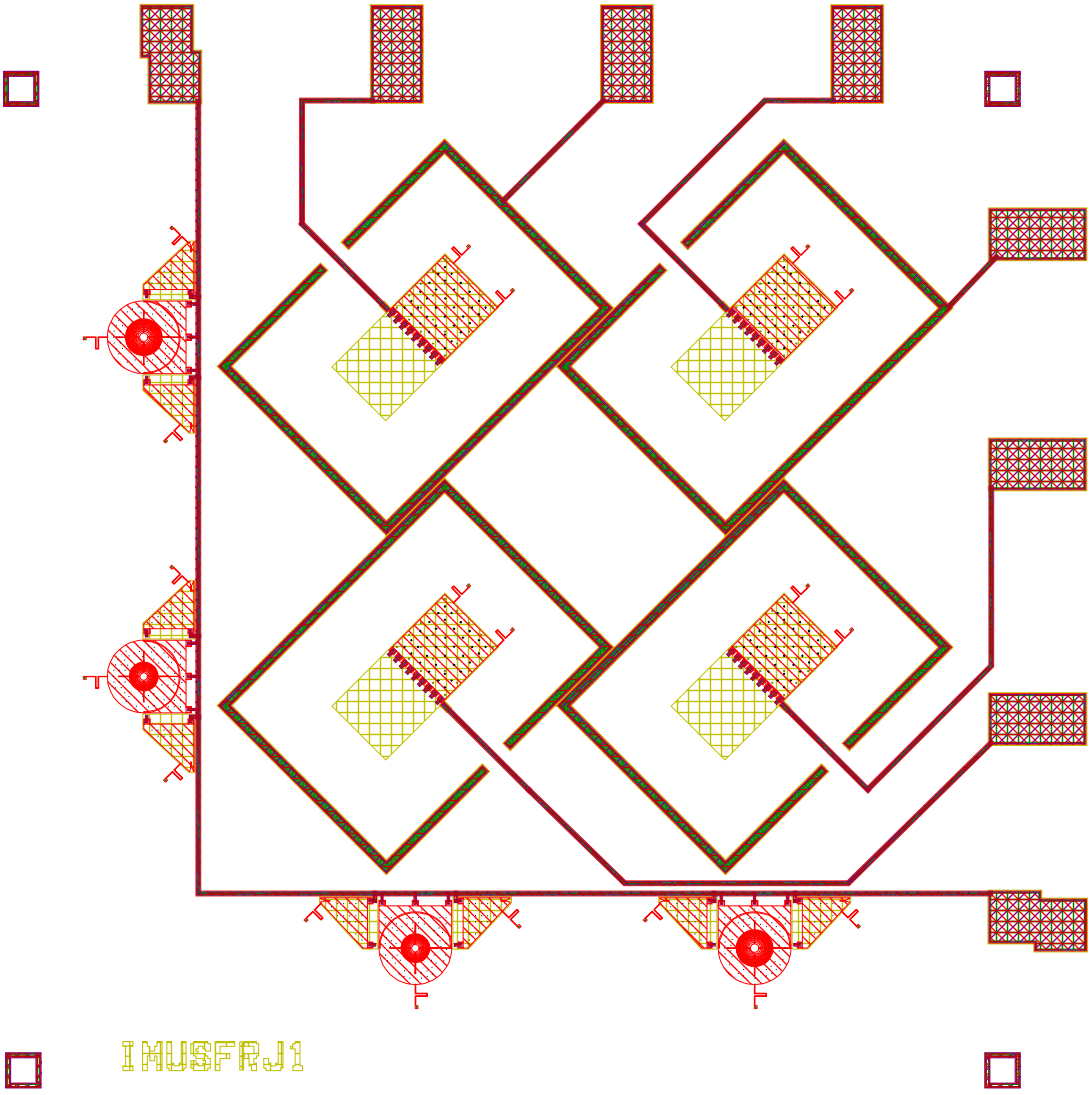

Figure 47: Layout for prototype chip (IMUSFRJ1).

6.6. CURRENT DESIGN

Figure 48 shows the mask layout of the most current design for the optical switch using electrostatic self-assembly [13]. Unlike the prototype chip, the entire optical switch

is to be fabricated using surface micromachining. The optical switch occupies a region shaped like a '+' through the centre of the chip. The optical switch does not use the corners of the chip. To avoid wasting space, a large number of other, unrelated, devices are located in these regions.

While both the prototype and the current design are for 2x2 switches, the current design uses only a single mirror, instead of the four used in the prototype design. This frees up considerable chip real estate, which can be used for testing other projects. However, the current design cannot be directly extended to create NxN switches.

Neglecting the unrelated regions, the optical switch design still appears quite complex. However, it is made up of a small number of similar parts. First, the switch contains four fibre pipes scaffolds. The fibre pipes and their arrangement are what gives the switch its '+' shape. At the head of each pipe is a self-assembling FZP. The lenses are all designed to collimate light exiting a fibre placed in the nearest fibre-pipe.

This design was optimized for operation at 1550 nm. Wavelength selection impacts switch design mainly in two areas. As previously mentioned, Fresnel-zone plates must be designed for specific wavelength. This design change is very trivial. More importantly, poly-silicon is transparent at this wavelength [10]. The mirrors thus use the metal layer of the MUMPs process, and so are coated with gold.

At the crossroads of the fibre pipes is a single mirror. When lying flat, the two horizontally located fibres form an optical path, and the two vertically located fibres form a second optical path. When a voltage is applied, the mirror is actuated and is placed in both optical paths. When the mirror is raised, the top and right fibres are connected and the left and bottom fibres are connected.

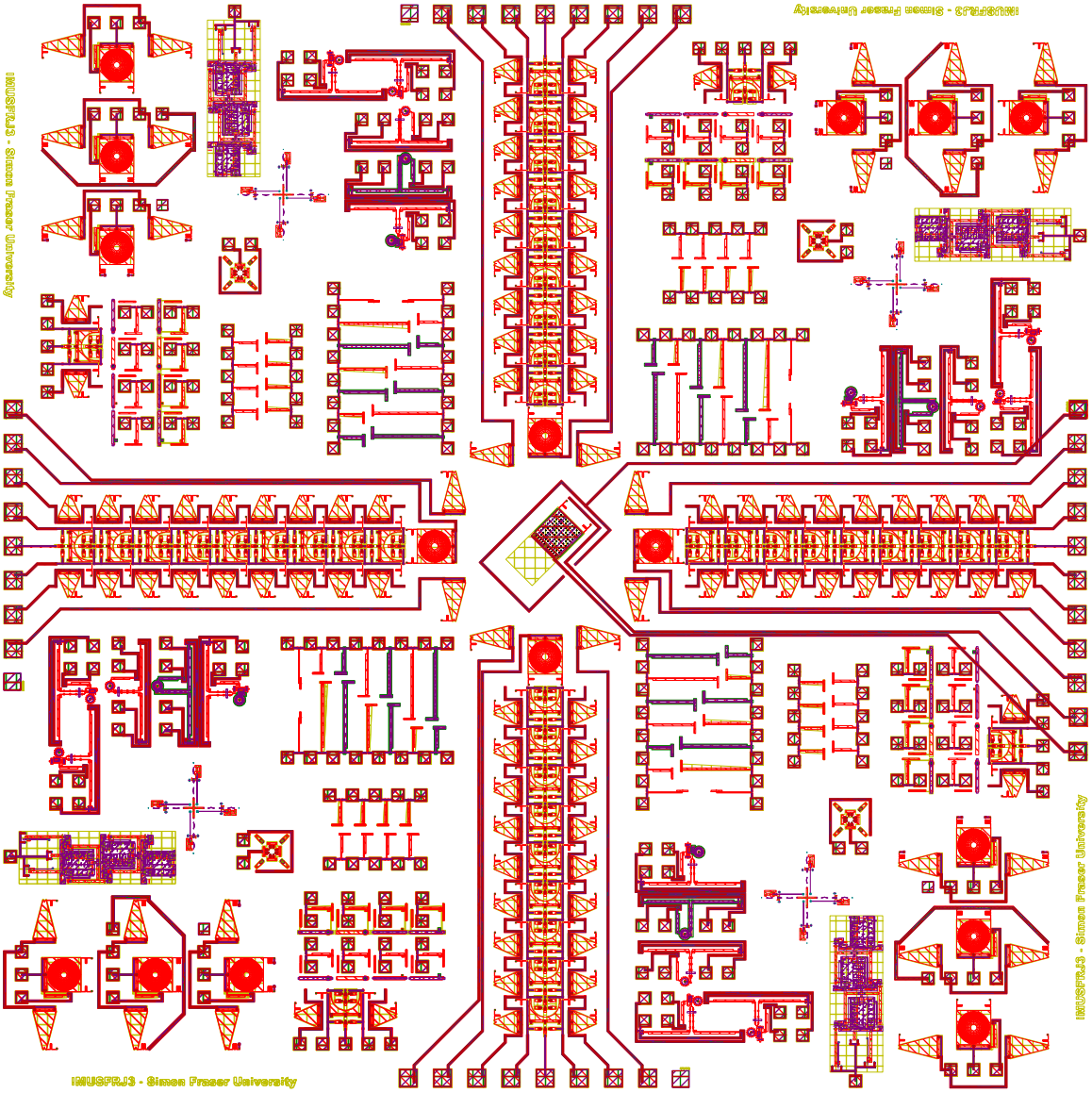

Figure 48: Layout for most current chip (IMUSFRJ3).

Because of the design's symmetry, all optical paths are essentially the same. This one optical path was modeled using traditional non-homogeneous ray-transfer matrices. The optical fibre is assumed to have an effective beam radius of 6.556 μm. To keep the geometry easy, the distance between all components is 500 μm.

The beam width and beam curvature are plotted in Figure 49 and Figure 50. The positions of the optical components are noted in the figures. The maximum beam width[48] is only 38 μm. Since the optical components all have radii of 150 μm, aperture effects are virtually non-existent.

Although not very visible, it should be noted that the beam curvature approaches infinity at both the input and output of the system.

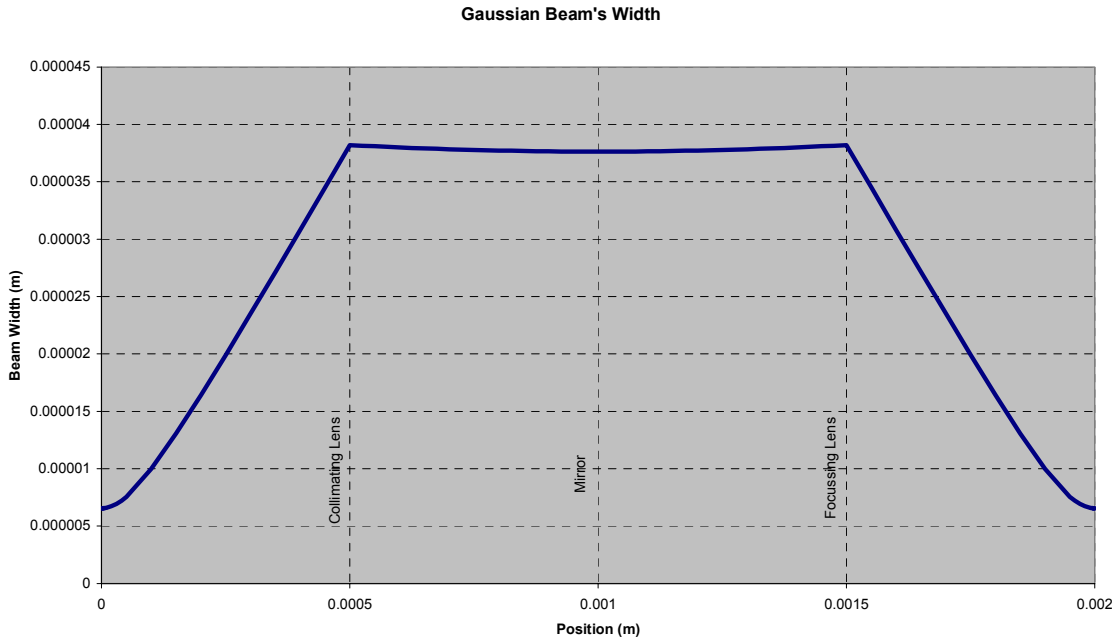

Figure 49: Plot of Gaussian beam's radius vs. position in optical switch.

[48] Measured from centre to e^{-2} intensity points.

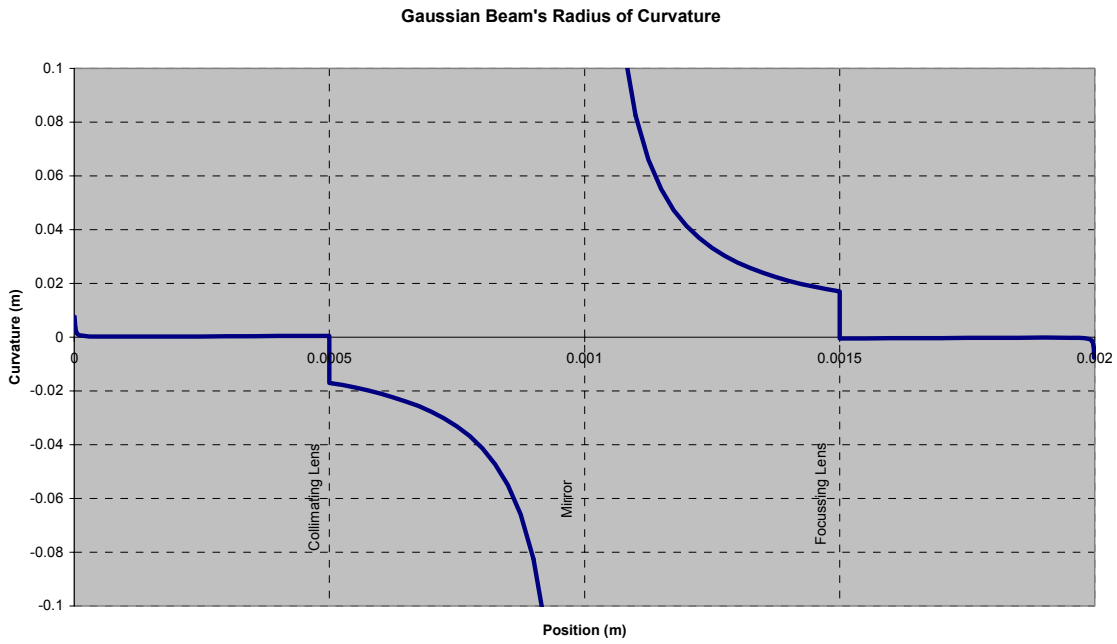

Figure 50: Plot of Gaussian beam's radius of curvature vs. position in optical switch.

6.7. REFERENCES

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CHAPTER 7
TESTS AND RESULTS

7.1. PROTOTYPE DESIGN

We fabricated several chips with hinged mirrors (Figure 51) through Cronos. We mounted the chips on standard 48-pin packages. We also deposited a thin film of titanium on 1x3 inch glass slides. The conducting layer was thin enough to be mostly transparent.

7.1.1. Fresnel-zone Plates

The Fresnel-zone plates (FZP) were designed for manual assembly using micromanipulators. Unfortunately, none of the FZPs were successfully assembled.

The size of the micromanipulator tips made assembly very difficult. When the lens is resting on its dimples, the space between the lens and the underlying ground plane is only 0.75 μm. Finding manipulators with tips sufficiently small is difficult. Further, the micromanipulator tips are quickly bent or blunted with use. Despite the relatively large size of the manipulator's tips, one can, with careful coercion, slide the micromanipulators under the lenses.

Even with the micromanipulators in place, the FZP could not be lifted very far. The FZPs became stuck and would visibly flex. Forcing the manipulator too high would simply break the hinges. The Fresnel-zone plates all used type A hinge designs. It is thus believed that the hinges became trapped in the staple wings, which hindered assembly.

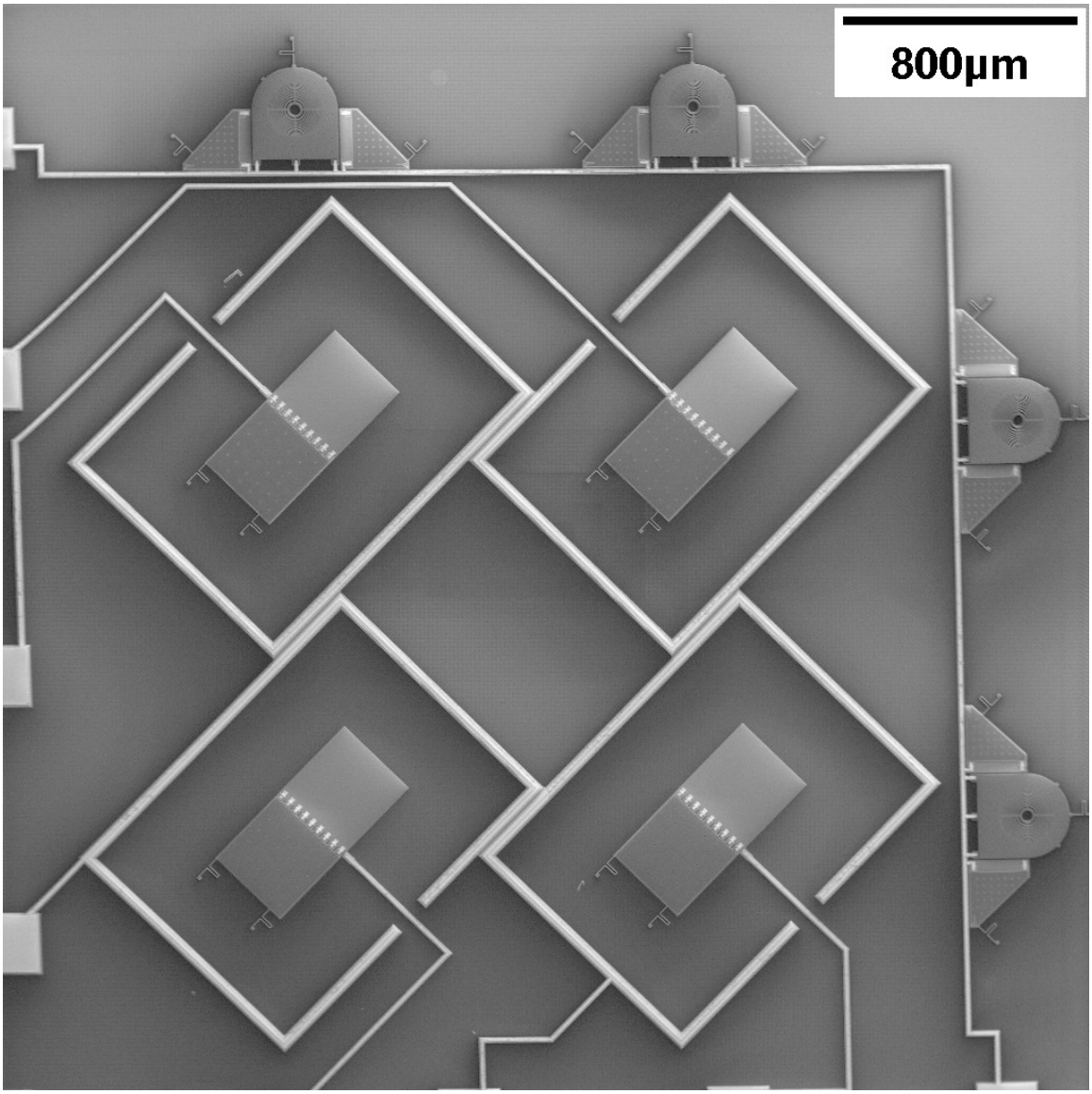

Figure 51: SEM of prototype chip (IMUSFRJ1).

7.1.2. Mirrors

As can be seen in Figure 51, the prototype chips each contained four 300 µm by 300 µm plates. Each plate had nine standard hinges. The plates all had ground planes,

which were connected to bonding pads along the edges of the chip. The chips were mounted on 48-pin ceramic packages[49] and bonded.

To test the electrostatic actuation, a thin layer of titanium was deposited onto standard microscope glass slides[50]. The metal layer was thin enough to have a transmittivity of approximately 50%. A conducting wire was connected to the metal-coated side of the slide using conducting epoxy. The glass slide was then placed on top of the ceramic package with the metal film face down.

This configuration matches the one described in the theory section for electrostatic actuation.

Using the package's pins, voltage was applied between the glass slides and the mirrors. Mirror actuation was easily verified by using an optical microscope. The actuation voltages typically varied around 35-40 volts. Occasionally, voltages as high as 50 volts were required. We were able to lift and lower each mirror several times. Our first prototype was a simple test of the electrostatic lifting so vertical supports were not included.

Surprisingly, the main difficulty with the prototype is lowering the plates. Once raised, the plates will remain standing even after the applied voltage is returned to zero. A sharp tap to the side or top of the ceramic package lowered the mirrors. This may be the result of adhesion between the hinge and staple, but further investigation is needed.

The main difficulty with the original design was that the mirrors often fell onto their top face, which had no dimples. When this happened, the mirror often adhered to the wafer surface and could not be raised again.

[49] Manufacturer NTK; Part # IDK-48f1-62221AA.
[50] 1 x 3 inches.

Unfortunately, the mirrors just as often fell over onto their topside as to their original position. This is important since the underside of the mirrors contain dimples to prevent adhesion to the ground plane. While I was often able to raise mirrors that fell onto their top side, it was just as likely that the mirror would adhere. Once adhesion had occurred, the mirror cannot be raised. Voltages as high as 300V were used without success. This is not surprising considering the extremely high adhesion energy of poly-silicon surfaces [1] [2].

The prototype chips were retested after approximately a year. Unfortunately, the mirrors did not actuate. The failure is most likely related to adhesion, as shown in Figure 52. The axles have adhered to the staple. More problematic, the staple has adhered within the cavity created by the conformal deposition of the second structural material. Since the sacrificial layer separating the axle from the staple is only 0.75 μm, the cavity is a very close fit.

7.2. CURRENT DESIGN

The current design (Figure 53) looks very little like the prototype chips. The only structure recognizable in both designs is the mirrors. Unlike the prototype, the current design attempts to include all of the fibre alignment. The current design thus uses fibre-pipe scaffolds for all of the input and output fibres. Another important change was to reduce the number of mirrors.

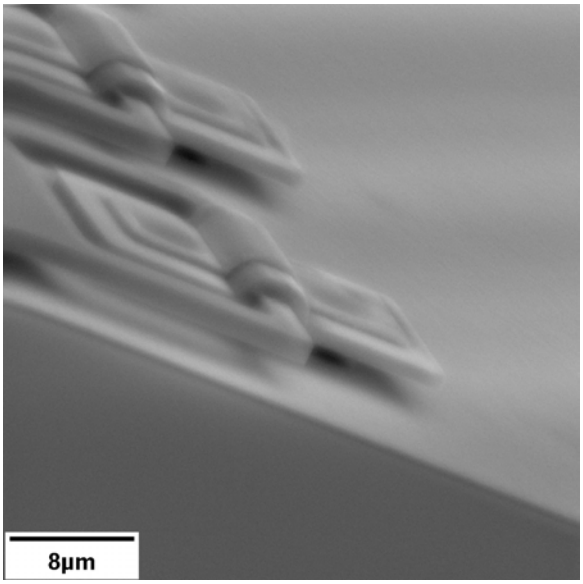

Figure 52: SEM of staple hinges where axle has adhered to the staple, preventing rotation.

The mirror, which forms the heart of the optical switch, is visible at the right

of Figure 53. Three fibre pipes are also visible. A fourth pipe is present, but to the right of the central mirror. At the end of each fibre pipe is a Fresnel-zone plate.

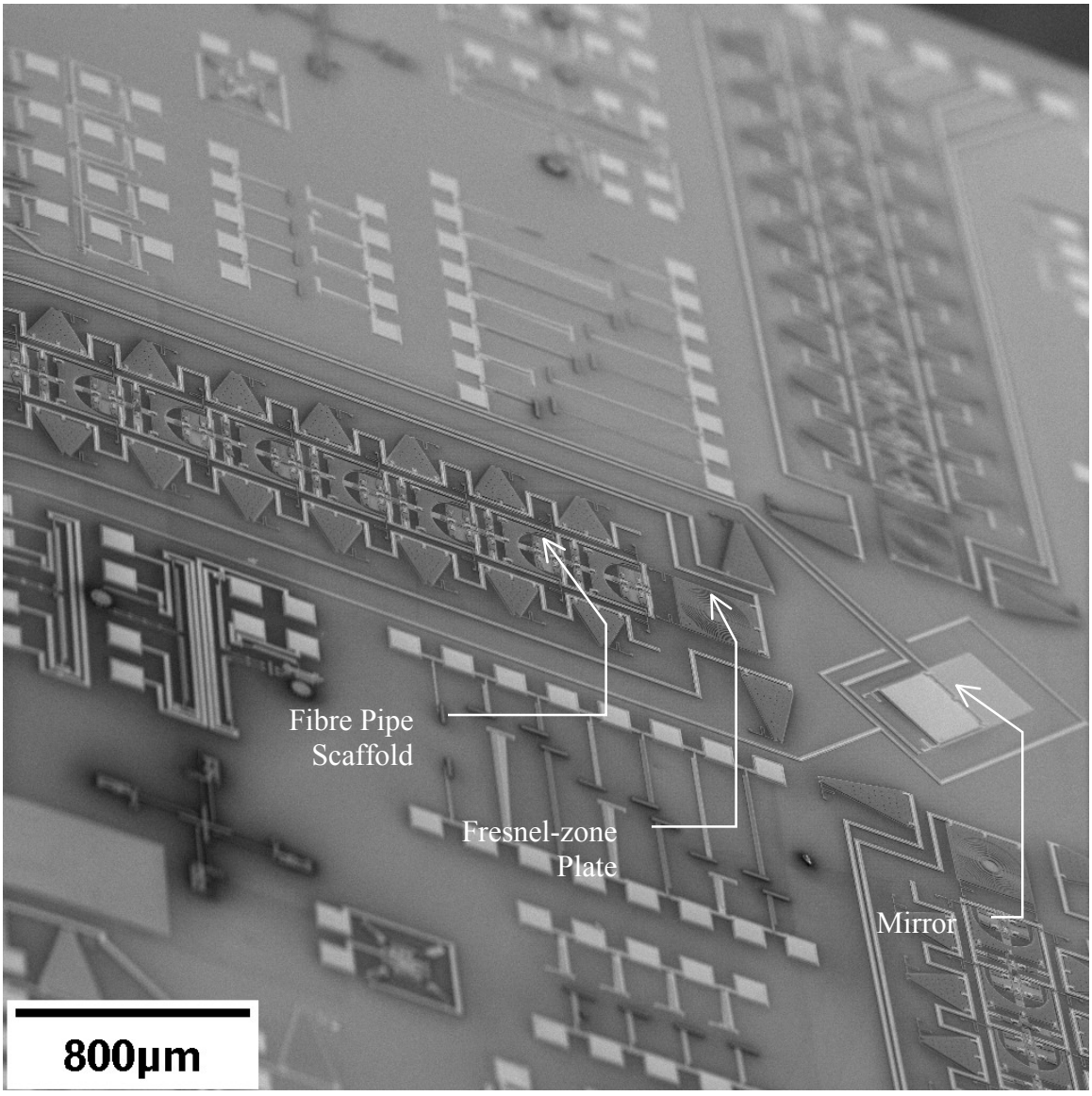

Figure 53: SEM of most current chip (IMUSFRJ3).

The current design tries to ensure that the mirrors fall onto their correct side (Figure 54). This is partially accomplished by placing a ridge along the staple hinges

opposite the plate. This should prevent the plate's face from coming into contact with the wafer surface if it falls backwards.

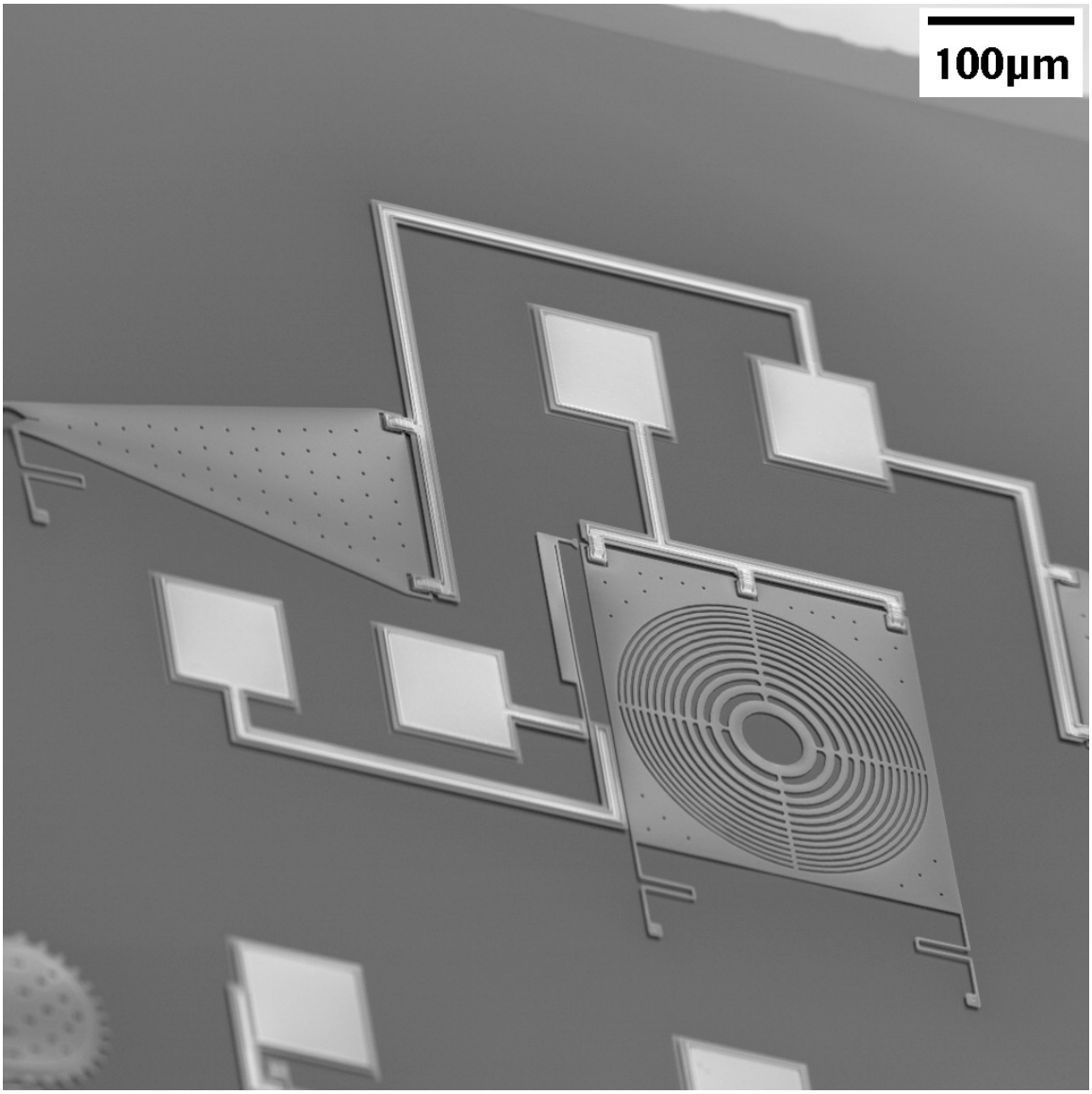

Figure 54: SEM of self-assembling Fresnel-zone plate

Unfortunately, the electrostatic assembly process was not successful. The components did not lift-off the wafer surface. The reason for the failure is evident in the following SEMs.

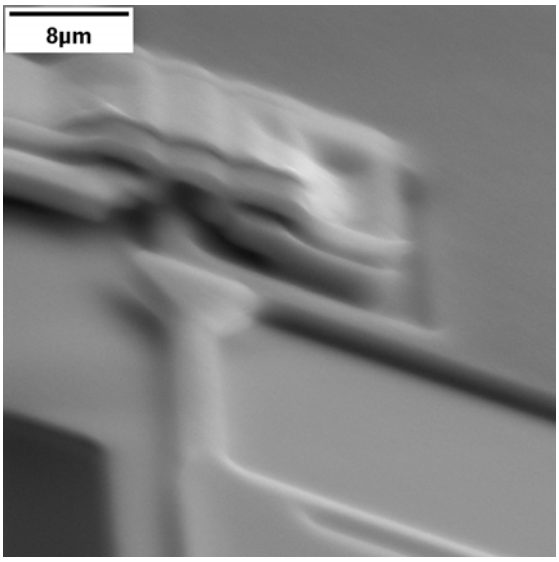

Figure 55: SEM close-up of Type-E hinge used for self-assembling Fresnel-zone plate.

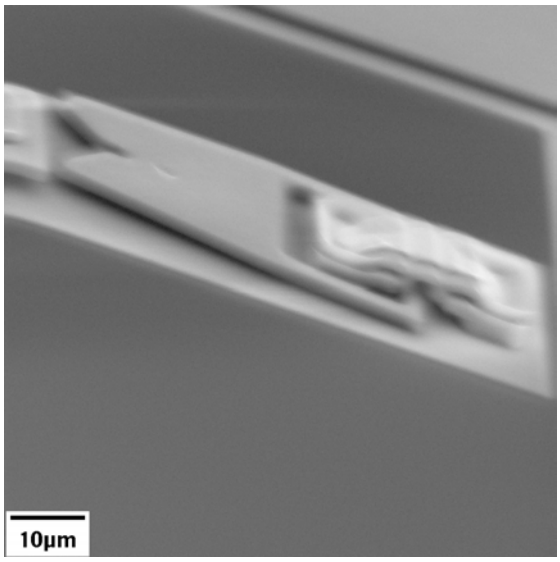

Figure 56: SEM close-up of short vertical support used in fibre-pipe.

Figure 55 is a close-up of one hinge from a self-assembling Fresnel-zone plate. The plate is touching the POLY0 ground plane and so has certainly adhered. The plate does have dimples placed along the top edge to prevent adhesion, but they are clearly too far away.

Similarly, Figure 56 shows one of the small vertical supports used in the fibre-pipe scaffolds. Because of the relatively close placement of the dimple near the mating slot, the region of adhesion is entirely visible. The axle, including the 20 µm connecting rods, has adhered to the POLY0 ground plane. The body of the vertical support angles up from the POLY0 to accommodate the dimple's height.

In addition to adhesion, the design of the small vertical supports has interference faults. This is clearly visible in Figure 57. While the Type-E hinge design does have space for the axle to rotate, the axle has shifted position. In the depicted position, the hinge can no longer freely rotate.

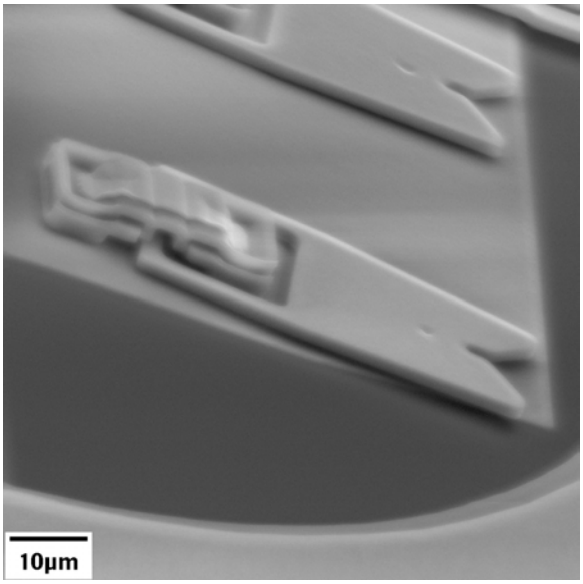

Figure 57: SEM close-up of staple hinge that has shifted.

Despite being designed to avoid traps for the axle, the design has failed to consider hinges with zero height above the zero polysilicon. While this entrapment may be a contributing factor to the assembly method's failure, it is not a real design fault of the hinge design. To avoid adhesion, better dimple spacing is clearly required. With dimples, the axle would maintain a height of 0.75 μm. At this height, the axle can no longer fit underneath the lips.

7.3. REFERENCES

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CHAPTER 8
CONCLUSION

Surface micromachining, by borrowing from the wealth of knowledge obtained for microelectronics fabrication, is capable of creating very complicated structures. However, the essentially planar processing, also borrowed from microelectronics fabrication, is often a major limitation for mechanical and optical-mechanical systems. This limitation can be overcome by including hinges in the surface micromachined designs.

However, including hinges requires additional fabrication steps. These steps are outside of the planar processing, and so are also outside of microelectronic fabrication techniques. Only a few proposals for accomplishing the assembly of the micromachined[51] components exist. This thesis suggests that electrostatic forces are best suited for the assembly process.

The electrostatic assembly was used in the design of a fibre-optic 2x2 switch. Besides using electrostatic assembly for Fresnel-zone plates, which can be assembled by other means, electrostatic assembly was also used in the construction of a fibre-pipe scaffold. Creating scaffolds, which require a large number of parts, would not be possible using the other methods suggested, as they are serial processes.

Electrostatic assembly can be a parallel process, which has significant implications for mass fabrication of devices.

Much work remains for the future. The hinge designs need further refinement to ensure proper dimple positioning. Hopefully, the electrostatic assembly method can be completed with this modification.

[51] The proposed methods are micromanipulators and surface tension.

If successful, the method can be extended to other types of structures. Although not presented in this thesis, preliminary designs for boxes with open and closed tops have been implemented. The complete list of structures and scaffolds is left for future development.

APPENDIX A
DESIGN RULES

A.1. MINIMUM AND NOMINAL WIDTH

This rule applies to all single shapes. The classic definition is that all lines must be at least as wide as the minimum width (Figure 58). More generally, this is the minimum dimension for all features. Any features that is less than the minimum width across in size may be undersized or missing. The minimum feature size is set by limitations in the mask making and lithographic processes.

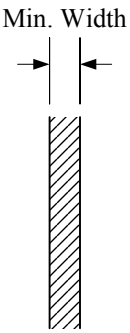

Figure 58: Illustration of minimum width design rule.

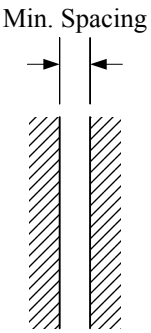

Figure 59: Illustration of minimum spacing design rule.

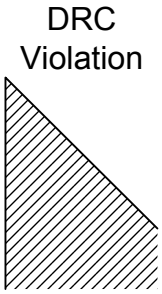

Figure 60: Acute angles will cause DRC errors.

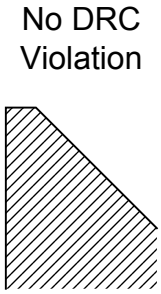

Figure 61: Acute angle has been chopped to avoid DRC error.

An important impact of this rule is that all acute angles will break the design rules (Figure 60). To avoid these errors, acute corners must be chopped (Figure 61)

A.2. MINIMUM AND NOMINAL SPACING

Two separate shapes cannot be placed arbitrarily close to each other, even if they are on different layers (Figure 59). Violating the minimum spacing rule can lead to fused parts.

A.3. MINIMUM ENCLOSURE

This rule applies to two shapes on different mask layers. If the designer wants to ensure that shape A is completely covered by shape B, then this is the size of the boundary that shape B must provide around the perimeter of shape A (Figure 62).

Minimum enclosure rules are important for anchors and vias. Minimum enclosure rules ensure that the holes cut in the sacrificial layer are completely covered by the following structural material.

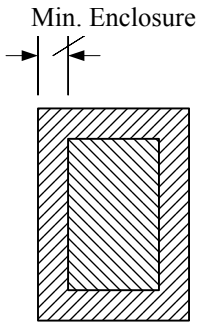

Figure 62: Illustration of minimum enclosure design rule.

A.4. CUT-INSIDE AND CUT-OUTSIDE

These rules also apply to two shapes on different mask layers. They are similar to the minimum enclosure rules, but apply instead to shapes that only partially overlap.

These rules specify the minimum lengths that features must overlap in the design to ensure that they do in fact overlap in the fabricated device (Figure 63 and Figure 64).

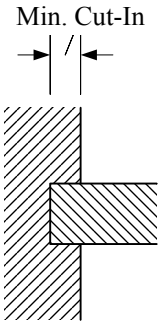

Figure 63: Illustration of minimum cut-in design rule.

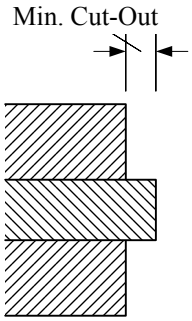

Figure 64: Illustration of minimum enclosure design rule.

APPENDIX B
ANSYS LISTINGS

B.1. ELECTROSTATIC SIMULATION FOR LOWERED PLATE

```
1.    FINISH
2.
3.    !
4.    !         Gather Modelling Parameters
5.    !
6.    /CLEAR
7.    *ASK,R,Size of hinge,20
8.    *ASK,S,Size of plate,300
9.    *ASK,H,Height of grounding plane,500
10.   *ASK,W,Width to model,S*4
11.
12.   !
13.   !         Initialize Coarse Model
14.   !
15.   /FILENAME,file_coarse
16.   /TITLE,SAM Mirror (Coarse Model)
17.
18.
19.   /PREP7
20.   ET,1,PLANE121
21.   ET,2,INFIN110,1,0,0,
22.
23.   MP,PERX,1,1,
24.   MP,PERX,2,7.5,                      ! silicon nitride
25.   MP,PERX,3,11.7,                     ! silicon
26.
27.   RECTNG,-W/2,W/2,-S,0,               ! silicon wafer
28.   RECTNG,-W/2,W/2,0,0.6,              ! nitride layer
29.   RECTNG,-S-R-4,S+R+4,0.6,1.1,        ! POLY0
30.   RECTNG,R,R+S,3.1,5.1,               ! POLY1 plate
31.   RECTNG,-W/2,W/2,0.6,H,              ! air region
32.   APTN,ALL
33.   AGLUE,ALL
34.   NUMCMP,ALL
35.
36.   ASEL,S,LOC,Y,-S/2,
37.   AATT,3, , , ,
38.   ASEL,S,LOC,Y,0.3,
39.   AATT,2, , , ,
40.   ASEL,S,LOC,Y,0.85
41.   AATT,3, , , ,
42.   ASEL,S,LOC,Y,4.1
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```
43.   AATT,3, , , ,
44.   ASEL,S,LOC,Y,H/2
45.   AATT,1, , , ,
46.   ASEL,ALL
47.
48.   SMRTSIZE,OFF
49.   MSHKEY,1
50.   ESIZE,2,0                   ! mesh POLY0
51.   ASEL,S,LOC,Y,0.85
52.   AMESH,ALL
53.   ASEL,S,LOC,Y,0.3,           ! mesh nitride
54.   LSEL,S,LOC,Y,0.6,
55.   LCCAT,ALL
56.   AMESH,ALL
57.   ESIZE,2,0                   ! mesh POLY1
58.   ASEL,S,LOC,Y,4.1,           ! mesh POLY1
59.   AMESH,ALL,
60.   ESIZE,0,0,                  ! mesh rest
61.   MSHKEY,0
62.   MOPT,EXPND,4
63.   MOPT,TRANS,4
64.   SMRTSIZE,3
65.   ASEL,S,LOC,Y,-S/2,
66.   AMESH,ALL,
67.   ASEL,S,LOC,Y,H/2,
68.   AMESH,ALL,
69.
70.   LSEL,ALL
71.   ASEL,ALL
72.   ARSCALE,ALL, , ,1e-6,1e-6,1e-6, ,0,1
73.   FINISH
74.
75.   /SOLU
76.   ASEL,S,LOC,Y,0.85e-6,
77.   DA,ALL,VOLT,1,
78.   ASEL,S,LOC,Y,4.1e-6,
79.   DA,ALL,VOLT,1,
80.   ASEL,ALL
81.   LSEL,S,LOC,Y,H*1e-6,
82.   DL,ALL,,VOLT,0,
83.   LSEL,ALL
84.   EMUNIT,MKS
85.   SOLVE
86.   FINISH
87.
88.   /POST1
89.   /TRIAD,OFF
90.   PLNSOL,EF,Y,0,
91.   SAVE
92.
```

```
93.   !
94.   !         Initialize Sub-Model
95.   !
96.   /PREP7
97.   ALLSEL,ALL                          ! Reselect Everything
98.   ACLEAR,ALL,                         ! Clear out any meshes
99.   ADELE,ALL,,1,                       ! Delete all areas and below
100.  LDELE,ALL,,,1                       ! Delete all lines and below
101.  KDELE,ALL
102.  FINISH
103.  /FILENAME,file_submodel
104.  /TITLE,SAM Mirror (Sub-Model)
105.
106.  /PREP7
107.  RECTNG,-S-R-4,S+R+4,0.6,1.1,        ! POLY0
108.  RECTNG,R,R+S,3.1,5.1,               ! POLY1 plate
109.  RECTNG,-W/2,W/2,0.6,5.1+10, ! air region
110.  APTN,ALL
111.  AGLUE,ALL
112.  NUMCMP,ALL
113.
114.  ASEL,S,LOC,Y,0.85
115.  AATT,3, , , ,
116.  ASEL,S,LOC,Y,4.1
117.  AATT,3, , , ,
118.  !ASEL,S,LOC,Y,15.1/2,
119.  ASEL,S,AREA,,3,
120.  AATT,1, , , ,
121.  ASEL,ALL
122.
123.  ESIZE,1,0
124.  AMESH,ALL
125.  ARSCALE,ALL, , ,1e-6,1e-6,1e-6, ,0,1
126.
127.  LSEL,S,LOC,X,-W/2*1e-6,     ! Select Boundary Lines
128.  LSEL,A,LOC,X,W/2*1e-6,
129.  LSEL,A,LOC,Y,15.1e-6,
130.  NSLL,S,1                    ! Select Associated Nodes
131.  NWRITE                      ! Writes all selected nodes to
      Jobname.NODE
132.  ALLSEL,ALL                  ! Reselect everything
133.  SAVE                        ! Save the database
134.
135.  RESUME,file_coarse,db       ! Resume from the coarse model
136.  FINISH                      ! Preform nodal interpolation for cut-
      model
137.  /POST1
138.  FILE,file_coarse,rth,       ! Redirect to results from coarse
      model
139.  SET,FIRST                   ! Read in results
```

```
140.  CBDOF                        ! Preform nodal interpolation
141.  FINISH                       ! Finished nodal interpolation
142.  RESUME                       ! Resume the sub-model
143.
144.  /SOLU
145.  /INPUT,,cbdo                 ! Read in the nodal constraints
146.  ASEL,S,LOC,Y,4.1e-6
147.  DA,ALL,VOLT,1,
148.  ESLA,S
149.  CM,'plate',ELEM
150.  FMAGBC,'plate'
151.  ALLSEL,ALL
152.  SOLVE                        ! Solve the model
153.  FINISH
154.
155.  /POST1                       ! Enter postprocessor
156.  /TRIAD,OFF
157.  /PLOPTS,MINM,0
158.  PLNSOL,VOLT,                 ! Plot the von Mises Stress
159.  FMAGSUM
160.  FINISH
161.  SAVE
```

B.2. ELECTROSTATIC SIMULATION FOR RAISED PLATE

```
1.    FINISH
2.
3.    !
4.    !         Gather Modelling Parameters
5.    !
6.    /CLEAR
7.    *ASK,R,Size of hinge,20
8.    *ASK,S,Size of plate,300
9.    *ASK,H,Height of grounding plane,500
10.   *ASK,W,Width to model,S*4
11.
12.   !
13.   !         Initialize Coarse Model
14.   !
15.   /FILENAME,file_coarse
16.   /TITLE,SAM Mirror (Coarse Model)
17.
18.
19.   /PREP7
20.   ET,1,PLANE121
21.   ET,2,INFIN110,1,0,0,
22.
23.   MP,PERX,1,1,
24.   MP,PERX,2,7.5,                    ! silicon nitride
25.   MP,PERX,3,11.7,                   ! silicon
```

```
26.
27.   RECTNG,-W/2,W/2,-S,0,                ! silicon wafer
28.   RECTNG,-W/2,W/2,0,0.6,               ! nitride layer
29.   RECTNG,-S-R-4,S+R+4,0.6,1.1,         ! POLY0
30.   RECTNG,-1,1,1.1+R,1.1+R+S,           ! POLY1 plate
31.   RECTNG,-W/2,W/2,0.6,H,               ! air region
32.   APTN,ALL
33.   AGLUE,ALL
34.   NUMCMP,ALL
35.
36.   ASEL,S,LOC,Y,-S/2,
37.   AATT,3, , , ,
38.   ASEL,S,LOC,Y,0.3,
39.   AATT,2, , , ,
40.   ASEL,S,LOC,Y,0.85
41.   AATT,3, , , ,
42.   ASEL,S,LOC,Y,1.1+R+S/2
43.   AATT,3, , , ,
44.   ASEL,S,LOC,Y,H/2
45.   AATT,1, , , ,
46.   ASEL,ALL
47.
48.   SMRTSIZE,OFF
49.   MSHKEY,1
50.   ESIZE,2,0                   ! mesh POLY0
51.   ASEL,S,LOC,Y,0.85
52.   AMESH,ALL
53.   ASEL,S,LOC,Y,0.3,           ! mesh nitride
54.   LSEL,S,LOC,Y,0.6,
55.   LCCAT,ALL
56.   AMESH,ALL
57.   ESIZE,2,0,                            ! mesh POLY1
58.   ASEL,S,LOC,Y,1.1+R+S/2,               ! mesh POLY1
59.   AMESH,ALL,
60.   ESIZE,0,0,                            ! mesh rest
61.   MSHKEY,0
62.   MOPT,EXPND,4
63.   MOPT,TRANS,4
64.   SMRTSIZE,3
65.   ASEL,S,LOC,Y,-S/2,
66.   AMESH,ALL,
67.   ASEL,S,LOC,Y,H/2,
68.   AMESH,ALL,
69.
70.   ALLSEL
71.   ARSCALE,ALL, , ,1e-6,1e-6,1e-6, ,0,1
72.   FINISH
73.
74.   /SOLU
75.   ASEL,S,LOC,Y,0.85e-6,
```

```
76.   DA,ALL,VOLT,1,
77.   ASEL,S,LOC,Y,(1.1+R+S/2)*1e-6,
78.   DA,ALL,VOLT,1,
79.   ESLA,S
80.   CM,'plate',ELEM
81.   FMAGBC,'plate'
82.   ALLSEL
83.   LSEL,S,LOC,Y,H*1e-6,
84.   DL,ALL,,VOLT,0,
85.   LSEL,ALL
86.   EMUNIT,MKS
87.   SOLVE
88.   FINISH
89.
90.   /POST1
91.   /TRIAD,OFF
92.   PLNSOL,EF,Y,0,
93.   FMAGSUM
94.   SAVE
```

B.3. MECHANICAL SIMULATION FOR RAISED PLATE (TYPE A)

```
1.    FINISH
2.
3.    !
4.    !         Gather Modelling Parameters
5.    !
6.    /CLEAR
7.    *ASK,F,Pulling force on the mirror (N),10e-6
8.    *ASK,THCK,Thickness of mirror (m),2e-6
9.
10.   !
11.   !         Initialize Coarse Model
12.   !
13.   /FILENAME,file_coarse
14.   /TITLE,SAM Mirror (Coarse Model)
15.
16.   /PREP7
17.   ET,1,PLANE42,,,3
18.   R,1,THCK
19.
20.   MP,EX,1, 169e9
21.   MP,NUXY,1, 0.22
22.   MP,DENS,1, 2331
23.
24.   RECTNG,-19,0,-150,-148
25.   RECTNG,-21,-19,-150,-130
26.   RECTNG,-21,-19,-146,-134
27.   RECTNG,-19,0,-132,-130
28.   RECTNG,-19,0,-10,-8
```

```
29.   RECTNG,-21,-19,-10,10
30.   RECTNG,-21,-19,-6,6
31.   RECTNG,-19,0,8,10
32.   RECTNG,-19,0,130,132
33.   RECTNG,-21,-19,130,150
34.   RECTNG,-21,-19,134,146
35.   RECTNG,-19,0,148,150
36.   APTN,ALL
37.   NUMCMP,ALL
38.   RECTNG,0,300,-150,150
39.   AGLUE,ALL
40.   NUMCMP,ALL
41.
42.   ESIZE,1,
43.   AMESH,1,15
44.   ESIZE,4,
45.   SMRTSIZE,1,
46.   AMESH,16
47.
48.   ARSCALE,ALL,,,1e-6,1e-6,1e-6,,0,1
49.   FINISH
50.
51.   /SOLU
52.   ANTYPE,0
53.   LSEL,S,LOC,X,-19e-6,
54.   LSEL,R,LOC,Y,140e-6,
55.   DL,ALL,,ALL,0
56.   LSEL,S,LOC,X,-19e-6,
57.   LSEL,R,LOC,Y,0e-6,
58.   DL,ALL,,ALL,0
59.   LSEL,S,LOC,X,-19e-6,
60.   LSEL,R,LOC,Y,-140e-6,
61.   DL,ALL,,ALL,0
62.   LSEL,S,LOC,X,300e-6,
63.   SFL,ALL,PRES,-F / 300e-6 / THCK
64.   ALLSEL
65.   SOLVE
66.   FINISH
67.
68.   /POST1
69.   /TRIAD,OFF
70.   /PLOPTS,MINM,0
71.   /DSCALE,1,OFF
72.   PLNSOL,S,EQV,0,1
73.   !*GET,MAXSEQV,PLNSOL,0,MAX
74.   !*STATUS,MAXSEQV
75.   FINISH
76.   SAVE
77.
78.   !
```

```
79.   !         Initialize Sub-Model
80.   !
81.   /PREP7
82.   ALLSEL                                ! Reselect Everything
83.   ACLEAR,ALL,                           ! Clear out any meshes
84.   ADELE,ALL,,1,                         ! Delete all areas and below
85.   LDELE,ALL,,,1                         ! Delete all lines and below
86.   KDELE,ALL
87.   FINISH
88.   /FILENAME,file_submodel
89.   /TITLE,SAM Mirror (Sub-Model)
90.
91.   /PREP7
92.   ET,1,PLANE42,,,3
93.   R,1,THCK
94.
95.   MP,EX,1, 169e9
96.   MP,NUXY,1, 0.22
97.   MP,DENS,1, 2331
98.
99.   RECTNG,-19,0,-150,-148
100.  RECTNG,-21,-19,-150,-130
101.  RECTNG,-21,-19,-146,-134
102.  RECTNG,-19,0,-132,-130
103.  RECTNG,0,20,-150,-110,
104.  APTN,ALL
105.  AGLUE,ALL
106.  NUMCMP,ALL
107.
108.  ESIZE,.25,
109.  AMESH,ALL
110.  ESIZE,,
111.
112.  ARSCALE,ALL,,,1e-6,1e-6,1e-6,,0,1
113.
114.  LSEL,S,LOC,Y,-110e-6,       ! Select Boundary Lines
115.  LSEL,A,LOC,X,20e-6,
116.  NSLL,S,1                    ! Select Associated Nodes
117.  NWRITE                      ! Writes all selected nodes to
      Jobname.NODE
118.  ALLSEL                      ! Reselect everything
119.  SAVE                        ! Save the database
120.  RESUME,file_coarse,db       ! Resume from the coarse model
121.
122.  FINISH                      ! Preform nodal interpolation for cut-
      model
123.  /POST1
124.  FILE,file_coarse,rst,       ! Redirect to results from coarse
      model
125.  SET,FIRST                   ! Read in results
```

```
126.  CBDOF                        ! Preform nodal interpolation
127.  FINISH                       ! Finished nodal interpolation
128.  RESUME                       ! Resume the sub-model
129.  /SOLU
130.  /INPUT,,cbdo                 ! Read in the nodal constraints
131.  LSEL,S,LOC,X,-19e-6          ! Apply hinge constraint
132.  LSEL,R,LOC,Y,-140e-6         ! Apply hinge constraint
133.  DL,ALL, ,ALL,0
134.  ALLSEL
135.  SOLVE                        ! Solve the model
136.  FINISH
137.
138.  /POST1                       ! Enter postprocessor
139.  /TRIAD,OFF
140.  /PLOPTS,MINM,0
141.  /DSCALE,1,OFF
142.  PLNSOL,S,EQV,0,1             ! Plot the von Mises Stress
143.  *GET,MAXSEQV,PLNSOL,0,MAX    ! Extract the maximum stress
144.  *STATUS,MAXSEQV              ! Display the maximum stress
145.  FINISH
146.  SAVE
147.
148.  !
149.  !         Initialize Sub-Sub-Model
150.  !
151.  /PREP7
152.  ALLSEL                       ! Reselect Everything
153.  ACLEAR,ALL,                  ! Clear out any meshes
154.  ADELE,ALL,,1,                ! Delete all areas and below
155.  LDELE,ALL,,,1                ! Delete all lines and below
156.  KDELE,ALL
157.  FINISH
158.  /FILENAME,file_subsubmodel
159.  /TITLE,SAM Mirror (Sub-Sub-Model)
160.
161.  /PREP7
162.  RECTNG,-21,-15,-132,-130
163.  RECTNG,-21,-19,-130,-134
164.  RECTNG,-21,-19,-134,-136
165.  APTN,ALL
166.  AGLUE,ALL
167.  NUMCMP,ALL
168.
169.  ESIZE,0.05,0
170.  MSHKEY,1
171.  AMESH,ALL
172.  ESIZE,,
173.
174.  ARSCALE,ALL,,,1e-6,1e-6,1e-6,,0,1
175.
```

```
176.  LSEL,S,LOC,Y,-136e-6,       ! Select Boundary Lines
177.  LSEL,A,LOC,X,-15e-6,
178.  NSLL,S,1                    ! Select Associated Nodes
179.  NWRITE                      ! Writes all selected nodes to
      Jobname.NODE
180.  ALLSEL                      ! Reselect everything
181.  SAVE                        ! Save the database
182.  RESUME,file_submodel,db     ! Resume from the coarse model
183.
184.  FINISH                      ! Preform nodal interpolation for cut-
      model
185.  /POST1
186.  FILE,file_submodel,rst,     ! Redirect to results from coarse
      model
187.  SET,FIRST                   ! Read in results
188.  CBDOF                       ! Preform nodal interpolation
189.  FINISH                      ! Finished nodal interpolation
190.  RESUME                      ! Resume the sub-model
191.  /SOLU
192.  /INPUT,,cbdo                ! Read in the nodal constraints
193.  LSEL,S,LOC,X,-19e-6         ! Apply hinge constraint
194.  LSEL,R,LOC,Y,-135e-6
195.  DL,ALL, ,ALL,0
196.  ALLSEL
197.  SOLVE                       ! Solve the model
198.  FINISH
199.
200.  /POST1                      ! Enter postprocessor
201.  /TRIAD,OFF
202.  /PLOPTS,MINM,0
203.  /DSCALE,1,OFF
204.  PLNSOL,S,EQV,0,1            ! Plot the von Mises Stress
205.  *GET,MAXSEQV,PLNSOL,0,MAX   ! Extract the maximum stress
206.  *STATUS,MAXSEQV             ! Display the maximum stress
207.  FINISH
208.  SAVE
```

B.4. MECHANICAL SIMULATION FOR RAISED PLATE (TYPE B)

```
1.    FINISH
2.
3.    !
4.    !         Gather Modelling Parameters
5.    !
6.    /CLEAR
7.    *ASK,F,Pulling force on the mirror (N),10e-6
8.    *ASK,THCK,Thickness of mirror (m),2e-6
9.
10.   !
11.   !         Initialize Coarse Model
```

```
!
/FILENAME,file_coarse
/TITLE,SAM Mirror (Coarse Model)

/PREP7
ET,1,PLANE42,,,3
R,1,THCK

MP,EX,1, 169e9
MP,NUXY,1, 0.22
MP,DENS,1, 2331

RECTNG,-19,0,-150,-148
RECTNG,-21,-19,-150,-130
RECTNG,-21,-19,-146,-134
RECTNG,-19,0,-132,-130
RECTNG,-19,0,-10,-8
RECTNG,-21,-19,-10,10
RECTNG,-21,-19,-6,6
RECTNG,-19,0,8,10
RECTNG,-19,0,130,132
RECTNG,-21,-19,130,150
RECTNG,-21,-19,134,146
RECTNG,-19,0,148,150
APTN,ALL
NUMCMP,ALL
RECTNG,-21,0,-130,-10
RECTNG,-21,0,10,130
RECTNG,0,300,-150,150
AGLUE,ALL
NUMCMP,ALL

ESIZE,1,
AMESH,1,15
ESIZE,2,
SMRTSIZE,1,
AMESH,16,17,
ESIZE,4,
SMRTSIZE,1,
AMESH,18

ARSCALE,ALL,,,1e-6,1e-6,1e-6,,0,1
FINISH

/SOLU
ANTYPE,0
LSEL,S,LOC,X,-19e-6,
LSEL,R,LOC,Y,140e-6,
DL,ALL,,ALL,0
LSEL,S,LOC,X,-19e-6,
```

```
62.   LSEL,R,LOC,Y,0e-6,
63.   DL,ALL,,ALL,0
64.   LSEL,S,LOC,X,-19e-6,
65.   LSEL,R,LOC,Y,-140e-6,
66.   DL,ALL,,ALL,0
67.   LSEL,S,LOC,X,300e-6,
68.   SFL,ALL,PRES,-F / 300e-6 / THCK
69.   ALLSEL
70.   SOLVE
71.   FINISH
72.
73.   /POST1
74.   /TRIAD,OFF
75.   /PLOPTS,MINM,0
76.   /DSCALE,1,OFF
77.   PLNSOL,S,EQV,0,1
78.   !*GET,MAXSEQV,PLNSOL,0,MAX
79.   !*STATUS,MAXSEQV
80.   FINISH
81.   SAVE
82.
83.   !
84.   !         Initialize Sub-Model
85.   !
86.   /PREP7
87.   ALLSEL                      ! Reselect Everything
88.   ACLEAR,ALL,                 ! Clear out any meshes
89.   ADELE,ALL,,1,               ! Delete all areas and below
90.   LDELE,ALL,,,1               ! Delete all lines and below
91.   KDELE,ALL
92.   FINISH
93.   /FILENAME,file_submodel
94.   /TITLE,SAM Mirror (Sub-Model)
95.
96.   /PREP7
97.   ET,1,PLANE42,,,3
98.   R,1,THCK
99.
100.  MP,EX,1, 169e9
101.  MP,NUXY,1, 0.22
102.  MP,DENS,1, 2331
103.
104.  RECTNG,-19,0,-150,-148
105.  RECTNG,-21,-19,-150,-130
106.  RECTNG,-21,-19,-146,-134
107.  RECTNG,-19,0,-132,-130
108.  RECTNG,0,20,-150,-110,
109.  RECTNG,-21,0,-130,-110,
110.  APTN,ALL
111.  AGLUE,ALL
```

```
112.  NUMCMP,ALL
113.
114.  ESIZE,.5,
115.  AMESH,ALL
116.  ESIZE,,
117.
118.  ARSCALE,ALL,,,1e-6,1e-6,1e-6,,0,1
119.
120.  LSEL,S,LOC,Y,-110e-6,       ! Select Boundary Lines
121.  LSEL,A,LOC,X,20e-6,
122.  NSLL,S,1                    ! Select Associated Nodes
123.  NWRITE                      ! Writes all selected nodes to
      Jobname.NODE
124.  ALLSEL                      ! Reselect everything
125.  SAVE                        ! Save the database
126.  RESUME,file_coarse,db       ! Resume from the coarse model
127.
128.  FINISH                      ! Preform nodal interpolation for cut-
      model
129.  /POST1
130.  FILE,file_coarse,rst,       ! Redirect to results from coarse
      model
131.  SET,FIRST                   ! Read in results
132.  CBDOF                       ! Preform nodal interpolation
133.  FINISH                      ! Finished nodal interpolation
134.  RESUME                      ! Resume the sub-model
135.  /SOLU
136.  /INPUT,,cbdo                ! Read in the nodal constraints
137.  LSEL,S,LOC,X,-19e-6         ! Apply hinge constraint
138.  LSEL,R,LOC,Y,-140e-6        ! Apply hinge constraint
139.  DL,ALL, ,ALL,0
140.  ALLSEL
141.  SOLVE                       ! Solve the model
142.  FINISH
143.
144.  /POST1                      ! Enter postprocessor
145.  /TRIAD,OFF
146.  /PLOPTS,MINM,0
147.  /DSCALE,1,OFF
148.  PLNSOL,S,EQV,0,1            ! Plot the von Mises Stress
149.  *GET,MAXSEQV,PLNSOL,0,MAX   ! Extract the maximum stress
150.  *STATUS,MAXSEQV             ! Display the maximum stress
151.  FINISH
152.  SAVE
153.
154.  !
155.  !         Initialize Sub-Sub-Model
156.  !
157.  /PREP7
158.  ALLSEL                      ! Reselect Everything
```

```
159.  ACLEAR,ALL,                ! Clear out any meshes
160.  ADELE,ALL,,1,              ! Delete all areas and below
161.  LDELE,ALL,,,1              ! Delete all lines and below
162.  KDELE,ALL
163.  FINISH
164.  /FILENAME,file_subsubmodel
165.  /TITLE,SAM Mirror (Sub-Sub-Model)
166.
167.  /PREP7
168.  RECTNG,-21,-15,-132,-130
169.  RECTNG,-21,-19,-130,-134
170.  RECTNG,-21,-19,-134,-136
171.  APTN,ALL
172.  AGLUE,ALL
173.  NUMCMP,ALL
174.
175.  ESIZE,0.05,0
176.  MSHKEY,1
177.  AMESH,ALL
178.  ESIZE,,
179.
180.  ARSCALE,ALL,,,1e-6,1e-6,1e-6,,0,1
181.
182.  LSEL,S,LOC,Y,-136e-6,       ! Select Boundary Lines
183.  LSEL,A,LOC,Y,-130e-6,
184.  LSEL,A,LOC,X,-15e-6,
185.  NSLL,S,1                   ! Select Associated Nodes
186.  NWRITE                     ! Writes all selected nodes to
      Jobname.NODE
187.  ALLSEL                     ! Reselect everything
188.  SAVE                       ! Save the database
189.  RESUME,file_submodel,db    ! Resume from the coarse model
190.
191.  FINISH                     ! Preform nodal interpolation for cut-
      model
192.  /POST1
193.  FILE,file_submodel,rst,    ! Redirect to results from coarse
      model
194.  SET,FIRST                  ! Read in results
195.  CBDOF                      ! Preform nodal interpolation
196.  FINISH                     ! Finished nodal interpolation
197.  RESUME                     ! Resume the sub-model
198.  /SOLU
199.  /INPUT,,cbdo               ! Read in the nodal constraints
200.  LSEL,S,LOC,X,-19e-6        ! Apply hinge constraint
201.  LSEL,R,LOC,Y,-135e-6
202.  DL,ALL, ,ALL,0
203.  ALLSEL
204.  SOLVE                      ! Solve the model
205.  FINISH
```

```
206.
207.  /POST1                      ! Enter postprocessor
208.  /TRIAD,OFF
209.  /PLOPTS,MINM,0
210.  /DSCALE,1,OFF
211.  PLNSOL,S,EQV,0,1            ! Plot the von Mises Stress
212.  *GET,MAXSEQV,PLNSOL,0,MAX   ! Extract the maximum stress
213.  *STATUS,MAXSEQV             ! Display the maximum stress
214.  FINISH
215.  SAVE
```

APPENDIX C
ATHENA LISTINGS

C.1. CROSS-SECTION OF STANDARD MUMPS CONDUCTING LINE

```
1.    go athena
2.    #
3.    line x loc=-12.00 spac=0.05
4.    line x loc=12.00 spac=0.05
5.    #
6.    line y loc=0.00 spac=0.1
7.    line y loc=1.00 spac=1.00
8.    #
9.    initialize
10.   #
11.   deposit nitride             thick=0.5
12.   #etch     nitride           start    x=-1     y=-10
13.   #etch                       cont     x=-1     y=10
14.   #etch                       cont     x=1      y=10
15.   #etch                       done     x=1      y=-10
16.   #deposit  nitride           thick=0.5
17.   #etch     nitride           start    x=-12    y=-0.5
18.   #etch                       cont     x=-12    y=-10
19.   #etch                       cont     x=12     y=-10
20.   #etch                       done     x=12     y=-0.5
21.   struct outfile=mumps_line.1.str
22.   deposit oxide               thick=2.0        divisions=1
23.   etch      oxide             start    x=-6     y=-10
24.   etch                        cont     x=-6     y=10
25.   etch                        cont     x=6      y=10
26.   etch                        done     x=6      y=-10
27.   struct outfile=mumps_line.2.str
28.   deposit poly                thick=2.0        divisions=4
29.   struct outfile=mumps_line.3.str
30.   etch      poly              start    x=-12    y=-10
31.   etch                        cont     x=-12    y=10
32.   etch                        cont     x=-10    y=10
33.   etch                        done     x=-10    y=-10
34.   etch      poly              start    x=10     y=-10
35.   etch                        cont     x=10     y=10
36.   etch                        cont     x=12     y=10
37.   etch                        done     x=12     y=-10
38.   struct outfile=mumps_line.4.str
39.   deposit oxide               thick=0.75       divisions=4
40.   struct outfile=mumps_line.5.str
41.   etch      oxide             start    x=-2     y=-10
42.   etch                        cont     x=-2     y=10
```

```
43.   etch                        cont    x=2     y=10
44.   etch                        done    x=2     y=-10
45.   struct outfile=mumps_line.6.str
46.   deposit   poly              thick=1.5       divisions=4
47.   struct outfile=mumps_line.7.str
48.   etch      poly              start   x=-12   y=-10
49.   etch                        cont    x=-12   y=-5
50.   etch                        cont    x=-6    y=-5
51.   etch                        done    x=-6    y=-10
52.   etch      poly              start   x=-12   y=-10
53.   etch                        cont    x=-12   y=-3
54.   etch                        cont    x=-10   y=-3
55.   etch                        done    x=-10   y=-10
56.   etch      poly              start   x=6     y=-10
57.   etch                        cont    x=6     y=-5
58.   etch                        cont    x=12    y=-5
59.   etch                        done    x=12    y=-10
60.   etch      poly              start   x=10    y=-10
61.   etch                        cont    x=10    y=-3
62.   etch                        cont    x=12    y=-3
63.   etch                        done    x=12    y=-10
64.   struct    outfile=mumps_line.8.str
65.   deposit   alumin            thick=0.5       division=4
66.   etch      alumin            start   x=-12   y=-10
67.   etch                        cont    x=-12   y=10
68.   etch                        cont    x=-3    y=10
69.   etch                        done    x=-3    y=-10
70.   etch      alumin            start   x=3     y=-10
71.   etch                        cont    x=3     y=10
72.   etch                        cont    x=12    y=10
73.   etch                        done    x=12    y=-10
74.   #
75.   struct outfile=mumps_line.str
76.   #
77.   tonyplot -st mumps_line*.str
78.   #
79.   quit
```

C.2. CROSS-SECTION OF STANDARD STAPLE HINGE DESIGN

```
1.    go athena
2.    #
3.    line x loc=0.00 spac=0.1
4.    line x loc=34.00 spac=0.1
5.    #
6.    line y loc=0.00 spac=0.1
7.    line y loc=1.00 spac=1.00
8.    #
9.    initialize
10.   #
```

```
11.   deposit nitride             thick=0.6
12.   struct outfile=staplehinge_3a_1.str
13.   deposit oxide               thick=2.0        divisions=8
14.   struct outfile=staplehinge_3a_2.str
15.   deposit poly                thick=2.0        divisions=8
16.   struct outfile=staplehinge_3a_3.str
17.   etch      poly              start    x=0.00  y=-10
18.   etch                        cont     x=0.00   y=10
19.   etch                        cont     x=15.50  y=10
20.   etch                        done     x=15.50  y=-10
21.   etch      poly              start    x=18.50  y=-10
22.   etch                        cont     x=18.50 y=10
23.   etch                        cont     x=34.00 y=10
24.   etch                        done     x=34.00 y=-10
25.   struct outfile=staplehinge_3a_4.str
26.   deposit oxide               thick=0.75       divisions=8
27.   struct outfile=staplehinge_3a_5.str
28.   etch      oxide             start    x=5.00  y=-10
29.   etch                        cont     x=5.00   y=10
30.   etch                        cont     x=12.50  y=10
31.   etch                        done     x=12.50  y=-10
32.   etch      oxide             start    x=21.50   y=-10
33.   etch                        cont     x=21.50  y=10
34.   etch                        cont     x=29.00  y=10
35.   etch                        done     x=29.00  y=-10
36.   struct outfile=staplehinge_3a_6.str
37.   deposit   poly              thick=1.5        divisions=8
38.   struct outfile=staplehinge_3a_7.str
39.   #
40.   #
41.   struct outfile=staplehinge_3a.str
42.   #
43.   tonyplot -st staplehinge_3a*.str
44.   #
45.   quit
```

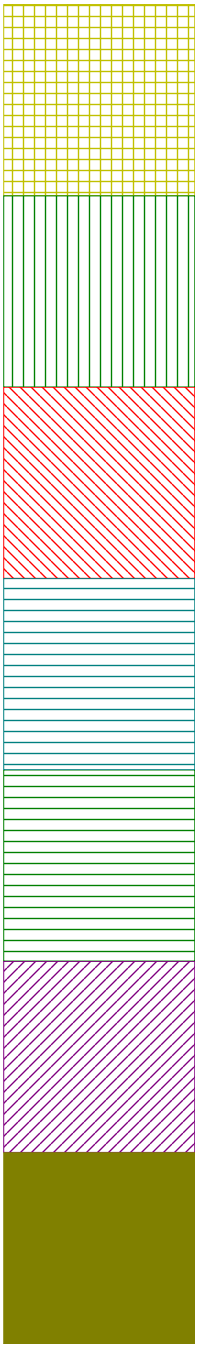
C.3. CROSS-SECTION OF TYPE E STAPLE HINGE DESIGN

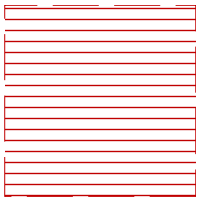
```
1.    go athena
2.    #
3.    line x loc=0.00 spac=0.05
4.    line x loc=34.00 spac=0.05
5.    #
6.    line y loc=0.00 spac=0.1
7.    line y loc=1.00 spac=1.00
8.    #
9.    initialize
10.   #
11.   deposit nitride             thick=0.6
12.   struct outfile=staplehinge_3e_1.str
```

```
13.   deposit oxide               thick=2.0        divisions=8
14.   struct outfile=staplehinge_3e_2.str
15.   etch      oxide             start    x=1.0    y=-10
16.   etch                        cont     x=1.0    y=10
17.   etch                        cont     x=9.5    y=10
18.   etch                        done     x=9.5    y=-10
19.   etch      oxide             start    x=24.5   y=-10
20.   etch                        cont     x=24.5   y=10
21.   etch                        cont     x=33.0   y=10
22.   etch                        end      x=33.0   y=-10
23.   etch      oxide             start    x=9.5    y=-10
24.   etch                        cont     x=9.5    y=-1.75
25.   etch                        cont     x=14     y=-1.75
26.   etch                        done     x=14     y=-10
27.   etch      oxide             start    x=20     y=-10
28.   etch                        cont     x=20     y=-1.75
29.   etch                        cont     x=24.5   y=-1.75
30.   etch                        done     x=24.5   y=-10
31.   struct outfile=staplehinge_3e_3.str
32.   deposit poly                thick=2.0        divisions=8
33.   struct outfile=staplehinge_3e_4.str
34.   etch      poly              start    x=0      y=-10
35.   etch                        cont     x=0      y=10
36.   etch                        cont     x=1      y=10
37.   etch                        done     x=1      y=-10
38.   etch      poly              start    x=13.5   y=-10
39.   etch                        cont     x=13.5   y=10
40.   etch                        cont     x=15.5   y=10
41.   etch                        done     x=15.5   y=-10
42.   etch      poly              start    x=18.5   y=-10
43.   etch                        cont     x=18.5   y=10
44.   etch                        cont     x=20.5   y=10
45.   etch                        done     x=20.5   y=-10
46.   etch      poly              start    x=33     y=-10
47.   etch                        cont     x=33     y=10
48.   etch                        cont     x=34     y=10
49.   etch                        done     x=34     y=-10
50.   struct outfile=staplehinge_3e_5.str
51.   deposit oxide               thick=0.75       divisions=3
52.   struct outfile=staplehinge_3e_6.str
53.   etch      oxide             start    x=1.0    y=-10
54.   etch                        cont     x=1.0    y=10
55.   etch                        cont     x=9.5    y=10
56.   etch                        done     x=9.5    y=-10
57.   etch      oxide             start    x=24.5   y=-10
58.   etch                        cont     x=24.5   y=10
59.   etch                        cont     x=33.0   y=10
60.   etch                        done     x=33.0   y=-10
61.   struct outfile=staplehinge_3e_7.str
62.   deposit   poly              thick=1.5        divisions=3
```

```
63.   struct outfile=staplehinge_3e_8.str
64.   etch      poly              start    x=0      y=-10
65.   etch                        cont     x=0      y=10
66.   etch                        cont     x=1      y=10
67.   etch                        done     x=1      y=-10
68.   etch      poly              start    x=33     y=-10
69.   etch                        cont     x=33     y=10
70.   etch                        cont     x=34     y=10
71.   etch                        done     x=34     y=-10
72.   struct outfile=staplehinge_3e_9.str
73.   #
74.   #
75.   struct outfile=staplehinge_3e.str
76.   #
77.   tonyplot -st staplehinge_3e*.str
78.   #
79.   quit
```

APPENDIX D
MASK LAYOUT LEGEND





METAL

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Assistant for Theses

From: Dr. Ash M. Parameswaran
Senior Supervisor

Date: _____

Re: Robert W. Johnstone's Thesis

I herewith certify that all required revisions and corrections on Robert W. Johnstone's M.A.Sc. thesis entitled "Electrostatic Self-Assembly of Raised Surface Micromachined Structures for Optics" have been made, and that the work is now complete to the satisfactionof the supervisory committee.

_____

Dr. Ash M. Parameswaran
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